User's Guide

DLP® Discovery™ 4100 Development Platform

ABSTRACT

The DLP Discovery 4100 Development Platform, or D4100 Platform, is an evaluation platform to experiment and develop with the DLP650LNIR, DLP7000, DLP9500, DLP7000UV, DLP9500UV, DLPC410, DLPR410 and DLPA200 chips.

This platform targets applications needing:

- Fast binary pattern refresh rates up to 32 kHz
- High speed data rates up to 48Gbps
- Ultraviolet (UV) imaging from 363 nm to 420 nm
- Near infrared (NIR) imaging from 850 nm to 2000 nm
- Visible imaging from 400 nm to 700 nm
- Resolutions up to 1080p (approximately 2.1 megapixels)

Table of Contents

List of Figures

List of Tables

Trademarks

ActiveX™ is a trademark of ACTIVE NETWORK, LLC.

All trademarks are the property of their respective owners.

1 Introduction

This guide explains the hardware and software features of the DLP Discovery 4100 Development Platform evaluation modules (EVMs). The EVM architectures and connectors are described along with a quick start guide on how to operate the D4100 Platform using a PC based Graphical User Interface (GUI). Specific DLP chip details and operation can be found in related component documentation.

1.1 Welcome

The DLP Discovery 4100 Development Platform is a great way to evaluate the fastest binary pattern and data rates the DLP chip portfolio offers. Designers get pixel accurate control of all DMD micromirrors with Global, Quad, Dual and Single Block Modes available for tailoring DMD micromirror pattern timing for continuous (lamp) or solid state (switched) illuminated applications. The D4100 is also a path for customers to design with the high performance UV and NIR DLP chips for systems such as:

- Lithography
- 3D printing and additive manufacturing
- Dynamic grayscale marking and coding
- Industrial printing
- Structured light such as:
  - Factory automation and 3D machine vision
  - 3D In-line automated optical inspection (AOI)
  - Robotic vision
  - Offline 3D metrology
  - 3D scanners
  - 3D identification and biometrics
- Medical and life sciences
- High speed imaging and display

WARNING

Hot Surfaces on the D4100 Controller Board near U11 and U5.

2 Overview

DLP Discovery 4100 is a group of six evaluation modules which, when paired together, create a highly flexible platform to learn, experiment and develop with DLP technology. At the heart of the platform is the DLPLCRC410EVM controller board. The DLPLCRC410EVM board includes the DLPC410, DLPR410, DLPA200, digital receiver, flash, power management circuits, and supporting digital logic. To give designers scalability to port their DLP design work across multiple DMD devices, the DLPLCRC410EVM operates with any of the following five DMD EVMs:

- DLPLCR65NEVM: includes DLP650LNIR DMD board, DLP650LNIR DMD, and one flex cable
- DLPLCR70EVM: includes the DLP7000 DMD board, DLP7000 DMD, and one flex cable
- DLPLCR70UVEVM: includes the DLP7000UV DMD board, DLP7000UV DMD, and one flex cable
- DLPLCR95EVM: includes the DLP9500 DMD board, DLP9500 DMD, and two flex cables
- DLPLCR95UVEVM: includes the DLP9500UV DMD board, DLP9500UV DMD, and two flex cables

When the DLPLCRC410EVM is connected to any of the DMD EVMs, the DLPC410, Applications FPGA, and Software GUI recognizes and provides the proper signals and timing to the attached DMD. Out of the box, the DLPLCRC410EVM delivers a small set of scrolling test patterns which allow customers to evaluate their optical designs for related optical performance. When desired, these scrolling test patterns can be stopped keeping a selected pattern constant. If these patterns are not sufficient, the PC-based software GUI can be used. The GUI program allows binary pattern data to be downloaded via USB to the on-board Applications FPGA (APPSFPGA). The Applications FPGA sends the data to the DLPC410 which then displays the image or pattern on the DMD.

The Xilinx Virtex 5 (LX50) APPSFPGA provides a user programmable platform for developing custom applications. The APPSFPGA is connected to EXP Expansion Connectors for custom interfaces. An onboard USB interface provides a convenient interface for development. Connections for DDR2 SODIMM memory and SPI Flash Memory to the Application FPGA are also included. A Cypress CY7C68013A USB controller is included for customer USB control applications. The source code for the APPSFPGA is provided on TI.COM to provide VHDL savvy customers a reference to leverage for their own development.

Users of the D4100 have the ability to work with visible, UV and NIR light with pixel-level precision and fast pattern rates. The D4100 offers developers a flexible platform to design products to fit many applications using the proven reliability of DLP technology. As previously mentioned, the five DMD-based EVMs enable five distinct DMD options: two in the visible spectrum, two in the UV spectrum, and one in the NIR spectrum. The EVMs, DMDs, and select performance data are shown in Table 2-1:

Table 2-1. D4100 Platform EVMs and DMD Types

EVM	DMD PRODUCT FOLDER	DMD COLUMNS	DMD ROWS	RESET MAX BINARY PATTERN RATE (Hz)		DATA BUS WIDTH
				GLOBAL RESET	PHASED RESET	
DLPLCR95EVM	DLP9500 0.95 1080p	1920	1080	17,636	23,148	64
DLPLCR95UVEVM	DLP9500UV 0.95 UV 1080p					
DLPLCR70EVM	DLP7000 0.7 XGA	1024	768	22,614	32,552	32
DLPLCR70UVEVM	DLP7000UV 0.7 UV XGA					
DLPLCR65NEVM	DLP650LNIR .65 NIR WXGA	1280	800	10,800	12,500	16

The D4100 Platform combines the high performance D4100 chip set with a user programmable Application FPGA (APPSFPGA).

The Xilinx Virtex 5 (LX50) APPSFPGA provides a user programmable platform for developing custom applications. The APPSFPGA is connected to EXP Expansion Connectors for custom interfaces. An onboard USB interface provides a convenient interface for rapid prototyping. Connections for DDR2 SO-DIMM memory and SPI Flash Memory to the Application FPGA are included for customer use. A Cypress CY7C68013A USB controller is included for customer USB control applications.

This document helps facilitate use of the D4100 Platform and provides a hardware reference design details for DLPLCRC410EVM.

2.1 The DLP Discovery 4100 Development Platform

The DLP Discovery 4100 Development Platform (D4100 Platform) typically refers to the combination of one DLPLCRC410EVM plus one DMD EVM. Together these include:

- 1 ea. DLPLCRC410EVM Controller Board
- 1 ea. DMD board with DMD and DMD mounting mechanics (Type-A DMDs only)
- 1 ea. or 2 ea. flexible PCB cables

Not included in the kit but needed for operation are:

- 1 ea. Power supply: V_{OUT} = 5 V, I_{OUT} = 6 A (required)

Not included, optional and only needed if developing and downloading new APPSFPGA firmware:

- 1 ea. Xilinx DLC9G programming cable.

Figure 2-1 is a simplified block diagram of the D4100 Platform.

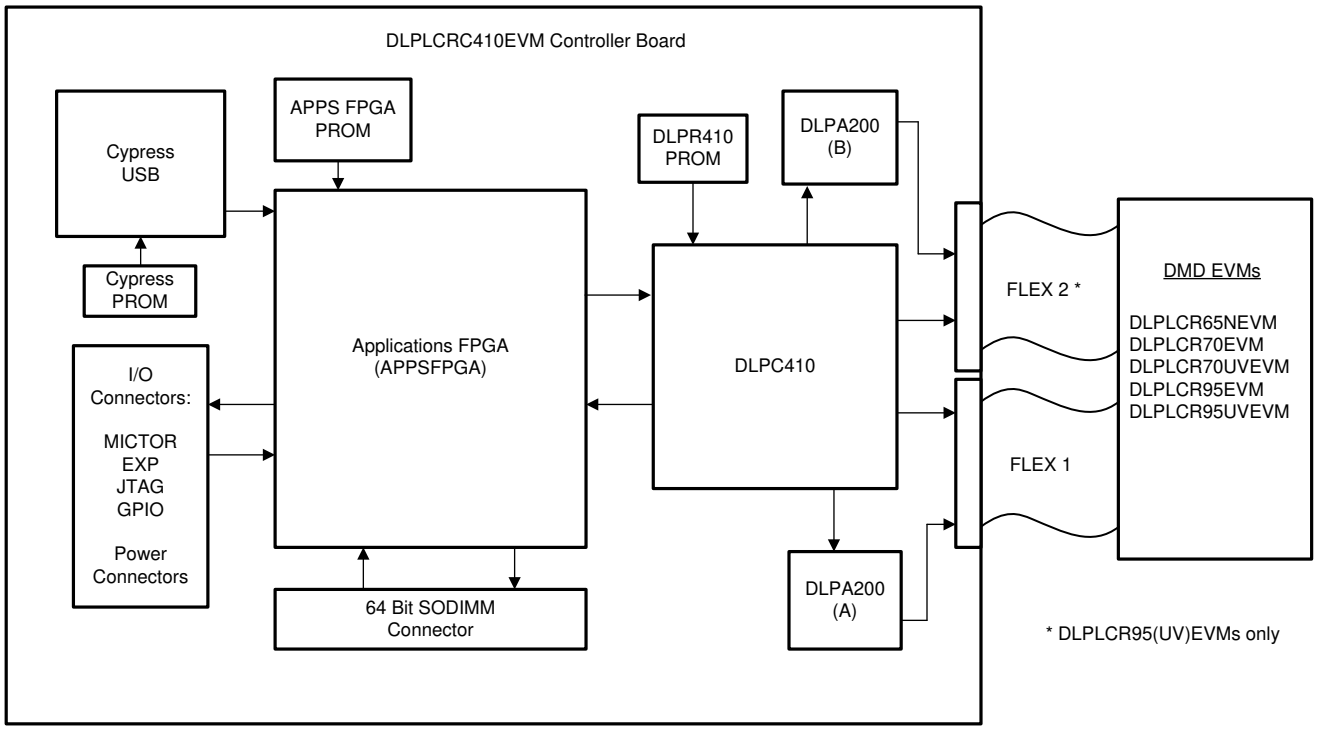

Figure 2-1. D4100 Platform Diagram

The DLP Discovery 4100 EVM Controller Board of the DLPLCRC410EVM contains:

- DLPC410 DLP Digital Controller
  - Provides input high speed 16/32/64 bit 2xLVDS data and control user interface.
  - Provides output data and control interface to the DMD and DLPA200s.
- DLPR410 Configuration PROM
  - Stores and provides configuration data for the DLPC410 controller.
- DLPA200 DMD Micromirror Driver
  - Generates Mirror Clocking Pulses (Resets) for up to 16 DMD Reset Blocks.
  - Supports high reset frequencies.
  - One required for DLP650LNIR, DLP7000, or DLP7000UV DMDs, and two for DLP9500, DLP9500UV DMDs.
- 16/32/64-bit 400 MHz 2xLVDS DLPC410 to DMD Data Interface
  - 16 bits used for the DLP650LNIR DMD.
  - 32 bits used for the DLP7000 and DLP7000UV DMDs.
  - 64 bits used for the DLP9500 and DLP9500UV DMDs.
- 5 Volt input power connector

  - On-board regulation of other power supplies included.
- Applications FPGA (APPSFPGA)
  - Xilinx Virtex 5 (XC5VLX50) FPGA for user application pattern generation and development opportunities.
- APPSFPGA Configuration PROM (XCF16P)
  - Stores and provides configuration data for the APPSFPGA. User programmable for future development.
- A 64-bit DDR2 SODIMM connector
  - For end user development of image storage.
- A Cypress CY7C68013A USB controller
  - Provides USB data and control interface (USB speeds can limit pattern rates).
  - Enabled end user development of USB interface.
- EXP Expansion Connectors
  - Connect to external EXP interface compatible customer boards.
  - Includes additional 2xLVDS pairs to support 64 bit 2xLVDS connection through EXP connectors.
- Flash Memory (connected to APPSFPGA)
  - Non-volatile storage for end user development.
- Various I/O connectors
  - Mictor test connectors for logic analyzer connection.
  - JTAG headers for device programming.
  - GPIO connectors for general purpose digital I/O.

2.2 DLP Discovery 4100 Development Platform Photo

When the DLPLCRC410EVM and the DLPLCR95EVM are assembled together, the combined D4100 Platform is as shown in Figure 2-2. Other DMD EVMs connect to the DLPLCRC410EVM in a similar fashion and look very similar, except the DLPLCRC410EVM only uses a single flex cable (Flex 1) for connection between the Controller Board and the DMD Board.

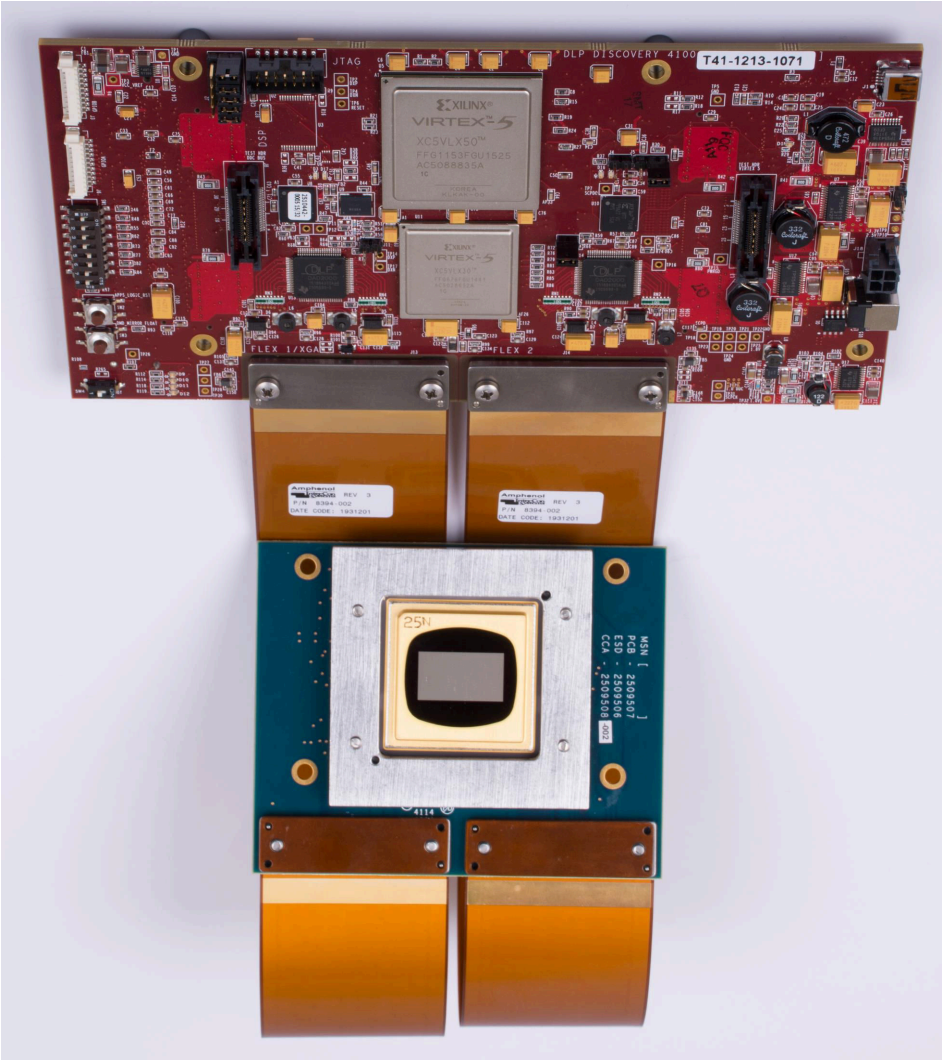

Figure 2-2. DLPLCRC410EVM connected to DLPLCR95EVM

2.3 Key Components

Figure 2-3 shows the D4100 Controller Board key components covered in this section.

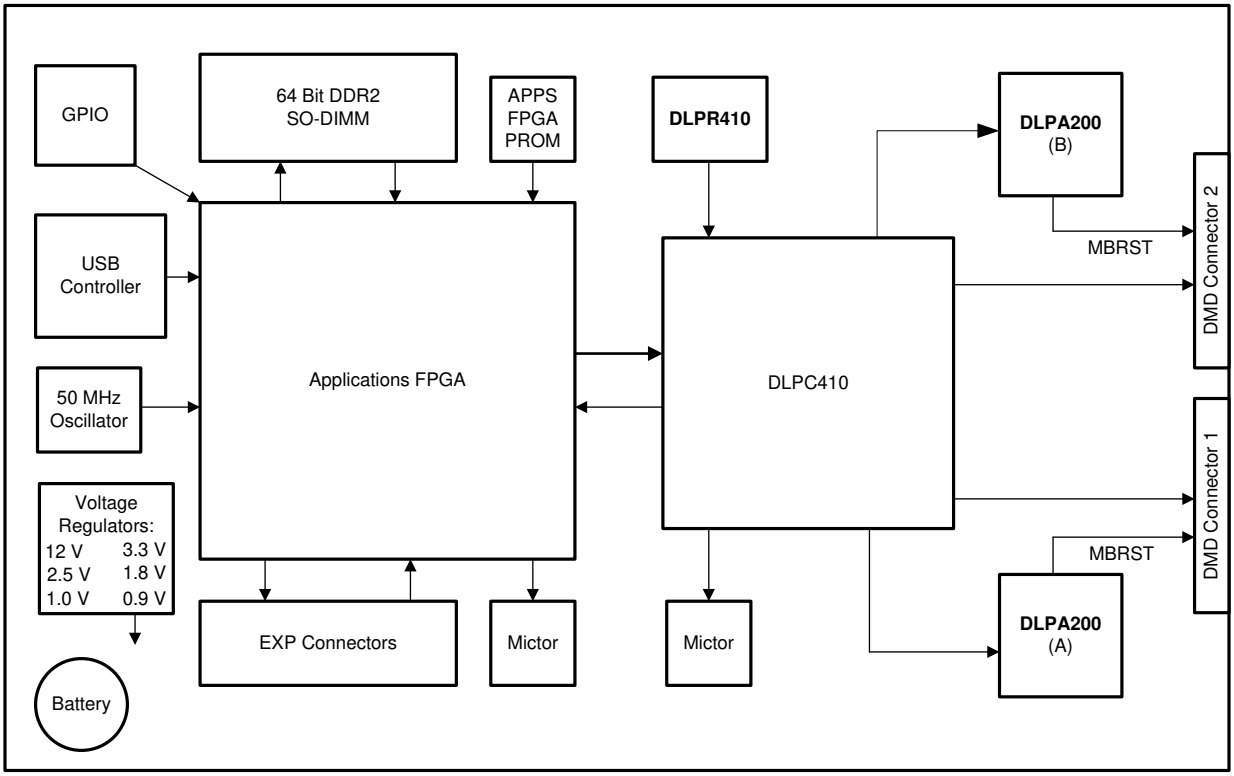

Figure 2-3. DLPLCRC410EVM Controller Board Key Components

2.3.1 Xilinx Virtex 5 APPSFPGA

The APPSFPGA (Xilinx Virtex 5 LX50) is used for development of interface and control solutions for the DMD. The APPSFPGA is connected to a number of I/O connectors, interface controllers, and memory for use in prototyping a custom control solution prior to developing a custom board solution.

2.3.2 DLPC410 - Digital Controller for DLP Discovery 4100 Chipset

The D4100 chipset includes the DLPC410 controller (configured Xilinx Virtex 5 LX30) which exposes a high-speed 2xLVDS data and control interface for DMD control. This interface is connected to the APPSFPGA to support control from the APPSFPGA. The DLPC410 generates DMD and DLPA200 initialization and control signals in response to the inputs on the control interface.

For more information, refer to the DLPC410 data sheet - DLPS024.

2.3.3 DLPA200 - DMD Micromirror Driver

Two DLPA200 reset drivers provide the high voltage power and reset driver functions for the DMD. One DLPA200 is required for the DLP650LNIR, DLP7000, or DLP7000UV DMDs, and two for the DLP9500 or DLP9500UV DMDs. J11 is used to enable/disable the second DLPA200.

For more information on the DLPA200, refer to the DLPA200 data sheet - DLPS015.

2.3.4 DLPR410 - Configuration PROM for DLPC410 Controller

The D4100 chipset includes the DLPR410 controller which configures the DLPC410 (Xilinx Virtex 5 LX30). **The contents of this PROM must not be altered and must not be programmed!**

For more information, refer to the DLPR410 data sheet - DLPS027.

2.3.5 APPSFPGA Flash Configuration PROM

The PROM is used to store and configure the APPSFPGA. The PROM is a Xilinx XCF16P Flash PROM pre-loaded with a test pattern generation capability. The APPSFPGA PROM programming can be changed by customers as needed via a JTAG interface and a Xilinx programming tool. **TI recommends downloading and saving a copy of the pre-loaded test pattern generation program before reprogramming this PROM.**

2.3.6 DMD Connectors

Two DMD Land Grid Array type connectors provide connections for two DMD flex cable. Connect a flex cable at both J13 and J14 locations for connection to a DLPLCR95EVM or DLPLCR95UVEVM. Otherwise, connect only one flex cable to J13 for connections to the DLPLCR70EVM, DLPLCR70UVEMV, and DLPLCR65NEVM.

2.3.7 USB Controller

A Cypress CY7C68013A USB controller is included for development of USB interface functions.

2.3.8 50-MHz Oscillator

The controller has a fixed 50-MHz, 2.5 Volt oscillator connected to the APPSFPGA for clock generation.

2.3.9 DDR2 SODIMM Connector

A 64-bit DDR2 SODIMM connector provides a high speed memory connection to the APPSFPGA. Memory controller design for the APPSFPGA is not included. For a memory controller reference design, visit www.xilinx.com.

2.3.10 Connectors

2.3.10.1 JTAG Header H1

The H1 JTAG header port provides a programming interface to the APPSFPGA and flash configuration PROM.

2.3.10.2 Mictor Connectors

The Mictor connectors support connection of a logic analyzer to the APPSFPGA and the Cypress CY7C68013A signals for development support.

2.3.10.3 GPIO Connectors

General purpose digital I/O connectors.

2.3.11 Battery

A battery provides power for encryption security in the Virtex 5 FPGA. See Xilinx Virtex 5 data sheet for more detail.

2.3.12 Power Supplies

Onboard voltage regulation is provided for all required power supplies. This section lists controller voltage regulators and their purposes.

2.3.12.1 J14 Power Connector

The J14 power connector is the input power supply connector for the DLPLCRC410EVM controller board. For proper operation, this power connector must be connected to a 5 VDC power supply capable of providing 30 W of input power. This connector must not be used when connecting power through input power connector J14.

2.3.12.2 J14 Power Connector

The J14 power connector is the input power supply connector for the DLPLCRC410EVM controller board. For proper operation, this power connector must be connected to a 5 VDC power supply capable of providing 30 W of input power. This connector must not be used when connecting power through input power connector J14.

2.3.12.3 REG. 0.9 V

This delivers 1 A at 0.9 V as a DDR2 reference voltage supply.

2.3.12.4 REG. 1.0 V

This delivers 3 A at 1.0 V as the Virtex 5 core supply.

2.3.12.5 REG. 1.8 V

This delivers 3 A at 1.8 V for the DDR2 supply and FPGA I/O.

2.3.12.6 REG. 2.5 V

This delivers 6 A at 2.5 V to supply the XCF16P FPGA I/O.

2.3.12.7 REG. 3.3 V

This delivers 3 A at 3.3 V to supply the DMD and USB controller.

2.3.12.8 REG. 12 V

This delivers the 0.5 A at 12 V to supply the DLPA200.

3 Hardware Overview and Setup

3.1 Getting Started

The following steps must be followed in starting board operation using the default APPSFPGA code installed at the factory:

1. Connect the desired DMD EVM to the DLPLCRC410EVM using the provided flex cables. A single flex cable connects J13 to either the DLPLCR70EVM, DLPLCR70UVEVM, or the DLPLCR65NEVM. Two flex cables attached to J13 and J14 are used for the DLPLCR95EVM and DLPLCR95UVEVM.
2. Confirm all SW1 switches are in the OFF position. Confirm all five J2 jumpers are in place. If using a DLPLCR95EVM and DLPLCR95UVEVM confirm J10 is installed.
3. Connect a 5 Volt, 6 Amp power supply to either power input connector J12 or J18 (not both) with the power supply OFF.
4. Turn the power supply ON and then slide SW4 to ON. D2 and D3 briefly illuminates to indicate the APPSFPGA and DLPC410 Controller are being configured. Once configuration is complete, D2 and D3 turns off and D16 and D17 illuminates green. D9 flashes green at 1 Hz. D10 displays green. From this point, the DMD repeatedly cycles through several test patterns.

To stop operation:

1. TI **highly recommends** to float the DMD mirrors to set the mirrors to a flat state before powering off. Press SW3 to float the DMD.
2. Turn power OFF.

3.2 User Connectors and I/O

This section describes the use of each DLPLCRC410EVM Controller Board external connector and provides pin out information. Figure 3-1 and Figure 3-2 show connector locations on the D4100 controller board.

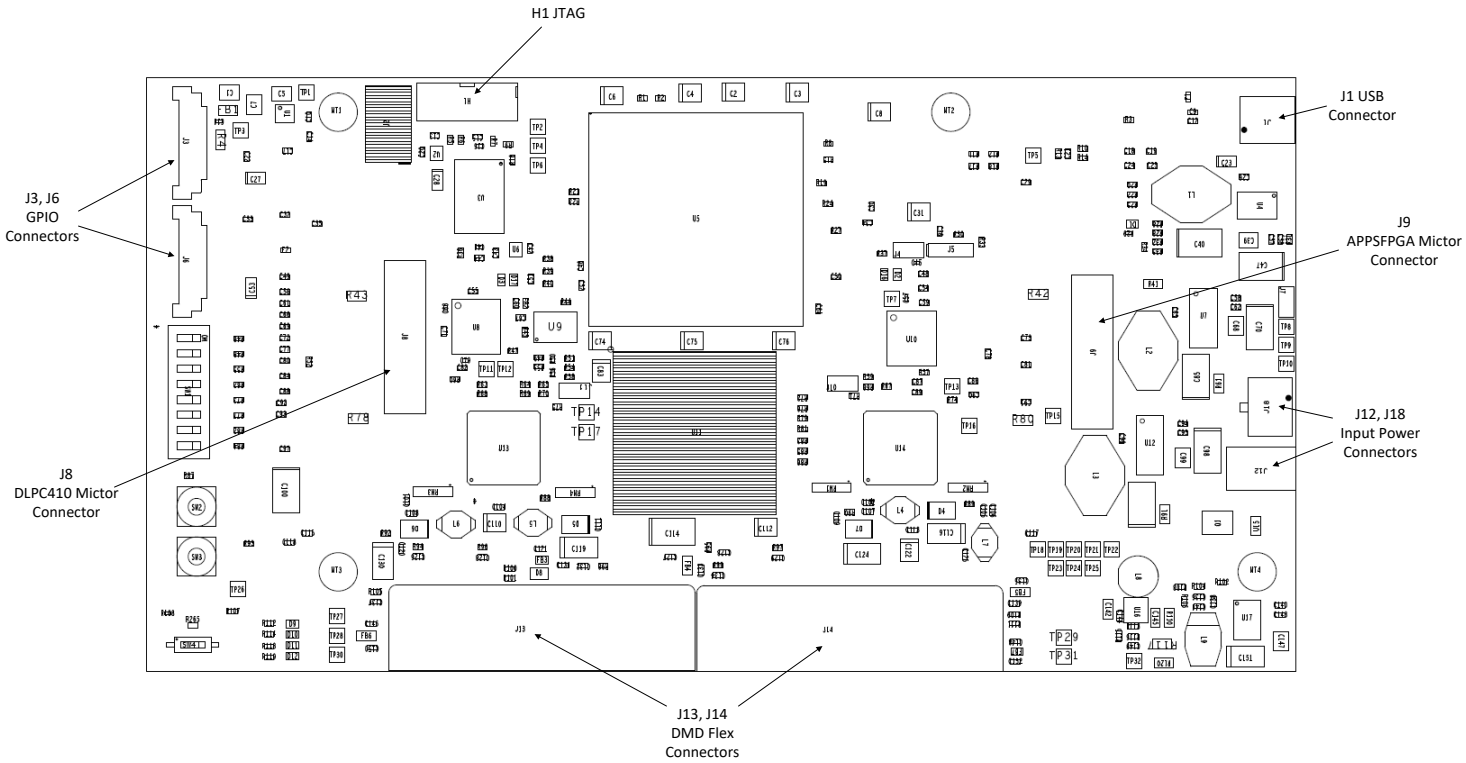

Figure 3-1. DLPLCRC410EVM Controller Connectors (Top View)

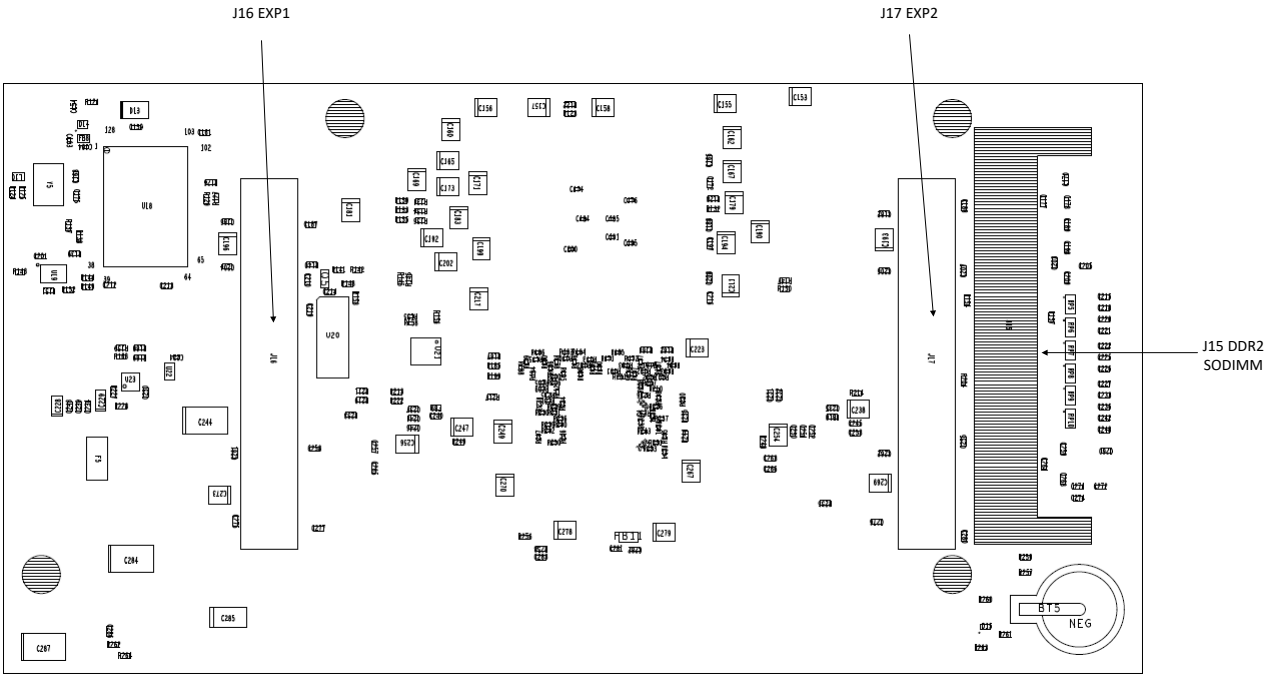

Figure 3-2. DLPLCRC410EVM Controller Connectors (Bottom View)

3.2.1 J12 Input Power Connector

Connector J12 accepts +5 VDC input power for the D4100 Platform. Do not use connectors J12 and J18 concurrently.

J12 is a DC Power Jack connector manufactured by CUI Inc., part number PJ-047BH, or equivalent.

Table 3-1. J12 Input Power Pinout

Pin Number	Pin Name	Description
1	+5V_IN	+5 VDC input, 30W maximum. Pin 1 is center and is 2.5 mm ID and 5.5 mm OD.
2	GND	Pins 2 and 3 are tied together to Ground
3	GND	Pins 2 and 3 are tied together to Ground

3.2.2 J18 Input Power Connector

Connector J18 accepts +5 VDC input power for the D4100 Platform. Do not use connectors J18 and J12 concurrently.

J18 is a Molex connector, part number 043045-0412 or equivalent.

Table 3-2. J18 Input Power Pinout

Pin Number	Pin Name	Description
1	GND	Ground
2	GND	Ground
3	+5V_IN	+5 VDC input, 30W maximum.
4	+5V_IN	+5 VDC input, 30W maximum.

3.2.3 J1 USB Connector Pinout

Connector J1 provides USB input to the controller board.

Table 3-3. J1 USB Pinout

Pin Number	Pin Name	Pin Number	Pin Name
1	USB_5V	2	D–
3	D+	4	NC
5	GND		

3.2.4 J3 USB GPIO

Connector J3 provides eight general purpose USB I/O pin connections to the Cypress USB Controller. For more information, see the Cypress CY7C68013A data sheet at www.cypress.com.

Table 3-4. J3 USB GPIO

Pin Number	Pin Name	Pin Number	Pin Name
1	3.3 V	6	USB_GPIO B3
2	USB_GPIO B7	7	USB_GPIO B2
3	USB_GPIO B6	8	USB_GPIO B1
4	USB_GPIO B5	9	USB_GPIO B0
5	USB_GPIO B4	10	GND

3.2.5 J6 GPIO_A Connector

Connector J6 provides eight general purpose I/O pins to the APPSFPGA.

Table 3-5. J6 GPIO_A Connector

Pin Number	Pin Name	APPSFPGA Pin Number	Pin Number	Pin Name	APPSFPGA Pin Number
1	2.5 V	NC	6	GPIO_A3	AG16
2	GPIO_A7	AF20	7	GPIO_A2	AG17
3	GPIO_A6	AF19	8	GPIO_A1	AH19
4	GPIO_A5	AG12	9	GPIO_A0	AG20
5	GPIO_A4	AH12	10	GND	NC

3.2.6 J8 DLPC410 Mictor Connector

J8 provides connection to the DLPC410 for a logic analyzer. This connector must not be used for normal development or operation.

Table 3-6. J8 DLPC410 Mictor Connector

J8 Pin Number	Pin Name	DLPC410 Pin Number	J8 Pin Number	Pin Name	DLPC410 Pin Number
1	NC	NC	2	ECP2_M_TP0	AD9
3	GND	NC	4	ECP2_M_TP1	AA11
5	DDCSPARE0	L7	6	ECP2_M_TP2	W11
7	DDCSPARE1	AC13	8	ECP2_M_TP3	AB26
9	NC	NC	10	ECP2_M_TP4	AB9
11	NC	NC	12	ECP2_M_TP5	AB11
13	ECP2_M_TP31	AA13	14	ECP2_M_TP6	AA10
15	ECP2_M_TP3O	AB13	16	ECP2_M_TP7	AA12
17	ECP2_M_TP29	AD14	18	ECP2_M_TP8	Y11
19	ECP2_M_TP28	L5	20	ECP2_M_TP9	AB17
21	ECP2_M_TP27	AC14	22	ECP2_M_TP10	AA17
23	ECP2_M_TP26	AB15	24	ECP2_M_TP11	AA15
25	ECP2_M_TP25	H19	26	ECP2_M_TP12	AF12
27	ECP2_M_TP24	J18	28	ECP2_M_TP13	AE11
29	ECP2_M_TP23	H18	30	ECP2_M_TP14	AC9
31	ECP2_M_TP22	G15	32	ECP2_M_TP15	AF11
33	ECP2_M_TP21	G14	34	ECP2_M_TP16	AB12
35	ECP2_M_TP20	H17	36	ECP2_M_TP17	AA16
37	ECP2_M_TP19	G20	38	ECP2_M_TP18	AD13

3.2.7 J9 USB/APPSFPGA Mictor Connector

J9 is the Mictor connector for the USB controller and APPSFPGA. Signals from the USB or APPSFPGA are routed to the connector as selected by jumper J6. Refer to the D4100 controller board schematic (DLPC410 Board Design Files) for more information. Signals can be routed to the connector by HDL code and monitored with a logic analyzer to support development.

Table 3-7. J9 USB/APPSFPGA Mictor Connector

J9 Pin Number	Pin Name	APPSFPGA Pin Number	J9 Pin Number	Pin Name	APPSFPGA Pin Number
1	NC	NC	2	NC	NC
3	GND	NC	4	D4100_I2C_CLK	P29
5	USB_IF_CLK/ TEST_CLK_0	N29	6	D4100_I2C_DATA	U28
7	USB_FDO/ TST_HDR_BY0_0	H29	8	GPIFADR0/ TST_HDR_BY2_0	K31
9	USB_FD1/ TST_HDR_BY0_1	H30	10	GPIFADR1/ TST_HDR_BY2_1	L31
11	USB_FD2/ TST_HDR_BY0_2	J31	12	GPIFADR2/ TST_HDR_BY2_2	P31
13	USB_FD3/ TST_HDR_BY0_3	G30	14	GPIFADR3/ TST_HDR_BY2_3	P30
15	USB_FD4/ TST_HDR_BY0_4	J30	16	GPIFADR4/ TST_HDR_BY2_4	N30
17	USB_FD5/ TST_HDR_BY0_5	G31	18	GPIFADR5/ TST_HDR_BY2_5	M31
19	USB_FD6/ TST_HDR_BY0_6	J29	20	GPIFADR6/ TST_HDR_BY2_6	R28
21	USB_FD7/ TST_HDR_BY0_7	F29	22	GPIFADR7/ TST_HDR_BY2_7	R29
23	USB_FD8/ TST_HDR_BY1_0	K29	24	GPIFADR8/ TST_HDR_BY3_0	T31
25	USB_FD9/ TST_HDR_BY1_1	F30	26	USB_CTRL0/ TST_HDR_BY3_1	R31
27	USB_FD1O/ TST_HDR_BY1_2	L30	28	USB_CTRL1/ TST_HDR_BY3_2	U30
29	USB_FD11/ TST_HDR_BY1_3	F31	30	USB_CTRL2/ TST_HDR_BY3_3	T30
31	USB_FD12/ TST_HDR_BY1_4	L29	32	USB_CTRL3/ TST_HDR_BY3_4	T28
33	USB_FD13/ TST_HDR_BY1_5	E29	34	USB_FPGA_RESET/ TST_HDR_BY3_5	T29
35	USB_FD14/ TST_HDR_BY1_6	E31	36	USB_INT5/ TST_HDR_BY3_6	U27
37	USB_FD15/ TST_HDR_BY1_7	M30	38	NC	NC

3.2.8 J13 DMD Flex 1 Connector

Connector J13 provides control and data signals to the DMD Flex 1 connector. This connector is used for connection to all DMD types.

Table 3-8. J13 DMD Flex Connector 1

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1A	GND	1B	3.3 V	1C	3.3 V
2C	GND	2A	DDC_DOUT_A13_DPP	2B	DDC_DOUT_A13_DPN
3A	GND	3B	DDC_DOUT_A11_DPP	3C	DDC_DOUT_A11_DPN
4C	GND	4A	DDC_DOUT_A9_DPP	4B	DDC_DOUT_A9_DPN
5A	GND	5B	DDC_DCLKOUT_A_DPP	5C	DDC_DCLKOUT_A_DPN
6C	GND	6A	DDC_DOUT_A7_DPP	6B	DDC_DOUT_A7_DPP
7A	GND	7B	DDC_DOUT_A5_DPP	7C	DDC_DOUT_A5_DPN
8C	GND	8A	DDC_DOUT_A3_DPP	8B	DDC_DOUT_A3_DPN
9A	GND	9B	DDC_DOUT_A1_DPP	9C	DDC_DOUT_A1_DPN
10C	GND	10A	DAD_A_SCPDO	10B	DAD_A_SCPCLK
11A	GND	11B	DMDSPARE1	11C	DMD_A_SCPEN
12C	GND	12A	MBRST1_15	12B	MBRST1_14
13A	GND	13B	DMD_VCC2	13C	DMD_VCC2
14C	GND	14A	MBRST1_10	14B	MBRST1_6
15A	GND	15B	MBRST1_9	15C	MBRST1_7
16C	GND	16A	MBRST1_13	16B	MBRST1_12
17A	GND	17B	DDC_DOUT_B1_DPP	17C	DDC_DOUT_B1_DPN
18C	GND	18A	DDC_DOUT_B3_DPP	18B	DDC_DOUT_B3_DPN
19A	GND	19B	DDC_DOUT_B5_DPP	19C	DDC_DOUT_B5_DPN
20C	GND	20A	DDC_DOUT_B7_DPP	20B	DDC_DOUT_B7_DPN
21A	GND	21B	DDC_DCLKOUT_B_DPP	21C	DDC_DCLKOUT_B_DPN
22C	GND	22A	DDC_DOUT_B9_DPP	22B	DDC_DOUT_B9_DPN
23A	GND	23B	DDC_DOUT_B11_DPP	23C	DDC_DOUT_B11_DPN
24C	GND	24A	DDC_DOUT_B13_DPP	24B	DDC_DOUT_B13_DPN
25A	GND	25B	DDC_DOUT_B15_DPP	25C	DDC_DOUT_B15_DPN
1D	GND	1E	DDC_DOUT_A15_DPP	1F	DDC_DOUT_A15_DPN
2F	GND	2D	DDC_DOUT_A14_DPP	2E	DDC_DOUT_A14_DPN
3D	GND	3E	DDC_DOUT_A12_DPP	3F	DDC_DOUT_A12_DPN
4F	GND	4D	DDC_DOUT_A10_DPP	4E	DDC_DOUT_A10_DPN
5D	GND	5E	DDC_DOUT_A8_DPP	5F	DDC_DOUT_A8_DPN
6F	GND	6D	DDC_SCTRL_A_DPP	6E	DDC_SCTRL_A_DPN
7D	GND	7E	DDC_DOUT_A6_DPP	7F	DDC_DOUT_A6_DPN
8F	GND	8D	DDC_DOUT_A4_DPP	8E	DDC_DOUT_A4_DPN
9D	GND	9E	DDC_DOUT_A2_DPP	9F	DDC_DOUT_A2_DPN
10F	GND	10D	DDC_DOUT_A0_DPP	10E	DDC_DOUT_A0_DPN
11D	GND	11E	SCPDI	11F	DMD_A_RESET
12F	GND	12D	DMDSPARE0	12E	MBRST1_11
13D	GND	13E	MBRST1_5	13F	MBRST1_4
14F	GND	14D	MBRST1_0	14E	MBRST1_3
15D	GND	15E	MBRST1_2	15F	MBRST1_8
16F	GND	16D	DDC_DOUT_B0_DPP	16E	DDC_DOUT_B0_DPN
17D	GND	17E	DDC_DOUT_B2_DPP	17F	DDC_DOUT_B2_DPN
18F	GND	18D	DDC_DOUT_B4_DPP	18E	DDC_DOUT_B4_DPN

Table 3-8. J13 DMD Flex Connector 1 (continued)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
19D	GND	19E	DDC_DOUT_B6_DPP	19F	DDC_DOUT_B6_DPN
20F	GND	20D	DDC_SCTRL_B_DPP	20E	DDC_SCTRL_B_DPP
21D	GND	21E	DDC_DOUT_B8_DPP	21F	DDC_DOUT_B8_DPN
22F	GND	22D	DDC_DOUT_B10_DPP	22E	DDC_DOUT_B10_DPN
23D	GND	23E	DDC_DOUT_B12_DPP	23F	DDC_DOUT_B12_DPN
24F	GND	24D	DDC_DOUT_B14_DPP	24E	DDC_DOUT_B14_DPN
25D	GND	25E	3.3 V	25F	3.3 V

3.2.9 J14 DMD Flex 2 Connector

Connector J14 provides control and data signals to the DMD Flex 2 connector. This connector is only used for connection to DLP9500 and DLP9500UV DMDs.

Table 3-9. J14 DMD Flex Connector 2

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1A	GND	1B	3.3 V	1C	3.3 V
2C	GND	2A	DDC_DOUT_C13_DPP	2B	DDC_DOUT_C13_DPN
3A	GND	3B	DDC_DOUT_C11_DPP	3C	DDC_DOUT_C11_DPN
4C	GND	4A	DDC_DOUT_C9_DPP	4B	DDC_DOUT_C9_DPN
5A	GND	5B	DDC_DCLKOUT_C_DPP	5C	DDC_DCLKOUT_C_DPN
6C	GND	6A	DDC_DOUT_C7_DPP	6B	DDC_DOUT_C7_DPP
7A	GND	7B	DDC_DOUT_C5_DPP	7C	DDC_DOUT_C5_DPN
8C	GND	8A	DDC_DOUT_C3_DPP	8B	DDC_DOUT_C3_DPN
9A	GND	9B	DDC_DOUT_C1_DPP	9C	DDC_DOUT_C1_DPN
10C	GND	10A	DAD_B_SCPDO	10B	DAD_B_SCPCLK
11A	GND	11B	DMDSPARE2	11C	DMD_B_SCPEN
12C	GND	12A	MBRST2_15	12B	MBRST2_14
13A	GND	13B	DMD_VCC2	13C	DMD_VCC2
14C	GND	14A	MBRST2_10	14B	MBRST2_6
15A	GND	15B	MBRST2_9	15C	MBRST2_7
16C	GND	16A	MBRST2_13	16B	MBRST2_12
17A	GND	17B	DDC_DOUT_D1_DPP	17C	DDC_DOUT_D1_DPN
18C	GND	18A	DDC_DOUT_D3_DPP	18B	DDC_DOUT_D3_DPN
19A	GND	19B	DDC_DOUT_D5_DPP	19C	DDC_DOUT_D5_DPN
20C	GND	20A	DDC_DOUT_D7_DPP	20B	DDC_DOUT_D7_DPN
21A	GND	21B	DDC_DCLKOUT_D_DPP	21C	DDC_DCLKOUT_D_DPN
22C	GND	22A	DDC_DOUT_D9_DPP	22B	DDC_DOUT_D9_DPN
23A	GND	23B	DDC_DOUT_D11_DPP	23C	DDC_DOUT_D11_DPN
24C	GND	24A	DDC_DOUT_D13_DPP	24B	DDC_DOUT_D13_DPN
25A	GND	25B	DDC_DOUT_D15_DPP	25C	DDC_DOUT_D15_DPN
1D	GND	1E	DDC_DOUT_C15_DPP	1F	DDC_DOUT_C15_DPN
2F	GND	2D	DDC_DOUT_C14_DPP	2E	DDC_DOUT_C14_DPN
3D	GND	3E	DDC_DOUT_C12_DPP	3F	DDC_DOUT_C12_DPN
4F	GND	4D	DDC_DOUT_C10_DPP	4E	DDC_DOUT_C10_DPN
5D	GND	5E	DDC_DOUT_C8_DPP	5F	DDC_DOUT_C8_DPN
6F	GND	6D	DDC_SCTRL_C_DPP	6E	DDC_SCTRL_C_DPN
7D	GND	7E	DDC_DOUT_C6_DPP	7F	DDC_DOUT_C6_DPN
8F	GND	8D	DDC_DOUT_C4_DPP	8E	DDC_DOUT_C4_DPN
9D	GND	9E	DDC_DOUT_C2_DPP	9F	DDC_DOUT_C2_DPN
10F	GND	10D	DDC_DOUT_C0_DPP	10E	DDC_DOUT_C0_DPN
11D	GND	11E	SCPDI	11F	DMD_B_RESET
12F	GND	12D	DMDSPARE0	12E	MBRST2_11
13D	GND	13E	MBRST2_5	13F	MBRST2_4
14F	GND	14D	MBRST2_0	14E	MBRST2_3
15D	GND	15E	MBRST2_2	15F	MBRST2_8
16F	GND	16D	DDC_DOUT_D0_DPP	16E	DDC_DOUT_D0_DPN
17D	GND	17E	DDC_DOUT_D2_DPP	17F	DDC_DOUT_D2_DPN
18F	GND	18D	DDC_DOUT_D4_DPP	18E	DDC_DOUT_D4_DPN

Table 3-9. J14 DMD Flex Connector 2 (continued)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
19D	GND	19E	DDC_DOUT_D6_DPP	19F	DDC_DOUT_D6_DPN
20F	GND	20D	DDC_SCTRL_D_DPP	20E	DDC_SCTRL_D_DPP
21D	GND	21E	DDC_DOUT_D8_DPP	21F	DDC_DOUT_D8_DPN
22F	GND	22D	DDC_DOUT_D10_DPP	22E	DDC_DOUT_D10_DPN
23D	GND	23E	DDC_DOUT_D12_DPP	23F	DDC_DOUT_D12_DPN
24F	GND	24D	DDC_DOUT_D14_DPP	24E	DDC_DOUT_D14_DPN
25D	GND	25E	3.3 V	25F	3.3 V

3.2.10 J15 DDR2 SODIMM Connector

Connector J15 provides a DDR2 SODIMM memory socket. No memory module is included. Memory controller design for the APPSFPGA is not included. For a memory controller reference design, visit www.xilinx.com.

Table 3-10. J15 DDR2 SODIMM Connector

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	VCC_VREF	2	GND	3	GND	4	DDR2_D4
5	DDR2_D0	6	DDR2_D5	7	DDR2_D1	8	GND
9	GND	10	DDR2_DM0	11	DDR2_DQS0_N	12	GND
13	DDR2_DQS0_P	14	DDR2_D6	15	GND	16	DDR2_D7
17	DDR2_D2	18	GND	19	DDR2_D3	20	DDR2_D12
21	GND	22	DDR2_D13	23	DDR2_D8	24	GND
25	DDR2_D9	26	DDR2_DM1	27	GND	28	GND
29	DDR2_DOS1_N	30	DDR2_CK0_P	31	DDR2_DOS1_P	32	DDR2_CK0_N
33	GND	34	GND	35	DDR2_D10	36	DDR2_D14
37	DDR2_D11	38	DDR2_D15	39	GND	40	GND
41	GND	42	GND	43	DDR2_D16	44	DDR2_D20
45	DDR2_D17	46	DDR2_D21	47	GND	48	GND
49	DDR2_DQS2_N	50	NC	51	DDR2_DQS2_P	52	DDR2_DM2
53	GND	54	GND	55	DDR2_D18	56	DDR2_D22
57	DDR2_D19	58	DDR2_D23	59	GND	60	GND
61	DDR2_D24	62	DDR2_D28	63	DDR2_D25	64	DDR2_D29
65	GND	66	GND	67	DDR2_DM3	68	DDR2_DQS3_N
69	NC	70	DDR2_DQS3_P	71	GND	72	GND
73	DDR2_D26	74	DDR2_D30	75	DDR2_D27	76	DDR2_D31
77	GND	78	GND	79	DDR2_CKE0	80	DDR2_CKE0
81	1.8V	82	1.8V	83	NC	84	NC
85	DDR2_BA2	86	NC	87	1.8V	88	1.8V
89	DDR2_A12	90	DDR2_A11	91	DDR2_A9	92	DDR2_A7
93	DDR2_A8	94	DDR2_A6	95	1.8V	96	1.8V
97	DDR2_A5	98	DDR2_A4	99	DDR2_A3	100	DDR2_A2
101	DDR2_A1	102	DDR2_A0	103	1.8V	104	1.8V
105	DDR2_A10	106	DDR2_BA1	107	DDR2_BA0	108	DDR2_RAS_B
109	DDR2_WE_B	110	DDR2_CS0_B	111	1.8V	112	1.8V
113	DDR2_CAS_B	114	DDR2_ODT0	115	DDR2_CS1_B	116	DDR2_A13
117	1.8V	118	1.8V	119	DDR2_ODT1	120	NC
121	GND	122	GND	123	DDR2_D32	124	DDR2_D36
125	DDR2_D33	126	DDR2_D37	127	GND	128	GND
129	DDR2_DQS4_N	130	DDR2_DDM4	131	DDR2_DQS4_P	132	GND
133	GND	134	DDR2_D38	135	DDR2_D34	136	DDR2_D30
137	DDR2_D35	138	GND	139	GND	140	DDR2_D44
141	DDR2_D40	142	DDR2_D44	143	DDR2_D41	144	GND
145	GND	146	DDR2_DQS5_N	147	DDR2_DM5	148	DDR2_DQS5_P
149	GND	150	GND	151	DDR2_D42	152	DDR2_D46
153	DDR2_D43	154	DDR2_D47	155	GND	156	GND
157	DDR2_D48	158	DDR2_D52	159	DDR2_D49	160	DDR2_D53
161	GND	162	GND	163	NC	164	DDR2_CK1_P
165	GND	166	DDR2_CK1_N	167	DDR2_DQ56_N	168	GND
169	DDR2_DQ56_P	170	DDR2_DM6	171	GND	172	GND

Table 3-10. J15 DDR2 SODIMM Connector (continued)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
173	DDR2_D50	174	DDR2_D54	175	DDR2_D51	176	DDR2_D55
177	GND	178	GND	179	DDR2_D56	180	DDR2_D60
181	DDR2_D57	182	DDR2_D61	183	GND	184	GND
185	DDR2_DM7	186	DDR2_DQS7_N	187	GND	188	DDR2_DQS7_P
189	DDR2_D58	190	GND	191	DDR2_D59	192	DDR2_D62
193	GND	194	DDR2_D63	195	DDR2_SDA	196	GND
197	DDR2_SDL	198	GND	199	1.8 V	200	GND

3.2.11 J16, J17 EXP Connectors

J16 and J17 provide connections to APPSFPGA compatible with the Avnet EXP Bus Specification. J16 and J17 can also be used as high speed interface connectors for accessory boards. The D4100 controller board routes some of the single-ended signals as differential pairs to support a full 64 bit 2xLVDS data bus. This routing can interfere with the EXP single-ended signals as noted in the Table 3-11 and Table 3-13 tablenotes.

Table 3-11. J16 EXP-1 Connector

J16 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number	J16 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number
1	EXP1_SE_IO_1		A33	2	EXP1_SE_IO_0		C34
3	EXP1_SE_IO_3		B32	4	EXP1_SE_IO_2		D32
7	EXP1_SE_IO_5		B33	8	EXP1_SE_IO_4		D34
9	EXP1_SE_IO_7		C32	10	EXP1_SE_IO_6		E34
13	EXP1_SE_IO_9		H32	14	EXP1_SE_IO_8		G32
15	EXP1_SE_IO_11		C33	16	EXP1_SE_IO_10		F33
19	EXP1_SE_IO_13(1)	EXP1_DIFF_23_P	K33	20	EXP1_SE_IO_12(1)	EXP1_DIFF_22	G33
21	EXP1_SE_IO_15(1)	EXP1_DIFF_23_N	K32	22	EXP1_SE_IO_14(1)	EXP1_DIFF_22	F34
25	EXP1_SE_IO_17(1)	EXP1_DIFF_25_P	P34	26	EXP1_SE_IO_16(1)	EXP1_DIFF_24	H34
27	EXP1_SE_IO_19(1)	EXP1_DIFF_25_N	N34	28	EXP1_SE_IO_18(1)	EXP1_DIFF_24	J34
31	EXP1_SE_IO_21(1)	EXP1_DIFF_27_P	N33	32	EXP1_SE_IO_20(1)	EXP1_DIFF_26	L34
33	EXP1_SE_IO_23(1)	EXP1_DIFF_27_N	M33	34	EXP1_SE_IO_22(1)	EXP1_DIFF_26	K34
37	EXP1_SE_IO_25(1)	EXP1_DIFF_29_P	L33	38	EXP1_SE_IO_24(1)	EXP1_DIFF_28	J32
39	EXP1_SE_IO_27(1)	EXP1_DIFF_29_N	M32	40	EXP1_SE_IO_26(1)	EXP1_DIFF_28	H33
41	EXP1_SE_IO_28		E32	42		EXP1_DIFF_CLK_IN_DPP	H19
43	EXP1_SE_CLK_IN		J20	44		EXP1_DIFF_CLK_IN_DPN	H20
47	EXP1_SE_IO_29		E33	48	EXP1_SE_IO_30(1)	EXP1_DIFF_30_P	R33
49	EXP1_SE_CLK_OUT		J21	50	EXP1_SE_IO_3(1)	EXP1_DIFF_30_N	R32
53		EXP1_DIFF_21_P	P32	54		EXP1_DIFF_20_P	AC32
55		EXP1_DIFF_21_N	N32	56		EXP1_DIFF_20_N	AB32
59	EXP1_SE_IO_32(1)	EXP1_DIFF_31_P	T33	60		EXP1_DIFF_18_P	AF34
61	EXP1_SE_IO_33(1)	EXP1_DIFF_31_N	R34	62		EXP1_DIFF_18_N	AE34
65		EXP1_DIFF_19_P	AG32	66		EXP1_DIFF_16_P	U33
67		EXP1_DIFF_19_N	AH32	68		EXP1_DIFF_16_N	T34

Table 3-11. J16 EXP-1 Connector (continued)

J16 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number	J16 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number
71		EXP1_DIFF_17_P	AJ32	72		EXP1_DIFF_CLK_OUT_P	U3
73		EXP1_DIFF_17_N	AK32	74		EXP1_DIFF_CLK_OUT_N	U2
77		EXP1_DIFF_15_P	W34	78		EXP1_DIFF_14_P	V33
79		EXP1_DIFF_15_N	V34	80		EXP1_DIFF_14_N	V32
81		EXP1_DIFF_13_P	AA34	82		EXP1_DIFF_12_P	AD32
83		EXP1_DIFF_13_N	Y34	84		EXP1_DIFF_12_N	AE32
87		EXP1_DIFF_11_P	Y32	88		EXP1_DIFF_10_P	AL34
89		EXP1_DIFF_11_N	W32	90		EXP1_DIFF_10_N	AL33
93		EXP1_DIFF_9_P	AA33	94		EXP1_DIFF_8_P	AK34
95		EXP1_DIFF_9_N	Y33	96		EXP1_DIFF_8_N	AK33
99		EXP1_DIFF_7_P	AC33	100		EXP1_DIFF_6_P	AF33
101		EXP1_DIFF_7_N	AB33	102		EXP1_DIFF_6_N	AE33
105		EXP1_DIFF_5_P	AC34	106		EXP1_DIFF_4_P	AH34
107		EXP1_DIFF_5_N	AD34	108		EXP1_DIFF_4_N	AJ34
111		EXP1_DIFF_3_P	AM33	112		EXP1_DIFF_2_P	AG33
113		EXP1_DIFF_3_N	AM32	114		EXP1_DIFF_2_N	AH33
117		EXP1_DIFF_1_P	AN34	118		EXP1_DIFF_0_P	AN32
119		EXP1_DIFF_1_N	AN33	120		EXP1_DIFF_0_N	AP32

(1) Single ended /IO with shared differential pairs; must only be slow switching signals or only one side of the pair be used.

Table 3-12. J16 EXP-1 Power and Ground Connections

J16 Pin Number	Power Connection
5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36	VCC_2P5V
45, 46, 41, 52, 57, 58, 63, 64, 69, 70, 75, 76, 121, 122, 124, 125, 126, 127, 128, 129, 130, 131, 132	Ground
85, 86, 91, 92, 97, 98, 103, 104, 109, 110, 115, 116	VCC_3P3V

Table 3-13. J17 EXP-2 Connector

J17 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number	J17 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number
1	EXP2_SE_IO_1		D1	2	EXP2_SE_IO_0		B3
3	EXP2_SE_IO_3		D2	4	EXP2_SE_IO_2		B1
7	EXP2_SE_IO_5		J2	8	EXP2_SE_IO_4		B2
9	EXP2_SE_IO_7		J1	10	EXP2_SE_IO_6		A3
13	EXP9_SE_IO_9		K1	14	EXP2_SE_IO_8		C2
15	EXP2_SE_IO_11		K2	16	EXP2_SE_IO_10		C3
19	EXP2_SE_IO_13(1)	EXP2_DIFF_23_P	H2	20	EXP2_SE_IO_12(1)	EXP2_DIFF_22	E2
21	EXP2_SE_IO_15(1)	EXP2_DIFF_23_N	H3	22	EXP2_SE_IO_14(1)	EXP2_DIFF_22	E1
25	EXP2_SE_IO_17(1)	EXP2_DIFF_25_P	P2	26	EXP2_SE_IO_16(1)	EXP2_DIFF_24	E3
27	EXP2_SE_IO_19(1)	EXP2_DIFF_25_N	R3	28	EXP2_SE_IO_18(1)	EXP2_DIFF_24	F3
31	EXP2_SE_IO_21(1)	EXP2_DIFF_27_P	T1	32	EXP2_SE_IO_20(1)	EXP2_DIFF_26	F1
33	EXP2_SE_IO_23(1)	EXP2_DIFF_27_N	R1	34	EXP2_SE_IO_22(1)	EXP2_DIFF_26	G1
37	EXP2_SE_IO_25(1)	EXP2_DIFF_29_P	K3	38	EXP2_SE_IO_24(1)	EXP2_DIFF_28	G3
39	EXP2_SE_IO_27(1)	EXP2_DIFF_29_N	L3	40	EXP2_SE_IO_26(1)	EXP2_DIFF_28	G2
41	EXP2_SE_IO_28		Y2	42		EXP2_DIFF_CLK_IN_DPP	H18
43	EXP2_SE_CLK_IN		J16	44		EXP2_DIFF_CLK_IN_DPN	J17
47	EXP2_SE_IO_29		Y3	48	EXP2_SE_IO_30(1)	EXP2_DIFF_30_P	N2
49	EXP2_SE_CLK_OUT		J15	50	EXP2_SE_IO_31	EXP2_DIFF_30_N	M2
53		EXP2_DIFF_21_P	M3	54		EXP2_DIFF_20_P	M1
55		EXP2_DIFF_21_N	N3	56		EXP2_DIFF_20_N	L1
59	EXP2_SE_IO_32(1)	EXP2_DIFF_31_P	P1	60		EXP2_DIFF_18_P	V4
61	EXP2_SE_IO_33(1)	EXP2_DIFF_31_N	R2	62		EXP2_DIFF_18_N	V3
65		EXP2_DIFF_19_P	U3	66		EXP2_DIFF_16_P	W1
67		EXP2_DIFF_19_N	T3	68		EXP2_DIFF_16_N	V2
71		EXP2_DIFF_17_P	U1	72		EXP2_DIFF_CLK_OUT_P	AC3
73		EXP2_DIFF_17_N	U2	74		EXP2_DIFF_CLK_OUT_N	AB2
77		EXP2_DIFF_15_P	W2	78		EXP2_DIFF_14_P	AB3
79		EXP2_DIFF_15_N	Y1	80		EXP2_DIFF_14_N	AA3
81		EXP2_DIFF_13_P	AF1	82		EXP2_DIFF_12_P	AG1
83		EXP2_DIFF_13_N	AE1	84		EXP2_DIFF_12_N	AG2
87		EXP2_DIFF_11_P	AF3	88		EXP2_DIFF_10_P	AE2
89		EXP2_DIFF_11_N	AE3	90		EXP2_DIFF_10_N	AD2
93		EXP2_DIFF_9_P	AH2	94		EXP2_DIFF_8_P	AB1
95		EXP2_DIFF_9_N	AJ2	96		EXP2_DIFF_8_N	AA1
99		EXP2_DIFF_7_P	AK2	100		EXP2_DIFF_6_P	AG3
101		EXP2_DIFF_7_N	AK3	102		EXP2_DIFF_6_N	AH3
105		EXP2_DIFF_5_P	AJ1	106		EXP2_DIFF_4_P	AC2
107		EXP2_DIFF_5_N	AK1	108		EXP2_DIFF_4_N	AD1
111		EXP2_DIFF_3_P	AM3	112		EXP2_DIFF_2_P	AN2
113		EXP2_DIFF_3_N	AN3	114		EXP2_DIFF_2_N	AP2
117		EXP2_DIFF_1_P	AL1	118		EXP2_DIFF_0_P	AM2

Table 3-13. J17 EXP-2 Connector (continued)

J17 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number	J17 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number
119		EXP2_DIFF_1_N	AM1	120		EXP2_DIFF_0_N	AL3

(1) Single ended /IO with shared differential pairs; must only be slow switching signals or only one side of the pair be used.

Table 3-14. J17 EXP-2 Power and Ground Connections

J17 Pin Number	Power Connection
5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36	VCC_2P5V
45, 46, 41, 52, 57, 58, 63, 64, 69, 70, 75, 76, 121, 122, 124, 125, 126, 127, 128, 129, 130, 131 ,132	Ground
85, 86, 91, 92, 97, 98, 103, 104, 109, 110, 115, 116	VCC_3P3V

3.2.12 H1 Xilinx FPGA JTAG Header

Provides direct connection for a Xilinx JTAG programming cable. Xilinx Model DLC9G is recommended. Visit www.xilinx.com for more information.

Table 3-15. H1 Xilinx APPSFPGA JTAG Header

H1 Pin Number	Pin Name
1, 3, 5, 7, 9, 11, 13	GND
2	P2P5V
4	TMS
6	TCK
8	TDO
10	TDI
12, 14	NC

3.3 Configuration Jumpers

This section describes the D4100 Controller Board configuration jumpers. Figure 3-3 shows jumper locations on the D4100 controller board.

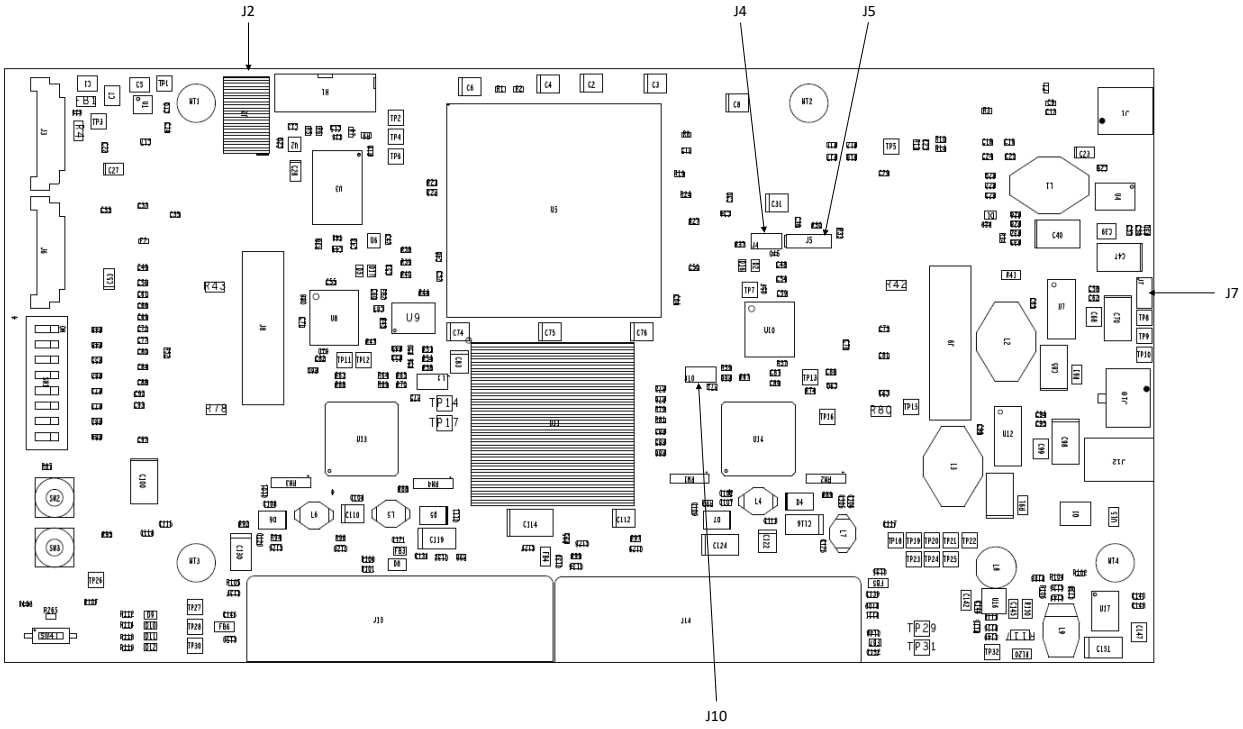

Figure 3-3. DLPLCRC410EVM Controller Configuration Jumpers

3.3.1 J2 – EXP Voltage Select

J2 – Used to select either 2.5 Volt or 3.3-V voltage supplies for the EXP bus FPGA banks. This setting needs to match the I/O voltage required by any board attached to the EXP connectors.

Table 3-16. EXP Voltage Select

Position	Bank Voltage
1-2	3.3 V
2-3	2.5 V

3.3.2 J4 – APPSFPGA Revision Select

J4 – If multiple firmware builds are stored in the APPSFPGA Configuration PROM, this is used to select the revision of firmware loaded from the PROM to the APPSFPGA.

Table 3-17. APPSFPGA Revision Select

Jumper Position	Revision Version
0-1	0
1-2	1

3.3.3 J5 – Shared USB Signal Enable/Disable

J5 – Used to connect or disconnect the USB signals that are shared between the USB/APPSFPGA Mictor Connector J10. This method can be useful to isolate test signals from the FPGA to the Mictor connector.

Table 3-18. Shared USB Signal Enable/Disable

Jumper Position	USB Signals
0-1	Disconnected from FPGA
1-2	Connected to FPGA
2-3	Automatically connect USB signals to FPGA when USB is connected to host PC

3.3.4 J7 – USB EEPROM Programming Header

J7 – Used to temporally disconnect the USB EEPROM from the device so the device can load the internal boot loader rather than any code in the EEPROM. Install J8 for Cypress internal boot loader.

3.3.5 J10 – DLPA200 B Output Enable

J10 – Used to enable the outputs for DLPA200 B. This needs to be enabled only if using the 1080p DMD, otherwise this can be disabled.

Table 3-19. DLPA200 B Output Enable

Jumper Position	DLPA200 B Outputs
0-1	Disabled
1-2	Enabled

3.4 Switches

This section defines the function of the switches on the DLPLCRC410EVM Controller Board. Switches 1 through 4 locations are shown in Figure 3-4

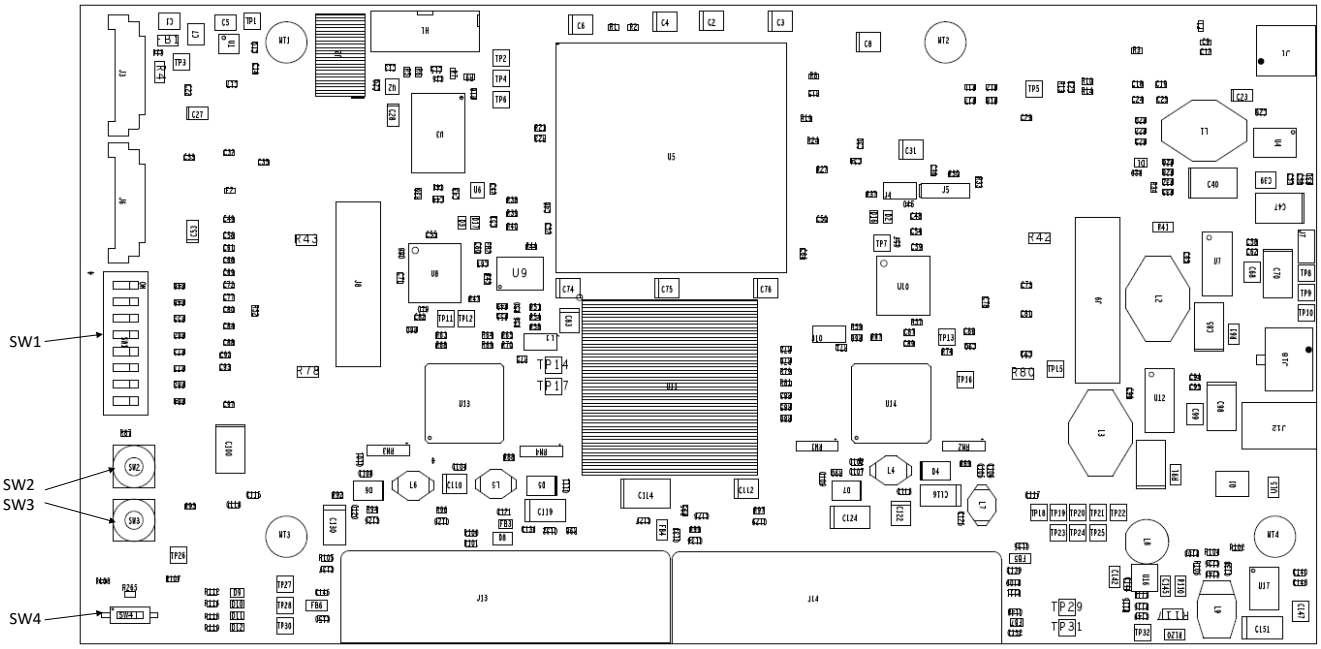

Figure 3-4. DLPLCRC410EVM On-Board Switches

3.4.1 SW1 - APPSFPGA Functional Switches

These switches provide controls within the Applications FPGA which impact the DLPC410/DMD modes of operation. For a list of the functions for each switch, see Table 3-20.

Table 3-20. SW1 Dip Switch Assignments

Switch Number	Effect
1	ON = Float (Park) all mirrors to the "flat" or "unbiased" state
2	ON = counter halt – this freezes the current test pattern on the DMD
3	ON = complement data – causes DLPC410 to complement all data received prior to sending to DMD
4	ON = north/south flip – causes the DLPC410 to reverse order of row loading, effectively flipping the image
6 and 5	Dictates the type of reset being used (where switch 6 is the MSB and ON = 1): • 00 : single block phased reset • 01 : dual block phased reset • 10 : global reset • 11 : quad block phased reset
7	ON = Row Address Mode
8	ON = Watchdog Timer Enable, disables other resets

3.4.2 SW2 - APPSFPGA Reset

This switch resets performs a logic reset of the APPSFPGA logic, also resulting in a reset of the DLPC410 and the DMD. This functionality is defined within the APPSFPGA.

3.4.3 SW3 - DMD Power Float (Park)

SW3 is a momentary push button switch which forces the DMD micromirrors to their Parked state. This functionality is defined within the APPSFPGA. TI **highly recommends** switch SW3 is pressed prior to removing power via SW4 or via the external power supply.

3.4.4 SW4 - Input Power On/Off

This switch turns of an off the 5 Volt input from the Power Connectors J12 and J18. Before powering off SW4 (or turning off the external power supply), TI **highly recommends** to first Park the DMD micromirrors by pressing SW3.

3.5 Power and Status LEDs

This section describes indicators that verify proper function of the DLPLCRC410EVM Controller Board. Figure 3-5 shows the controller board indicator locations.

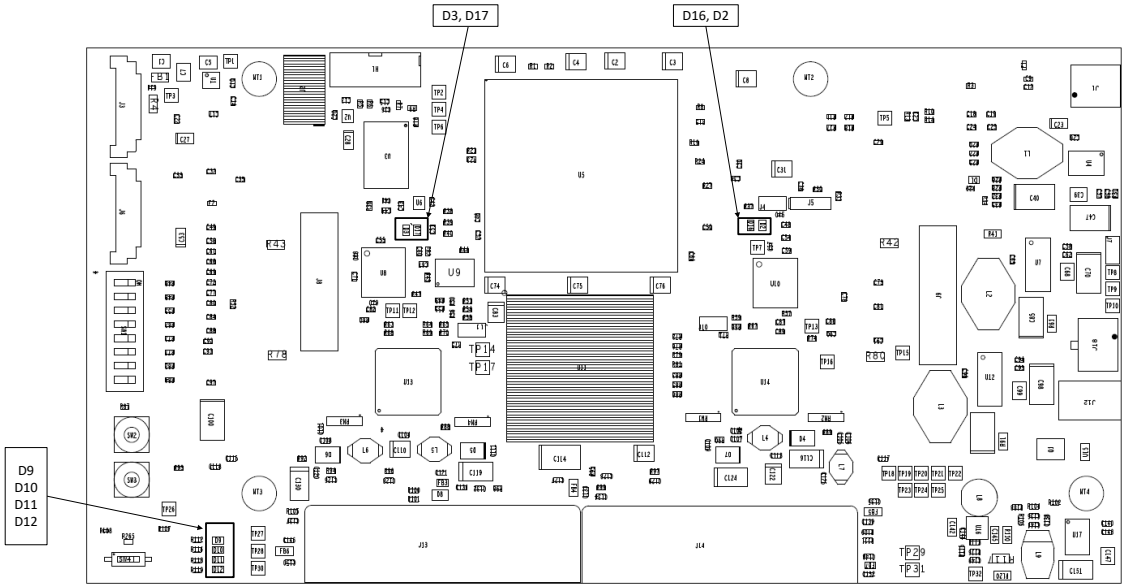

Figure 3-5. DLPLCRC410EVM Controller Board Indicators

3.5.1 D1 – USB Connection Indicator

This LED is not used at this time.

3.5.2 D2 and D16 – APPSFPGA Done

D2 is an LED which indicates the APPSFPGA is currently being configured from the Xilinx PROM. D2 is turned on when the APPSFPGA DONE pin is low, [not DONE]. Once the APPSFPGA is completely configured, the APPSFPGA DONE pin goes high and this LED turns OFF.

When the APPSFPGA DONE pin goes high indicating the APPSFPGA completed programming successfully and the APPSFPGA is up and running, the green LED D16 is turned on by internal logic with the enabling of the FPGA IO. This logic is to be defined by the application, although the logic can be a DCM lock monitor or a *heart beat* indicating clocks are operating. The default load drives with a simple high to turn the green LED on.

3.5.3 D3 and D17 – DLPC410 Done

D3 is an LED which indicates the DLPC410 is currently being configured from the DLPR410 PROM. D3 is turned on when the DLPC410 DONE pin is low, [not DONE]. Once the DLPC410 is completely configured, the DLPC410 DONE pin goes high and this LED turns OFF.

When the DLPC10 DONE pin goes high indicating the DLPC410 completed programming successfully and the DLPC410 is up and running, the green LED D17 is turned on by internal logic with the enabling of the DLPC410 IO.

3.5.4 D9 – DDC_LED0

D9 – DDC_LED0: Status LED for the DLPC410. See the DLPC410 data sheet for more details.

3.5.5 D10 – DDC_LED1

D10 – DDC_LED1: Status LED for the DLPC410. See the DLPC410 data sheet for more details.

3.5.6 D11 – VLED0

D11 – VLED0: The APPSFPGA application defines this logic. Drive low to turn on the LED. Drive high to turn off the LED.

3.5.7 D12 – VLED1

D12 – VLED1: This logic is to be defined by the APPSFPGA application. Drive low to turn on the LED. Drive high to turn off the LED.

3.6 Test Points

This chapter defines the location of on-board test points shown in Figure 3-6. Table 3-21 lists these test points.

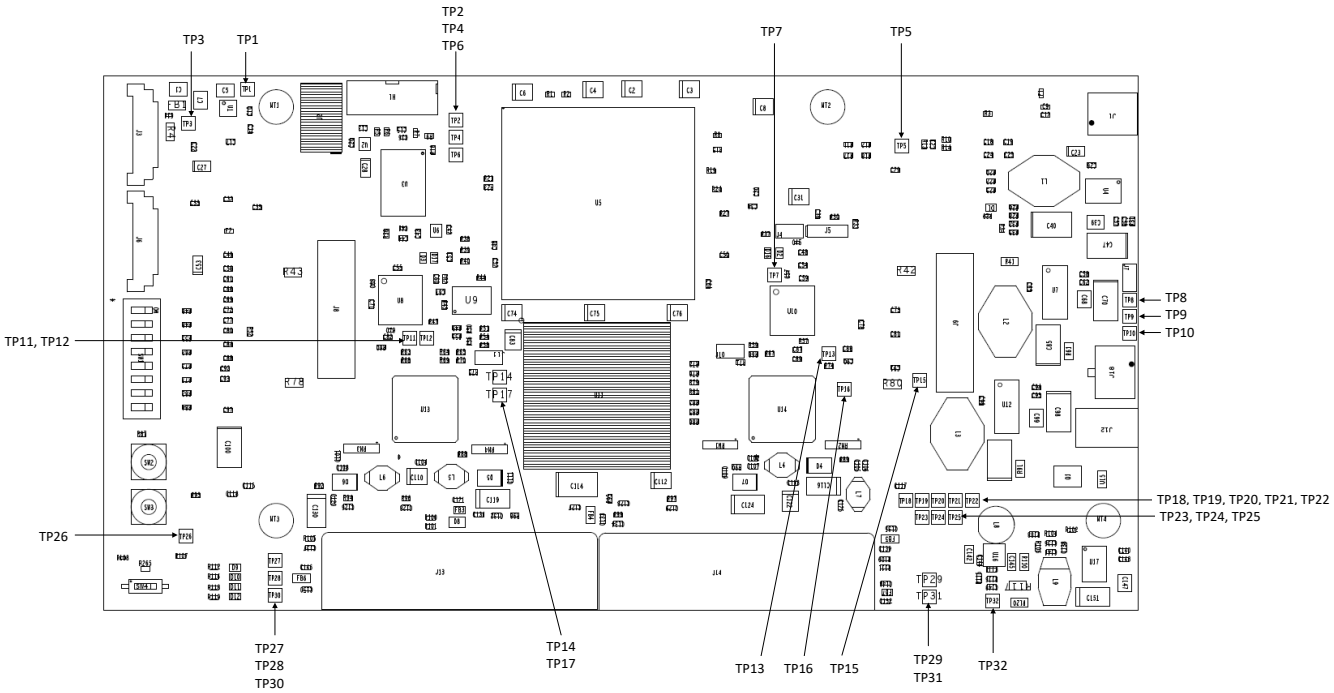

Figure 3-6. DLPLCRC410EVM Test Point Locations

Table 3-21. DLPLCRC410EVM Test Point Net Names

Test Point	Net Name	Test Point	Net Name
TP1	GROUND	TP2	V5_DXP
TP3	VCC_VREF	TP4	V5_DXN
TP5	GROUND	TP6	RESET
TP7	SCPDO	TP8	BKPT
TP9	VCC_3P3V	TP10	VCC_2P5V
TP11	MBRST1_8	TP12	DAD_A_IRQZ
TP13	DAD_B_IRQZ	TP14	DXP_0
TP15	PWRGD	TP16	MBRST2_0
TP17	DXN_0	TP18	SCPDI
TP19	DMDSPARE2	TP20	MBRST2_8
TP21	VCC_12V	TP22	GROUND
TP23	DMDSPARE3	TP24	GROUND
TP25	VCC_1P8V	TP26	POWER_STANDBY#
TP27	DMDSPARE0	TP28	MBRST1_0
TP29	VCC_1P0V_DDC	TP30	DMDSPARE0
TP31	SCPCLK	TP32	VCC_1P0V

4 Software

This chapter describes the operation of the DLP Discovery 4100 Explorer Graphical User Interface (GUI) software. The Discovery 4100 Explorer GUI provides control and display functions for the DLP Discovery 4100 Development Platform via the USB 2.0 interface to the DLPLCRC410EVM.

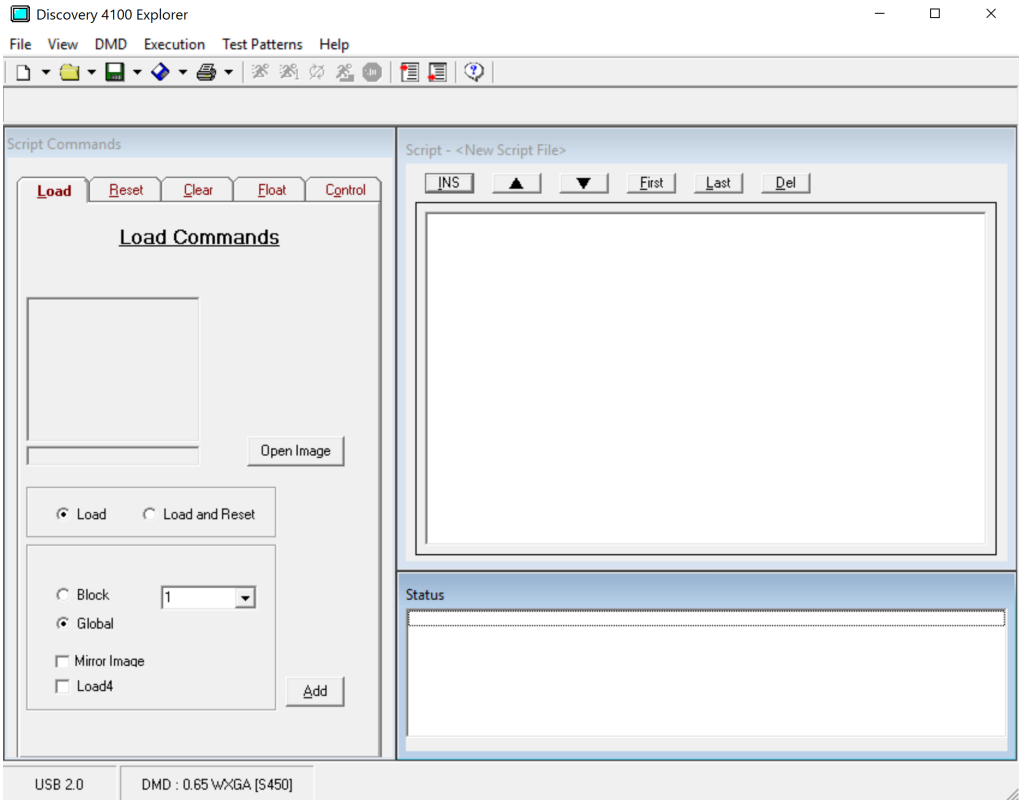

Figure 4-1. Discovery 4100 Explorer GUI

4.1 Overview

This section provides:

- A general description of the DLP Discovery 4100 Explorer GUI
- Descriptions of the Discovery 4100 Explorer menus, toolbars and display windows
- Operation instructions

4.1.1 Software Overview

The DLP Discovery 4100 Explorer GUI allows the user to control the DLPLCRC410EVM controller board hardware via USB 2.0 (or 1.1). The software uses the Discovery 4100 ActiveX™ control API which is documented separately in the *DLP® Discovery™ 4100 Development Platform API Programmer's Guide* (DLPU039). The software has controls for building and executing a command script.

The GUI provides users with access to the ActiveX control's implementations of the following commands:

- Load individual blocks or entire DMD from image file
- Reset individual blocks or global reset
- Clear individual blocks or global clear
- Float all DMD mirrors
- Wait for external global reset input
- Timed delay
- Loop iteration control – Loop for N times or until break
- General purpose digital output control
- Display internal test patterns
- Override HW switch (SW1) settings

Note

The GUI tool is intended for DMD demonstration capabilities only. The GUI tool is not intended for 24/7 operation, nor does the GUI necessarily meet customer end-application requirements as designed.

4.1.1.1 DMD Image Control

Images are controlled and displayed in blocks on the DMD. The organization of the DMD blocks varies for different DMD types as shown in Table 4-1. Blocks can be loaded and displayed individually, or as an entire image (all 15 or 16 blocks). Section 4.1.1.2 explains the commands to control the different ways an image can be displayed.

There are numerous combinations of display options available and this manual is not designed to cover them all. This user's guide presents an overview of how each command can be used to control an image. Section 4.4 describes how to run a script of commands to control the displaying of an image.

Table 4-1. DMD Characteristics

TYPE	COLUMNS	ROWS	BLOCKS	ROWS / BLOCK
DLP9500 - 0.95 1080p Type A	1920	1080	15	72
DLP7000 - 0.7 XGA Type A	1024	768	16	48
DLP650LNIR - .65 WXGA NIR S450	1280	800	16	50

For more information on display blocks for each DMD type refer to the DMD data sheets (DLP7000 § 8.4, DLP650LNIR § 8.4 and DLP9500 § 8.4).

4.1.1.2 Image Commands

- **Load** – Loads customer image blocks into the DMD memory.
- **Load and Reset** – Loads image blocks to the DMD memory. Displays contents on DMD micromirrors.
- **Reset** – Initiates a Mirror Clocking Pulse (Reset) to display DMD memory on DMD micromirrors.
- **Clear** – Clears (zeroes) the contents of DMD memory.
- **Clear and Reset** – Clears (zeroes) blocks of DMD memory. Displays contents on DMD micromirrors.
- **Float Mirrors** – Sets the mirrors to an unbiased (Parked) condition.

4.2 DLP Discovery 4100 Operation

The DLP Discovery 4100 Development Platform is capable of operating at about 7-10 DMD frames per second (DMD dependent) when connected to a host system's USB 2.0 port.

4.2.1 Quick Start Guide on Operation

D4100 Explorer Windows Installer Error

During installation, user can be prompted with an error stating the installation did not complete correctly and that there was an error executing the post installation script. If this happens, then please follow the steps below:

1. Uninstall the program
2. Download and Install Microsoft 2010 Vcredist x86 version
3. Reboot and re-install the DLPC410 GUI program

Note

Users need the 32-bit 2010 version of Vcredist, regardless of Windows OS bit level since the DLP Discovery 4100 Explorer GUI program is 32-bits.Vcredist 2010 installation is not a fix, but is the most prominent method that works for majority of customers.

If there are no installation errors, then the following steps must be followed to operate the device:

1. Install the software by executing the file *D4100Explorer-2.0-windows-installer.exe*. Install the software BEFORE connecting the USB cable to the DLPLCRC410EVM Controller Board. The setup program installa the software and driver INF files necessary for operation.
2. A reboot is recommended before connecting the kit because some systems do not properly install the drivers if the system is not re-booted first.
3. Connect the DLP with a USB 2.0 [mini-B to Type A] cable and apply power to the DLP Discovery 4100 Development Platform. The operating system detects the USB device and automatically install or prompt to install the driver.
4. If automatic driver installation fails, go to Device Manager (Search for Device Manager in Windows search bar).
5. Find the device and right click to select *Update Driver Software*.

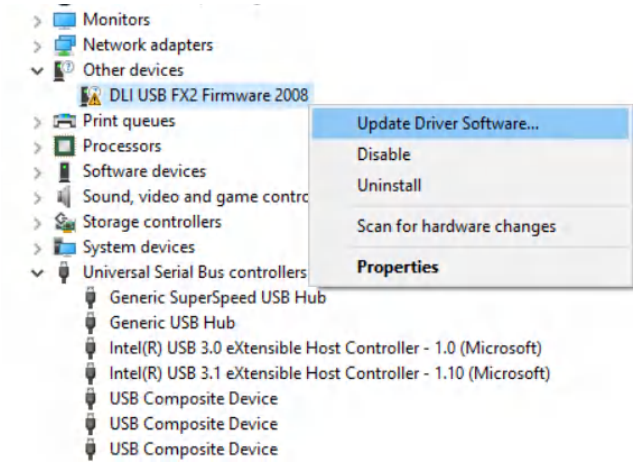

Figure 4-2. Updating Driver Software

6. Select *Browse my computer for driver software*.

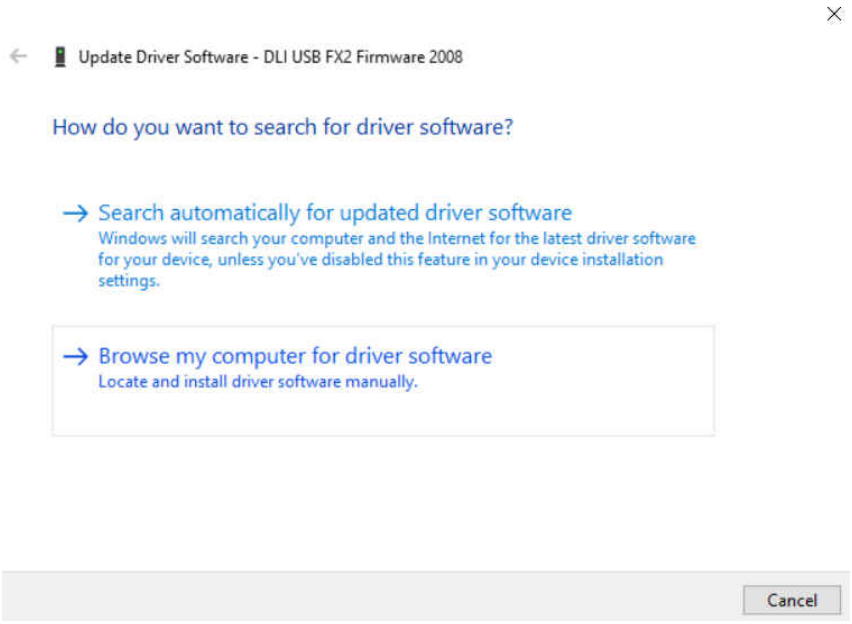

Figure 4-3. Browse for Driver Software

7. Click **Let me pick from a list of device drivers on my computer**.

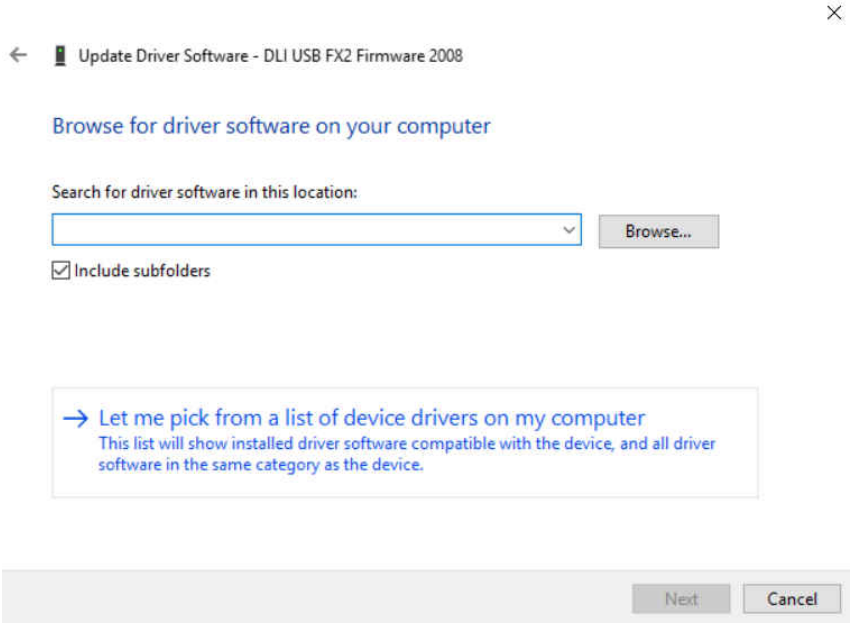

Figure 4-4. Pick from a list of Device Drivers

8. Select *Universal Serial Bus devices*. Click Next.

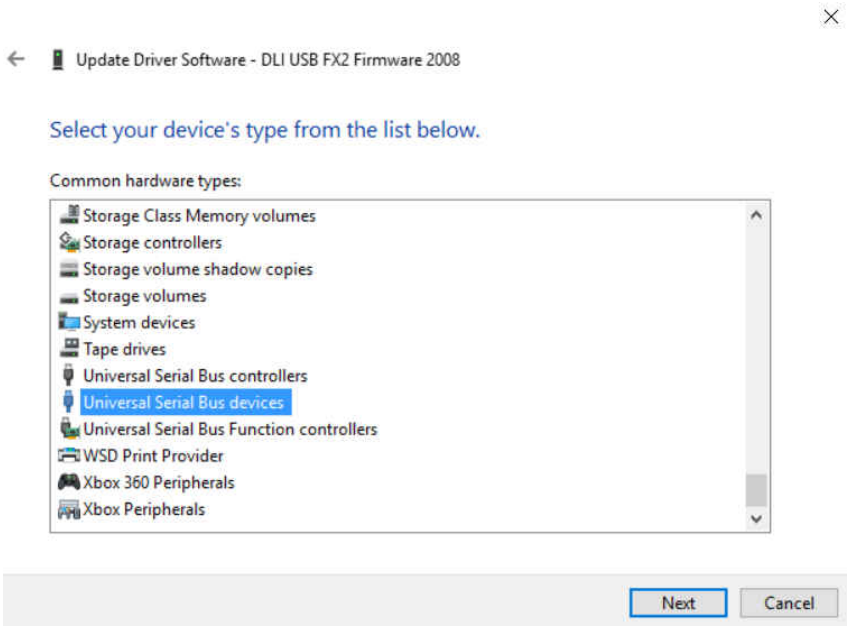

Figure 4-5. Select Universal Serial Bus devices

9. Click on **Have Disk**.

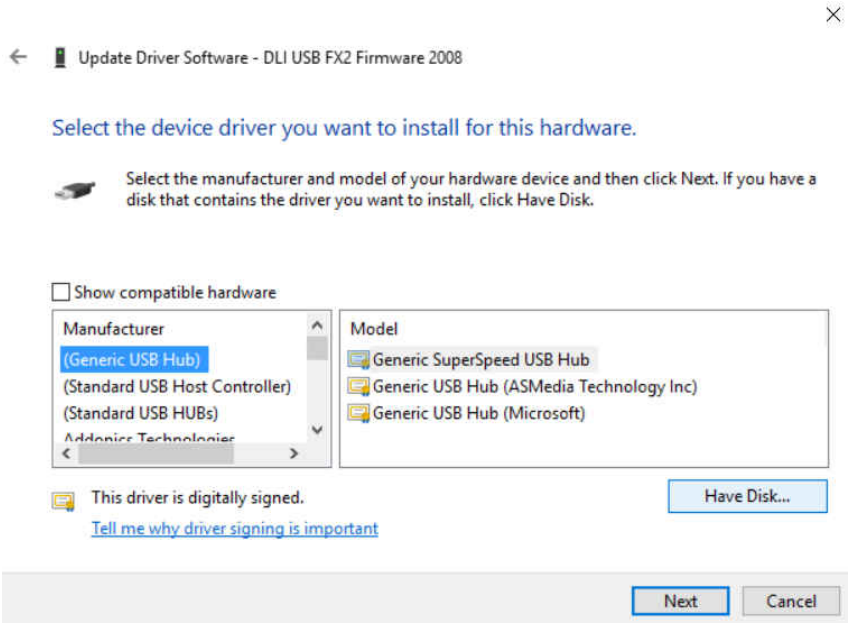

Figure 4-6. Have Disk

10. Browse to folder that contains the file *D4100-USB.inf*. This file is found in <GUI Install Directory>\Driver\. For example, in the Wndows 10 64 bit operating environment, navigate to *C:\Program Files (x86)\D4100Explorer\Driver\Win10\x64*. Click **Ok**.

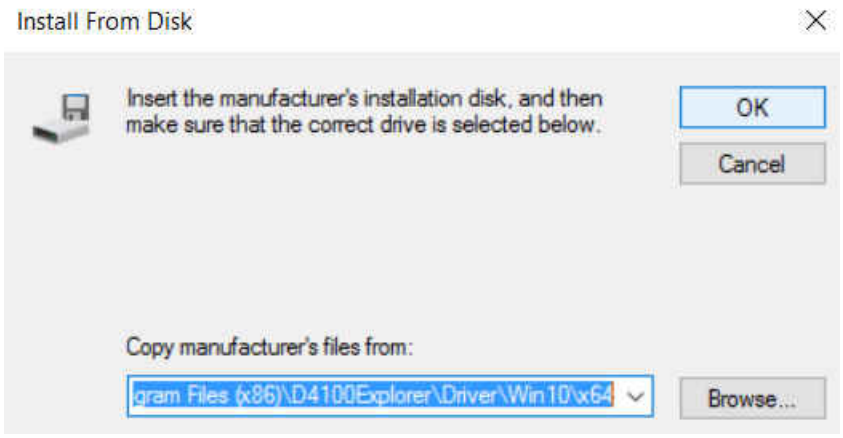

Figure 4-7. Browse for .inf file

11. Click **TI D4100 Explorer**
12. Click **Next**.

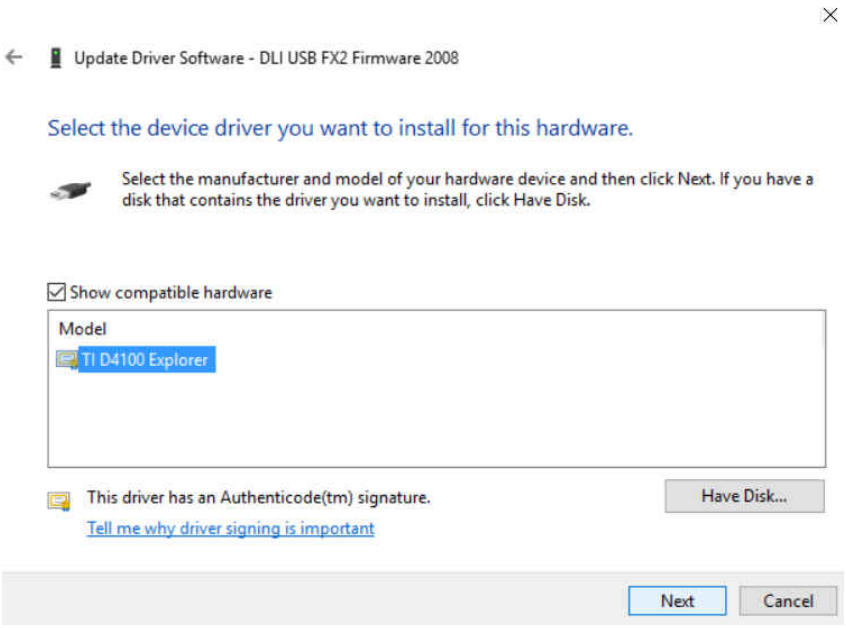

Figure 4-8. Select TI D4100 Explorer

13. Windows installs the driver.

14. Click **Close**.

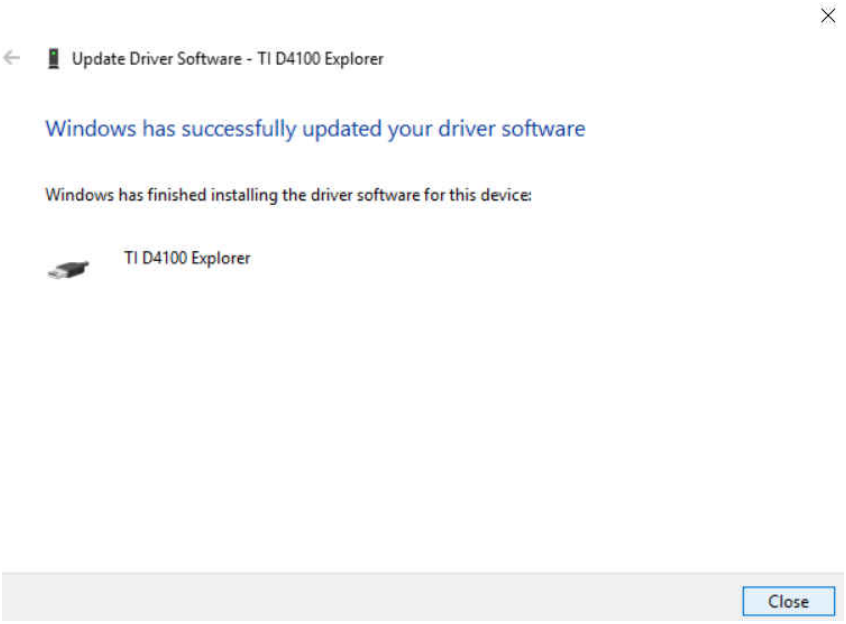

Figure 4-9. Driver Installation Window

15. Verify driver installation in **Device Manager** window as shown in Figure 4-10.

Figure 4-10. Verify Device

16. Start the DLP Discovery Explorer GUI from the *Start/Texas Instruments/DLP Discovery 4100 Explorer* menu.

17. The software starts. The USB connection status and DMD type is displayed in the lower left status panel (Figure 4-11):

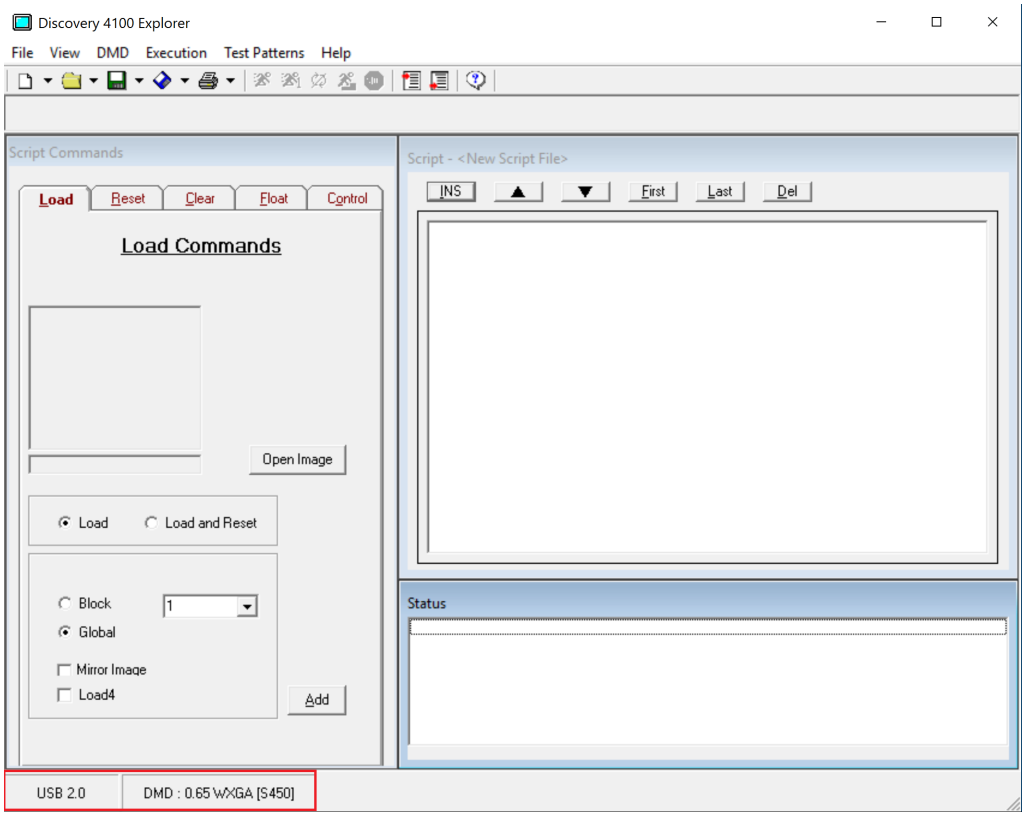

Figure 4-11. Discovery 4100 Explorer USB and DMD - Connection Status

18. Open an image using the Load Tab / Open Image button.
19. Enter an image command in the script by selecting the desired options in the Load Tab button and clicking **Add**.
20. Select and enter commands in the script. You select commands from any one of the command tabs on the Commands Window. Each tab contains a set of related commands and the options assigned to each command. Once you have selected the right combination of commands and options, enter the command into the script by clicking the **Add** button at the bottom of the command tab. Each tab has an **Add** button to enter that command into the script.
21. Execute the script. Once the desired list of commands has been entered into the Script Window, click the (Run) icon on the toolbar to begin executing commands. You can also choose to step through the commands using the (Step) icon on the toolbar instead of running through them all. You can also use the Execution menu to perform the same functions. Use the (Stop) icon on the toolbar to stop executing commands.

4.2.2

Note

When the GUI is connected to a single Discovery EVM, moving the USB connector to a different Discovery EVM of different resolution does not scale the images already defined in the GUI scripts, and, therefore, can show up as incorrect on the DMD. The answer is to always restart the GUI software program after connecting to a different Discovery EVM.

4.3 Graphical User Interface

The Explorer Software user interface consists of a multiple display interface containing a menu bar, toolbar and three display windows: Script Commands Window, Script Window and Status Window. The function of each item is described in the following sections.

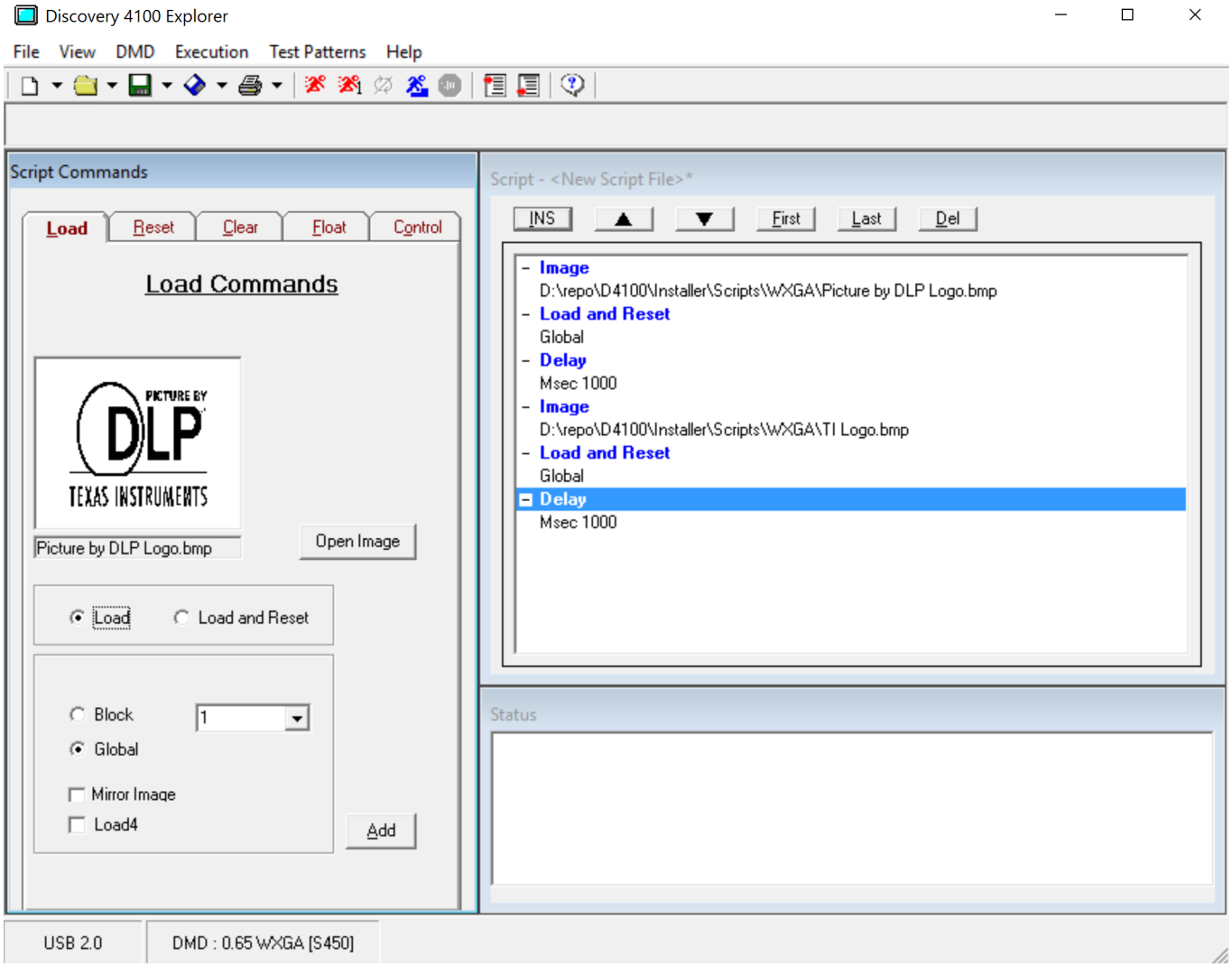

Figure 4-12. Graphical User Interface Layout

4.3.1 Menu Bar

The menu bar commands provide standard menu access to software commands as shown in Figure 4-13.

Figure 4-13. Menu Bar

4.3.1.1 File Menu

The File menu contains the standard New, Open, Save, Print, and Exit menu items. There are options to open a script or a status and to save a script or a status.

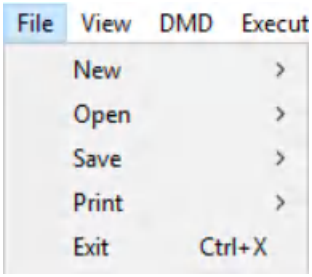

Figure 4-14. File Menu

4.3.1.2 View Menu

The View menu allows you to show or hide any of the display windows.

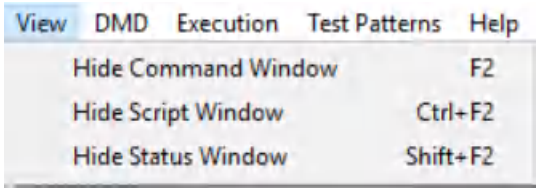

Figure 4-15. View Menu

4.3.1.3 DMD Menu

The DMD menu is used to select the DLPC410 Control operation mode.

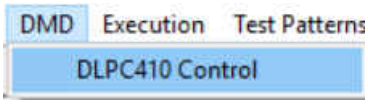

Figure 4-16. DMD Menu

4.3.1.4 Execution Menu

The Execution menu contains script commands and configuration options:

- Run – Executes all the commands in the list without interruption, repeating script until Stop selected.
- Run Once – Executes all the commands in the list without interruption for one cycle.
- Loop Break – Exit a "Loop Until Break" script command.
- Step – Sets the execution of commands to one step at a time mode.
- Next Step – Executes the next script command.
- Stop – End execution.
- Set Start – Sets the start point of command execution within the script.
- Set End – Sets the end point of command execution within the script.

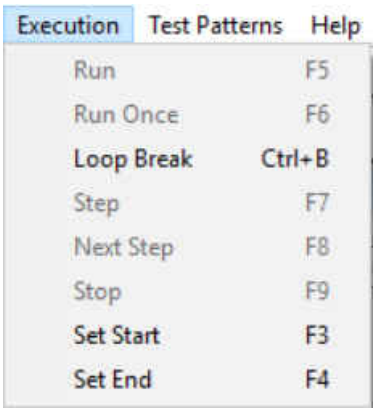

Figure 4-17. Execution Menu

4.3.1.5 Test Patterns Menu

The Test Pattern menu contains options to enter/exit internal test pattern mode, enable/disable software switch override and turn on/off GPIOs via GUI software.

- Pattern 1: DMD outside border
- Pattern 2: Varying size vertical lines
- Pattern 3: Small checkerboard
- Pattern 4: Vertical Bars
- Pattern 5: Tiny horizontal lines
- Pattern 6: Diagonal lines
- Pattern 7: Horizontal herringbone
- Pattern 8: Black field (all off)

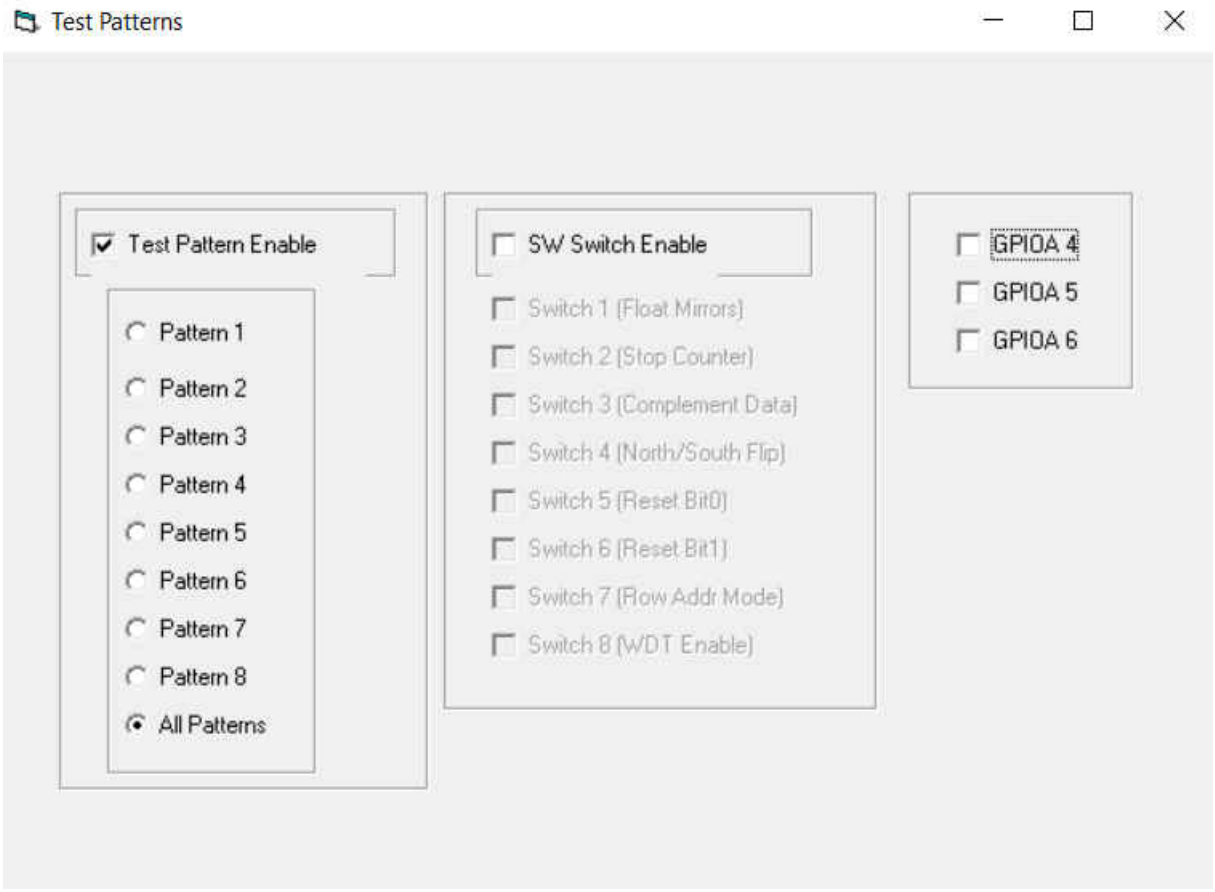

Figure 4-18. Test Patterns Menu

4.3.1.6 Help Menu

The Help menu contains a link to standard Windows help file contents and the command to load the About dialog box.

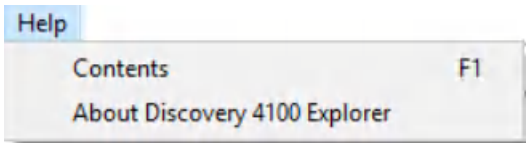

Figure 4-19. Help Menu

4.3.2 Toolbar

The toolbar provides operation shortcuts.

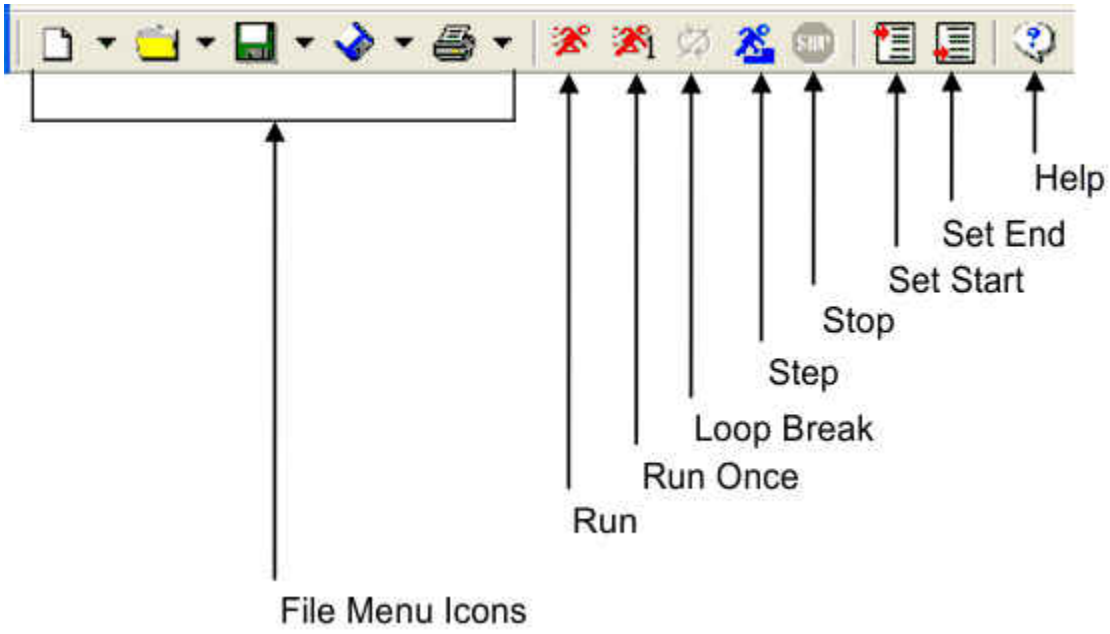

Figure 4-20. Toolbar

4.3.2.1 File Menu Buttons

The first five buttons on the toolbar, New, Open, Save, Save As, and Print, have the same function as the five items in the File menu.

4.3.2.2 Run, Run Once, Loop Break, Step and Stop Controls

Run, Run Once, Loop Break, Step and Stop icons control the execution of the list of commands in the script window. Command function is as described in Section 4.3.1.4.

4.3.2.3 Set Start and End Buttons

Set Start and Set End icons set the start point and end point of command execution within a script.

4.3.2.4 Help Button

The Help button displays the help contents for the application.

4.3.3 Script Commands Window

The Script Commands Window, Figure 4-21, contains a series of Command Tabs with command options for building script commands. A script is built by adding commands to execute the desired sequence of operations on the DMD. To view and select the options associated with a command, click on the corresponding command tab. Once you've selected the commands and options, click the Add button to add the command options to the script.

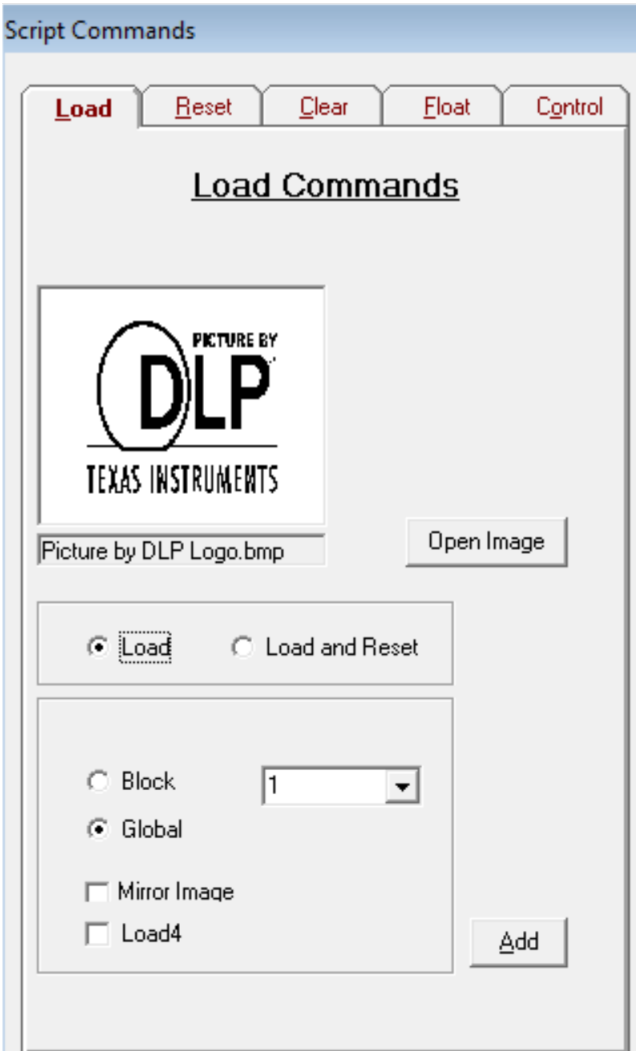

Figure 4-21. Script Commands Window

4.3.3.1 Load Tab

Load commands select the image file and specify load operations.

An image file must be selected before the Add button is pressed. To select an image file click the Open Image button and select the image file. Supported image file types are .bmp, .jpg, .gif and .bin. A .bin file is a binary file containing one bit per DMD pixel. TI recommends to use the initial 24 bit (non-binary) images and let GUI do the conversion to binary image to avoid error due to any unrecognized image format.

The image data can be loaded to DMD memory by selecting **Load** or the image data can be loaded and the DMD reset to display the image by selecting **Load and Reset**. If **Load and Reset** is not selected the image is not visible until a separate Reset command is executed.

The entire image can be loaded (**Global**) or individual blocks can be loaded (**Block**). Block numbers can be from 1 to 16. Loading block 16 on a DLP9500 (0.95 1080p) DMD is ignored since this DMD has only 15 blocks.

The image can be mirrored in the horizontal direction by selecting **Mirror Image**.

The DMD incorporates the Load4 operation to write 4 rows simultaneously with the same column data. This allows fast loading since only 1/4th of actual image data need to be sent to DMD. **Load4** option can be selected to enable this mode.

Select the desired options and **Add** button to add the command to the script.

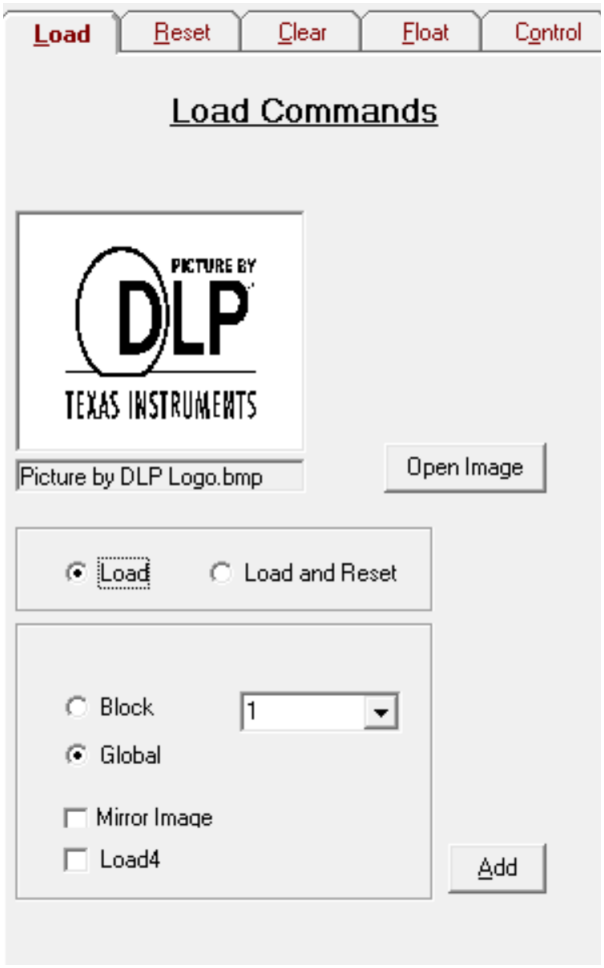

Figure 4-22. Load Tab

4.3.3.2 Reset Tab

The **Reset** command causes the mirrors to change from the current state to the state of that in memory. The contents of memory are determined by the Load or Clear commands. You can choose to reset all the blocks (**Global**), or you can choose to reset blocks individually using the **Single Block** option or a group of blocks using one of the **Multiple Blocks** options. Select the option you want to use and click the **Add** button to add the command to the script.

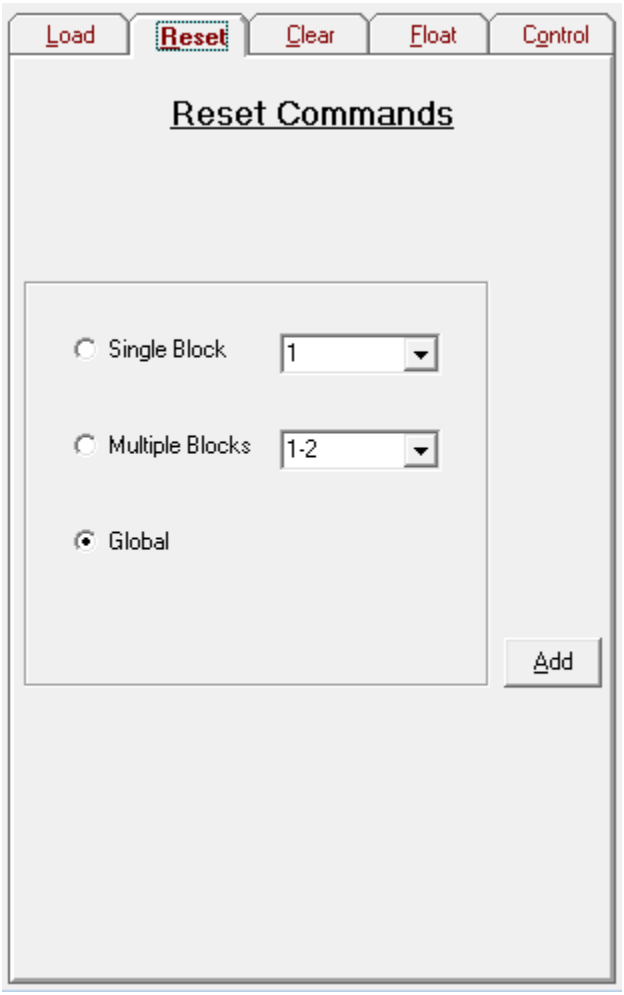

Figure 4-23. Reset Tab

4.3.3.3 Clear Tab

The Clear Tab commands clear the memory contents of all the blocks using the **Global** option or individually using the **Single Block** option by writing zeroes to the contents of DMD memory. The Clear option clears memory only, the **Clear and Reset** option clears memory and performs a reset to change the display. Select the desired option and click on the **Add** button to add to script (see Figure 4-24).

Note

NOTE: The **Global** option is implemented in software by sequentially issuing a DMD Block Clear command to all the blocks on the DMD.

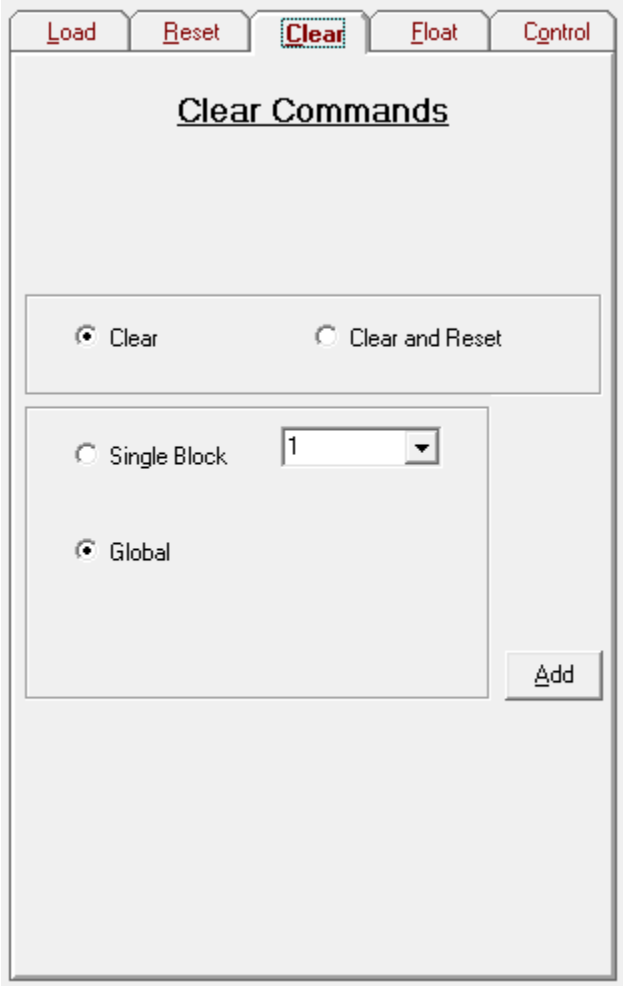

Figure 4-24. Clear Tab

4.3.3.4 Float Tab

The **Float Tab** script command places the DMD in a short-term safe state with the mirrors in the software induced floated (nominally flat) condition with bias removed from the DMD mirrors. For power down conditions, a hardware power-float is recommended prior to power removal via assertion of switch SW3 of the EVM, or an equivalent assertion of the PWR_FLOAT input pin of the DLPC410.

Figure 4-25. Float Tab

4.3.3.5 Control Tab

The Control commands tab supports commands for script execution control, external reset, and digital output:

- The Wait for External Reset scripting command waits 10 seconds for an external global reset triggered by a rising edge on APPSFPGA input GPIO_A0. After 10 seconds, execution of the script resumes with the next command in the script. GPIO_A0 is a 2.5 Volt CMOS input.
- The Delay command delays for the specified time in msec.
- The Loop Until Break command loops until the Break button is clicked.
- The Loop command loops for the specified number of iterations.
- The Set GP Output command sets the value of the APPSFPGA general purpose digital outputs GPIO_A(4 - 6). Value is entered in decimal or hexadecimal (e.g. 0x3). Bits 0, 1, 2 of value control the output state of GPIO_A4, GPIO_A5, and GPIO_A6 respectively. Bits 7, 6, 5, 4, 3 of Value are not used. GPIO_A(4 - 6) are 2.5 Volt CMOS outputs.

Note

NOTE: For more information on GPIO outputs see the *DLP® Discovery™ 4100 Development Platform API Programmer's Guide* (DLPU039 § 5.2.24 and § 6.2.24).

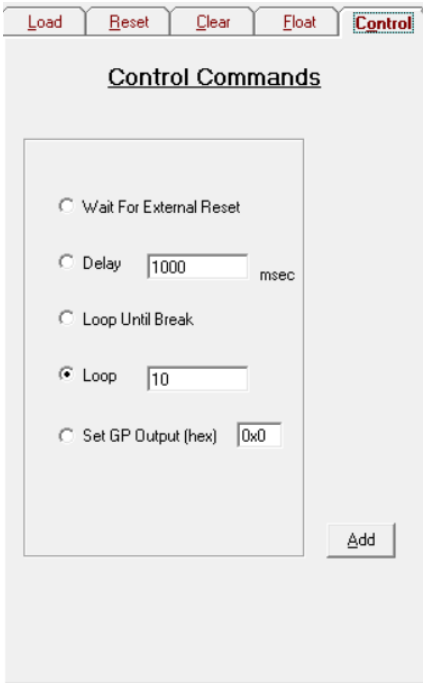

Figure 4-26. Control Tab

4.3.4 Status Window

The Status Windows displays the execution status, retrieved information and any responses sent back to the host from the DLP Discovery 4100 Development Platform after a command has been executed.

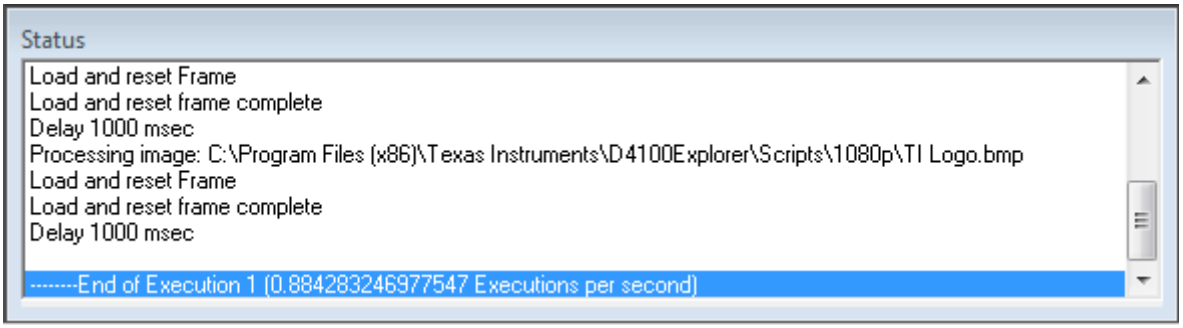

Figure 4-27. Status Window

4.3.5 Script Window

The Controller Board GUI uses a Script window to keep track of the images to be loaded and the commands to be executed on the DMD (Figure 4-28). Once you've added an image and the commands you want to execute to the script, you can change the command order, delete and insert commands at a specified location within the script.

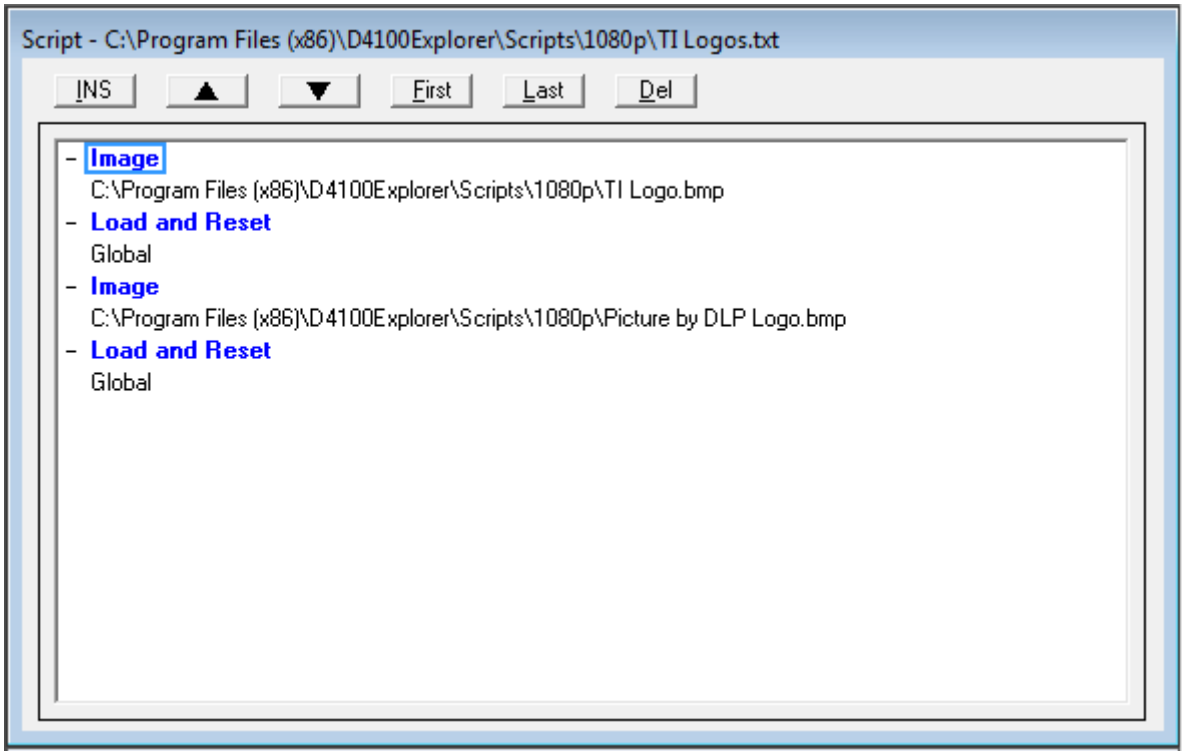

Figure 4-28. Script Window

The application executes commands in the order in which the commands are entered in the script. For the application to execute commands, the first command in the script must be the **Image** command followed by the correct path and file name for an existing image. To learn how to insert an image into the script, see Section 4.3.3.1.

4.3.5.1 Inserting Commands

To insert a command in a specified location on the script:

- Select the command from the Commands window, go to the desired location in the script and click the INS (INS) button at the top of the Script Window.

4.3.5.2 Moving Commands

To alter the command order:

- Select the command you want to move by clicking on the command, then click the ▲ (Up) arrow or the ▼ (Down) arrow to move to the desired location.

You can also move a command by:

- Clicking the First (First) position in the script by using the button, or move the command to the Last (Last) position with the button.

4.3.5.3 Deleting Commands

To delete a command from the script, click on the command and click the (Del) button at the top of the Script Window.

4.4 Script and Status Operations

4.4.1 Saving Scripts and Statuses

4.4.1.1 Saving a Script

To save a script, proceed as follows:

1. Select the Script option from the (Save) or (Save As) icon drop down menu on the tool bar, or select Save Script or Save Script As from the Save option menu on the File menu.
2. Once the selection is made, a common dialog box appears. Select or type the name of the file to save the script to.
3. Click the **OK** button and a message box appears to notify you that the script has been saved.

4.4.1.2 Saving a Status

To save the contents of the Status Window, proceed as follows:

1. Select the Status option from the (Save) or (Save As) icon drop down menu on the tool bar, or select Save Status or Save Status As from the Save option menu on the File menu.
2. Once the selection is made, a common dialog box appears. Select or type the name of the file to save the status.
3. Click the OK button and a message box appears to notify that the status log has been saved.

Note

Status files are saved with a .sts extension.

4.4.2 Printing Scripts and Statuses

4.4.2.1 Printing a Script

To print a script:

- Select the Script option from the  (Print) icon drop down menu on the toolbar, or select the Script item from the Print option menu on the File menu.

4.4.2.2 Printing a Status

To print the contents of the Status Window:

- Select the Status option from the  (Print) icon drop down menu on the toolbar, or select the Status item from the Print option menu on the File menu.

4.4.3 Opening Scripts and Statuses

You can open scripts [*.txt] or status files [*.sts] that have been previously saved by:

- Clicking the (Open File) icon on the toolbar or by selecting the Script or Status option from the  Open File menu on the File menu. Once you have selected the desired file, the file is opened and the script or status file is displayed in the Script or Status window.

Note

Scripts can be edited with a simple text editor. Therefore, when a script is opened, the script is checked for consistency. If a command is missing a matching parameter or a parameter is missing a matching command, then an error dialog appears and the script is not opened. The script must be corrected before the script can be opened.

4.4.4 Creating New Scripts and Statuses

You can create a new script or status file by clicking the New File icon on the toolbar and then selecting the Script or Status option or by selecting the Script or Status option from the New File menu item on the File menu.

4.4.4.1 Creating a New Script

To open a new script:

- Select the Script option from the  (New) toolbar icon drop down menu, or select the Script item from the New option menu on the File Menu.

Once the selection is made, you are first prompted to save the current script and then a blank script is inserted.

4.4.4.2 Creating a New Status

To open a new status:

- Select the Status option from the  (New) toolbar icon drop down menu, or select the Status item from the New option menu on the File Menu.

Once the selection is made, you are first prompted to save the current status log and then a blank status is inserted.

4.5 DLPC410 Control Window

The DLPC410 Control window is accessed through the DMD/DLPC410 Control menu and provides direct control of the DLPC410 input signals. No script commands are generated, the control is applied immediately to the DLPC410 when a Set button is clicked.

The upper portion of the window supports reading and setting of the DLPC410 signals used in writing data to the DMD. The current value for ROWMD (Row Mode), ROWADDR (Row Address), BLKMD (Block Mode), and BLKADDR (Block Address) is displayed in the Current Value column. When a new value is entered in Hexadecimal in the Hex column and the Set button is clicked the value sent to the DLPC410. The Load Row button sends one row with repeating values of the 4 digit hex value entered.

The lower portion of the window supports control of the DLPC410 input signals which are control operational modes. Click a button to toggle the current value of the signal.

Note: Asserting PWRFLOAT (Power Float) Parks the DMD mirrors. Recovery requires reset to the APPSFPGA either via asserting APPS_LOGIC_RST (HW switch SW2) or power cycling the EVM to restart the operation of the D4100 system again.

Refer to the DLPC410 data sheet (DLPS024) for detailed information on the DLPC410 input signals.

Refer to the DLP Discovery 4100 Development Platform API Programmer's Guide (DLPU039) for detailed information about the ActiveX functions called by the buttons on this DMD/DLPC410 Control menu page.

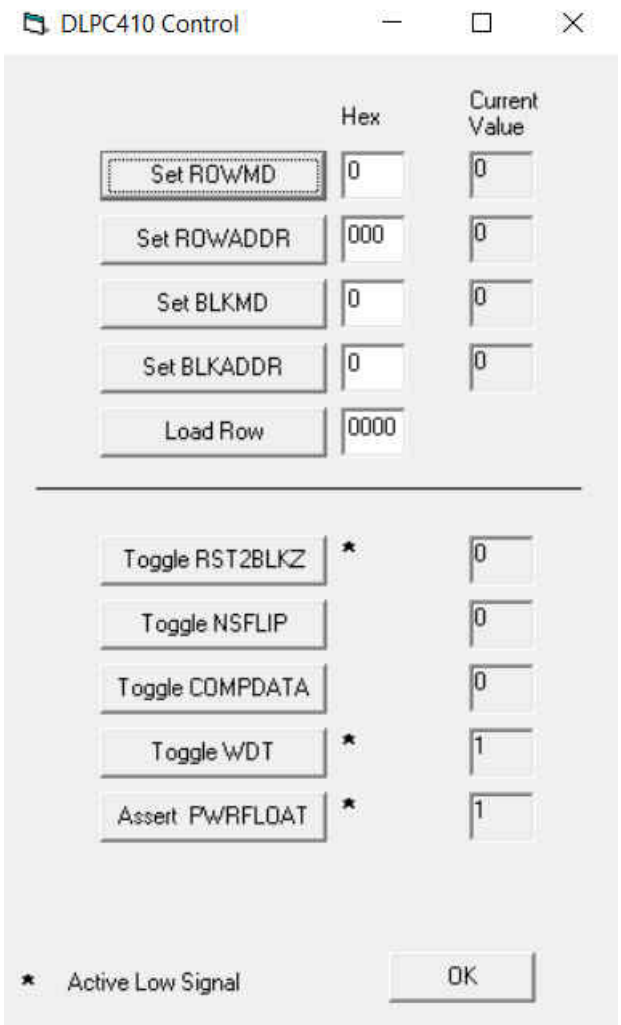

Figure 4-29. DLPC410 Control Window

4.6 Test Patterns Window

The Applications FPGA (APPSFPGA) supports two modes.

- Internal Test Patterns Mode - Fixed test patterns stored in the APPSFPGA are selected and displayed on the DMD. This mode does not support scripting.
- User Pattern Mode - User defined images can be downloaded to the APPSFPGA from the GUI for display on the DMD. This is done using the Script Window. When a script is run, the GUI automatically switches to User Pattern Mode even if Internal Test Patterns Mode was previously enabled.

The Test Patterns window is accessed through the Test Patterns menu as seen in Figure 4-30.

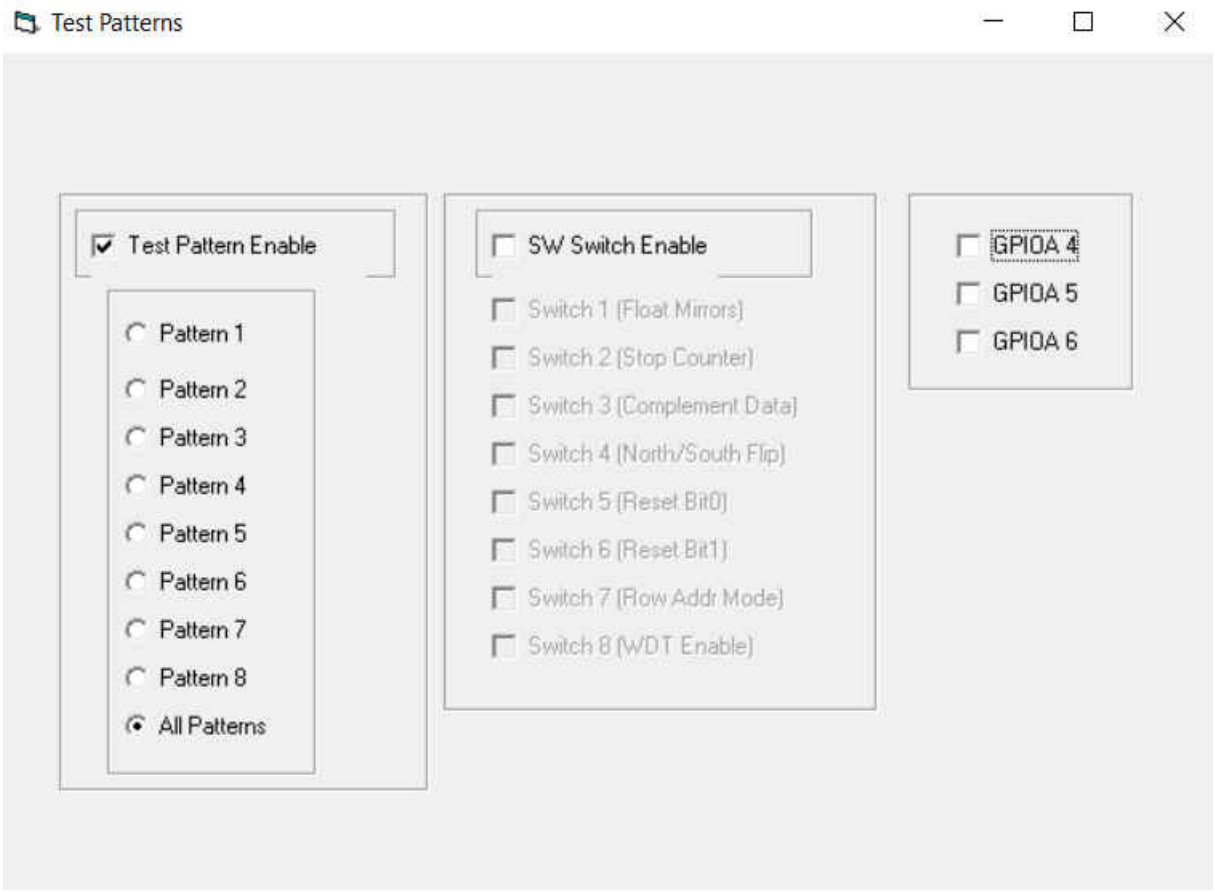

Figure 4-30. Test Patterns Window

The Test Patterns window provides the following functions:

- **Enable/Disable Internal Test Patterns Mode.** If Internal Test Patterns Mode is enabled, then various internal patterns can be selected to display on the DMD. When "All Patterns" is selected then all internal patterns are displayed in round-robin fashion.
- **Enable/Disable Software Switch Override**. When enabled, this switch overrides the hardware switch settings of switch SW1 found on the DLPLCRC410EVM Controller Board. The HW DIP Switch assignments are repeated here in Table 4-2 for clarity.
- **GPIO_A(4 - 6) enable/disable**. The [GPIOA 4], [GPIOA 5], and [GPIOA 6] selections in the Test Patterns window map directly to the GPIO_A4, GPIO_A5, and GPIO_A6 outputs of the APPSFPGA, found on connector GPIO_A.

Table 4-2. SW1 Dip Switch Assignments

HW Switch SW1 Number	Effect
1	ON = float – float all mirrors
2	ON = counter halt – stop counter, this freezes the image on the DMD
3	ON = complement data – causes DLPC410 to complement all data received
4	ON = north/south flip – causes the DLPC410 to reverse order of row loading, effectively flipping the image
6 and 5	Dictates the type of reset being used (where switch 6 is the MSB and ON = 1): • 00 : single block phased reset • 01 : dual block phased reset • 10 : global reset • 11 : quad block phased reset
7	ON = Row Address Mode
8	ON = Watchdog Timer (WDT) Enable, disables other resets

Refer to the DLP Discovery 4100 Development Platform API Programmer's Guide (DLPU039) for detailed information about the ActiveX functions called by the buttons on this Test Patterns menu page.

4.7 About Box

The About Box provides version information about various software and hardware of the DLP Discovery 4100 Development Platform.

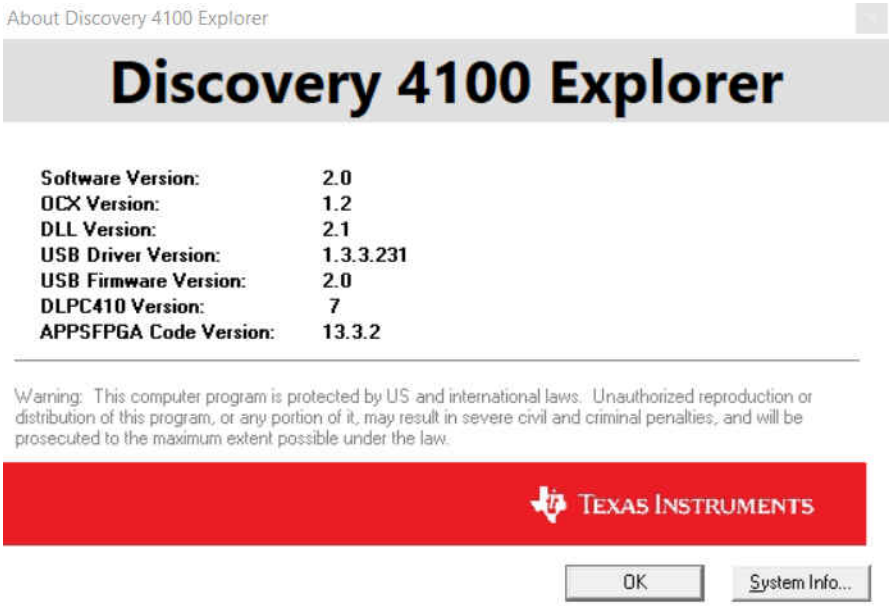

Figure 4-31. About Box

4.8 Links

For more information about Texas Instruments DLP Discovery 4100 Development Platform visit www.ti.com/tool/dlpd4x00kit.

5 Related Documentation

This section lists related documents associated with the use of the DLPC410 Controller Board.

DLP650LNIR DMD Data Sheet

DLP7000 DMD Data Sheet

DLP7000UV DMD Data Sheet

DLP9500 DMD Data Sheet

DLP9500UV DMD Data Sheet

DLPC410 Digital Controller Data Sheet

DLPR410 Configuration PROM Data Sheet

DLPA200 Micromirror Driver Data Sheet

D4100 Controller Board design files containing:

- D4100 Board ESD - electronic schematic
- D4100 Board GERBER & BRD files
- D4100 Board CCA - circuit card assembly
- D4100 Board BOM - circuit card assembly

DLP9500(UV) Board design files containing:

- DLP9500 Board ESD - electronic schematic
- DLP9500 Board GERBER & BRD files
- DLP9500 Board CCA - circuit card assembly
- DLP9500 Board BOM - circuit card assembly

DLP7000(UV) Board design files containing:

- DLP7000 Board ESD - electronic schematic
- DLP7000 Board GERBER & BRD files
- DLP7000 Board CCA - circuit card assembly
- DLP7000 Board BOM - circuit card assembly

DLP650LNIR Board design files containing:

- DLP650LNIR Board ESD - electronic schematic
- DLP650LNIR Board GERBER & BRD files
- DLP650LNIR Board CCA - circuit card assembly
- DLP650LNIR Board BOM - circuit card assembly

DLP DIscovery 4100 Development Platform API Programmer's Guide

www.cypress.com for the Cypress CY7C68013A USB Controller

www.xilinx.com APPSFPGA development tools and information

6 Appendix

6.1 Abbreviations and Acronyms

The following lists abbreviations and acronyms used in this manual.

APPSFPGA	Xilinx Virtex 5 FPGA on DLPLCRC410EVM for customer applications
D4100 Platform	DLP Discovery 4100 Development Platform
DC	Direct Current
DDR	Double Data Rate
DMD	Digital Micromirror Device
EVM	Evaluation Board
FCC	Federal Communications Commission
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
GUI	Graphical user interface
HW	Hardware
NIR	Near Infrared
PROM	Programmable Read Only Memory
SCP	Serial Communications Port
SW	Switch
SRAM	Static Random Access Memory
USB	Universal Serial Bus
WXGA	Wide Extended Graphics Array
XGA	Extended Graphics Array

6.2 Notational Conventions

This document uses the following conventions.

6.2.1 Information About Cautions and Warnings

This book contains cautions and warnings.

CAUTION

This is a description of a caution statement: A caution statement describes a situation that can potentially damage your software or equipment.

WARNING

This is a description of a warning statement: A warning statement describes a situation that can potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning: This equipment is intended for use in a laboratory test environment only. The equipment generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments can cause interference with radio communications, in which case the user at his/her own expense is required to take whatever measures can be required to correct this interference.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2018) to Revision B (March 2023)	Page
• Added steps on Windows Installer Error for DLP Discovery 4100 Explorer GUI	33

Changes from Revision * (October 2016) to Revision A (November 2018)	Page
• Added Discovery EVM Technical Reference Manual (DLPU053) into this EVM GUI Software Users Guide.	5
• Changed overview to identify updated Discovery 4100 Platform with 6 mix and match EVMs	5
• Added new DLP650LNIR DMD references (multiple)	5
• Swapped out old DLPC410 Controller PCB layout with new one (new power connector, D16, D17) multiple places	12
• Added J12 and J18 Input Power Connector definitions	13
• Added a switch location diagram to Section 3.4. Renamed and edited switch sections for clarity	27
• Added D16 (last layout changed dual LED D2 into single LEDs D2 and D16)	29
• Added D17 (last layout changed dual LED D3 into single LEDs D3 and D17	29
• Updated GUI screenshot showing DLP650LNIR connected (0.65 WXGA)	31
• Added support information and links for DLP650LNIR (multiple)	32
• Added description of new GUI Test Pattern Menu/controls	42
• Changed Load Tab Image to new screen capture with Load4	45
• Added description of new Test Patterns Window and allowed selections	54

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265