High Speed Transistor Optocouplers

Single Channel:
HCPL0453, HCPL0500, HCPL0501
Dual Channel:
HCPL0531, HCPL0534

HCPL0453, HCPL0500, HCPL0501, HCPL0531, HCPL0534

Description

The HCPL05XX, and HCPL04XX optocouplers consist of an AlGaAs LED optically coupled to a high speed photo−detector transistor housed in a compact 8−pin small outline package.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base−collector capacitance of the input transistor. The HCPL04XX devices do not have the base bonded out to a lead for additional noise margin. The HCPL053X devices have two channels per package for optimum mounting density.

Features

- High Speed − 1 MBit/s
- 15 kV/μs Minimum Commone Mode Transient Immunity at V_{CM} = 1500 V (HCPL0453/0534)
- Open Collector Output
- Guaranteed Performance Over Temperature: 0°C to 70°C
- U.L. Recognized (File # E90700)
- VDE0884 Recognized (File # 136616)
  - Approval Pending for HCPL0531/0453
  - Ordering Option V, e.g., HCPL0500V
- BSI Recognized (File # 8661, 8662)
  - HCPL0500/0501 only

Applications

- Line Receivers
- Pulse Transformer Replacement
- Output Interface to CMOS−LSTTL−TTL
- Wide Bandwidth Analog Coupling

TRUTH TABLE (Positive Logic)

LED	V_O
ON	LOW
OFF	HIGH

ON Semiconductor®

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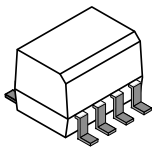

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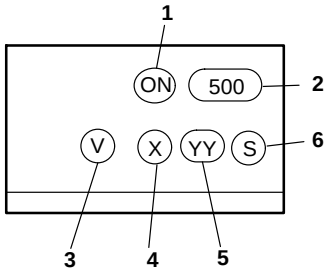
MARKING DIAGRAM



1. ON = ON Semiconductor Logo
2. 500 = Device Number
3. V = VDE mark indicates DIN EN/IEC60747−5−5 approval (Note: Only appears on parts ordered with VDE option – See Ordering Information Table)
4. X = One−Digit Year Code, e.g. ‘3’
5. YY = Two Digit Work Week Ranging from ‘01’ to ‘53’
6. S = Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

SCHEMATICS

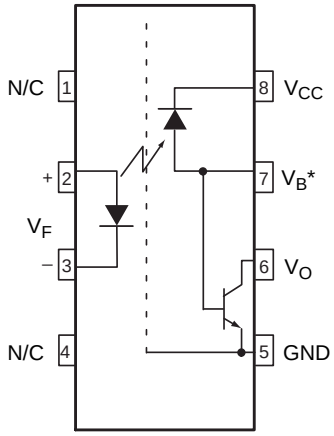


Figure 1. Single−channel Circuit Schematics (HCPL0500, HCPL0501 *Base Not Connected for HCPL0453)

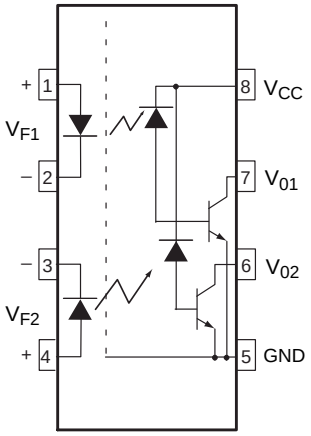


Figure 2. Dual−channel Circuit Schematics (HCPL0531, HCPL0534)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +85	°C
	Reflow Temperature Profile (Refer to page 7)		
EMITTER			
I_F (avg)	DC/Average Forward Input Current	25	mA
I_F (pk)	Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	50	mA
I_F (trans)	Peak Transient Input Current (t ≤ 1 μs P.W., 300 pps)	1.0	A
V_R	Reverse Input Voltage	5.0	V
P_D	Input Power Dissipation	45	mW
DETECTOR			
I_O (avg)	Average Output Current (Pin 6)	8	mA
I_O (pk)	Peak Output Current	16	mA
V_{EBR}	Emitter−Base Reverse Voltage (HCPL0500/0501 only)	5	V
V_{CC}	Supply Voltage	−0.5 to 30	V
V_O	Output Voltage	−0.5 to 20	V
I_B	Base Current (HCPL0500/0501 only)	5	mA
P_D	Output Power Dissipation	100	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max.	Unit
EMITTER							
V_F	Input Forward Voltage	I_F = 16 mA, T_A = 25°C	All		1.45	1.7	V
		I_F = 16 mA				1.8	
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	All	5.0			V
$\Delta V_F / \Delta T_A$	Temperature Coefficient of Forward Voltage	I_F = 16 mA	All		−1.6		mV/°C
DETECTOR							
I_{OH}	Logic High Output Current	I_F = 0 mA, V_O = V_{CC} = 5.5 V, T_A = 25°C	All		0.001	0.5	μA
		I_F = 0 mA, V_O = V_{CC} = 15 V, T_A = 25°C	All		0.005	1	
		I_F = 0 mA, V_O = V_{CC} = 15 V	All			50	
I_{CCL}	Logic Low Supply Current	I_F = 16 mA, V_O = Open, V_{CC} = 15 V	HCPL0453/ 0500/1		120	200	μA
			HCPL0531/4			400	
I_{CCH}	Logic High Supply Current	I_F = 0 mA, V_O = Open, V_{CC} = 15 V, T_A = 25°C	All		0.01	1	μA
		I_F = 0 mA, V_O = Open, V_{CC} = 15 V	HCPL0453/ 0500/1			2	
			HCPL0531/4			4	

TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max.	Unit
COUPLED							
CTR	Current Transfer Ratio (Note 1)	I_F = 16 mA, V_O = 0.4 V, V_{CC} = 4.5 V, T_A = 25°C	HCPL0500	7	27	50	%
			HCPL0453	19	27	50	
			HCPL0501/0531				
		I_F = 16 mA, V_O = 0.5 V, V_{CC} = 4.5 V	HCPL0500	5	30		
			HCPL0453	15	30		
			HCPL0501/0534				
V_{OL}	Logic Low Output Voltage	I_F = 16 mA, I_O = 1.1 mA, V_{CC} = 4.5 V, T_A = 25°C	HCPL0500		0.18	0.4	V
		I_F = 16 mA, I_O = 3 mA, V_{CC} = 4.5 V, T_A = 25°C	HCPL0453		0.25	0.4	
			HCPL0501/0531/4				
		I_F = 16 mA, I_O = 0.8 mA, V_{CC} = 4.5 V	HCPL0500		0.13	0.5	
		I_F = 16 mA, I_O = 2.4 mA, V_{CC} = 4.5 V	HCPL0453		0.23	0.5	
			HCPL0501/0531/4				

*All typicals at T_A = 25°C

ELECTRICAL CHARACTERISTICS (CONTINUED) (T_A = 0°C to 70°C unless otherwise specified)

SWITCHING CHARACTERISTICS (TV_{CC} = 5 V)

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max.	Unit
T_{PHL}	Propagation Delay Time to Logic LOW	T_A = 25°C, R_L = 4.1 kΩ, I_F = 16 mA (Note 2) (Fig. 9)	HCPL0500		0.45	1.5	μs
		R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C (Note 3) (Fig. 9)	HCPL0453		0.45	0.8	
			HCPL0501/0531/4				
		R_L = 4.1 kΩ, I_F = 16 mA (Note 2) (Fig. 9)	HCPL0500			2.0	
		R_L = 1.9 kΩ, I_F = 16 mA (Note 3) (Fig. 9)	HCPL0453			1.0	
			HCPL0501/0531/4				
T_{PLH}	Propagation Delay Time to Logic HIGH	T_A = 25°C, R_L = 4.1 kΩ, I_F = 16 mA (Note 2) (Fig. 9)	HCPL0500		0.5	1.5	μs
		R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C (Note 3) (Fig. 9)	HCPL0453		0.3	0.8	
			HCPL0501/0531/4				
		R_L = 4.1 kΩ, I_F = 16 mA (Note 2) (Fig. 9)	HCPL0500			2.0	
		R_L = 1.9 kΩ, I_F = 16 mA (Note 3) (Fig. 9)	HCPL0453			1.0	
			HCPL0501/0531/4				
$\|CM_H\|$	Common Mode Transient Immunity at Logic HIGH	I_F = 0 mA, V_{CM} = 10 V_{P-P}, R_L = 4.1 kΩ, T_A = 25°C (Note 4) (Fig. 10)	HCPL0500	1,000	10,000		V/μs
		I_F = 0 mA, V_{CM} = 10 V_{P-P}, R_L = 1.9 kΩ T_A = 25°C (Note 4) (Fig. 10)	HCPL0501/31	1,000	10,000		
			HCPL0534	15,000	40,000		
		I_F = 0 mA, V_{CM} = 1500 V_{P-P}, R_L = 1.9 kΩ, T_A = 25°C (Note 4) (Fig. 10)	HCPL0453	15,000	40,000		
$\|CM_L\|$	Common Mode Transient Immunity at Logic LOW	I_F = 16 mA, V_{CM} = 10 V_{P-P}, R_L = 4.1 kΩ, T_A = 25°C (Note 4) (Fig. 10)	HCPL0500	1,000	10,000		V/μs
		I_F = 16 mA, V_{CM} = 10 V_{P-P}, R_L = 1.9 kΩ (Note 4) (Fig. 10)	HCPL0501/31	1,000	10,000		
			HCPL0534	15,000	40,000		
		I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}, R_L = 1.9 kΩ (Note 4) (Fig. 10)	HCPL0453	15,000	40,000		

ISOLATION CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
V_{ISO}	Input−Output Isolation Voltage	f = 60 Hz, t = 1.0 min., $I_{I-O} \le 2$ μA (Notes 5, 6)	2500			Vac_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500V (Note 5)	10^{11}			
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, f = 1.0MHz (Note 5)		0.2		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*All typicals at T_A = 25°C

1. Current Transfer Ratio is designed as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull−up resistor.
3. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull−up resistor.
4. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8 V).
5. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
6. 2500 VAC RMS for 1 minute duration is equivalent to 3000 VAC RMS for 1 second duration.

TYPICAL PERFORMANCE CURVES

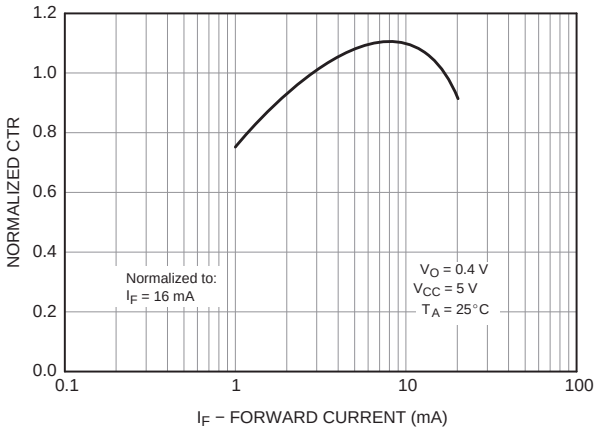


Figure 3. Normalized CTR vs. Forward Current

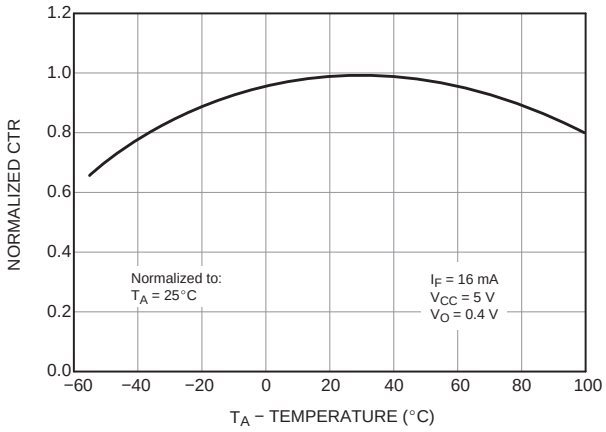


Figure 4. Normalized CTR vs. Temperature

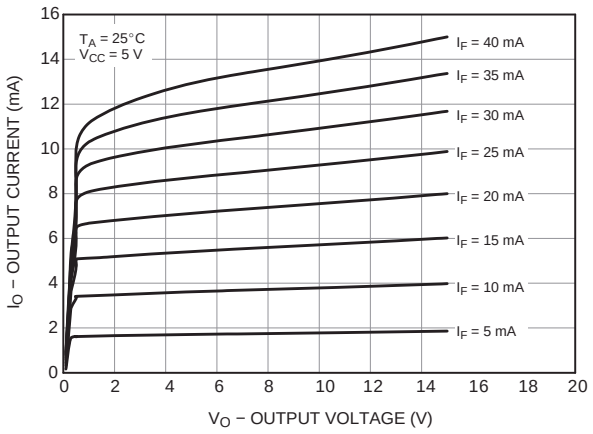


Figure 5. Output Current vs. Output Voltage

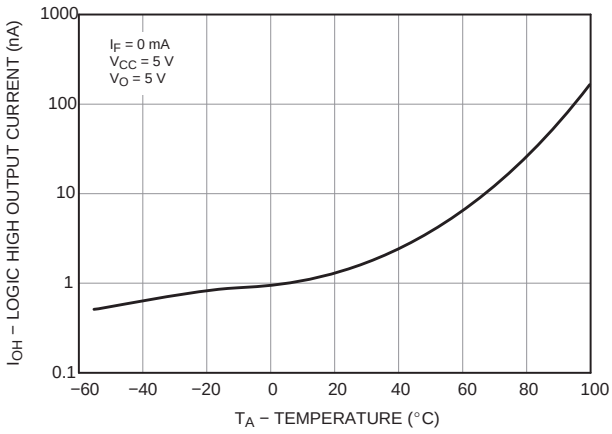


Figure 6. Logic High Output Current vs. Temperature

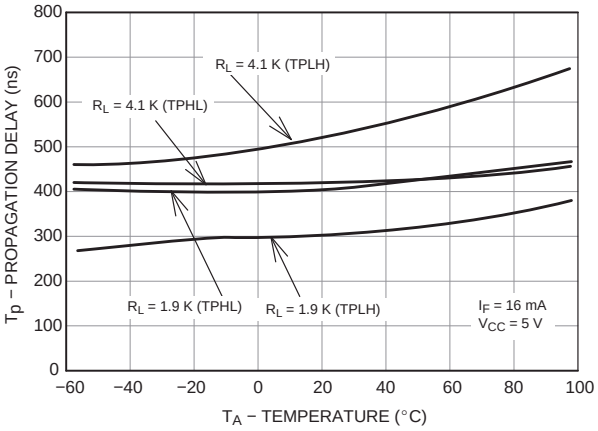


Figure 7. Propagation Delay vs. Temperature

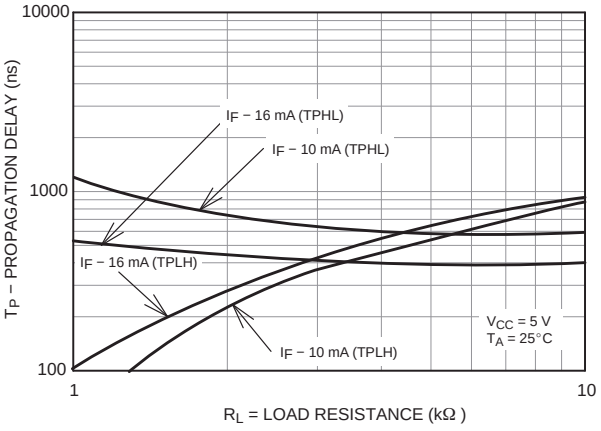
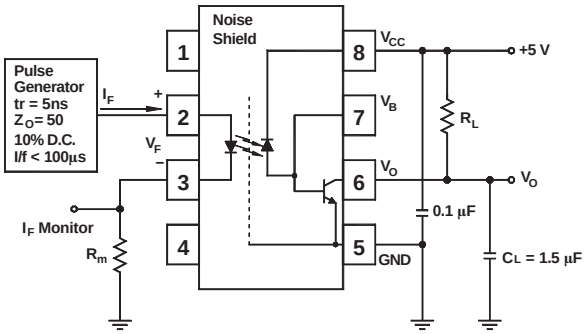
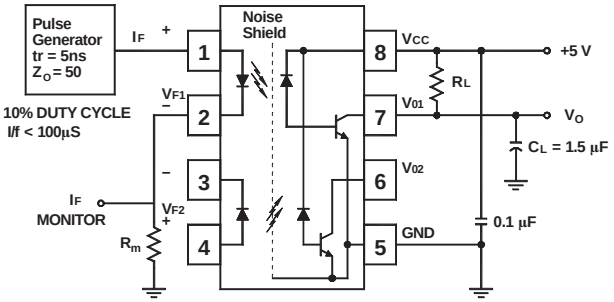


Figure 8. Propagation Delay vs. Load Resistance



Test Circuit for HCPL0453, HCPL0500 and HCPL0501



Test Circuit for HCPL0531 and HCPL0534

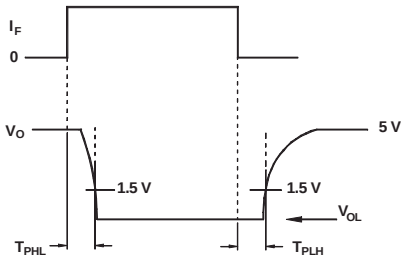
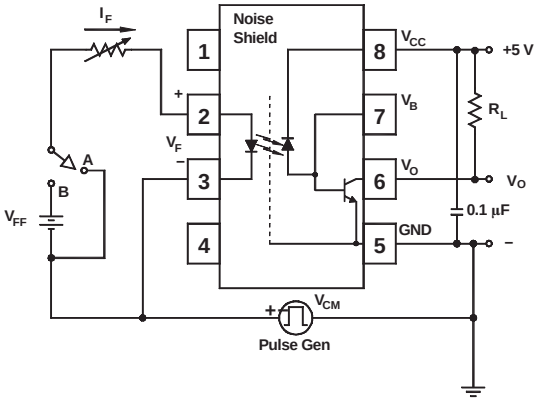
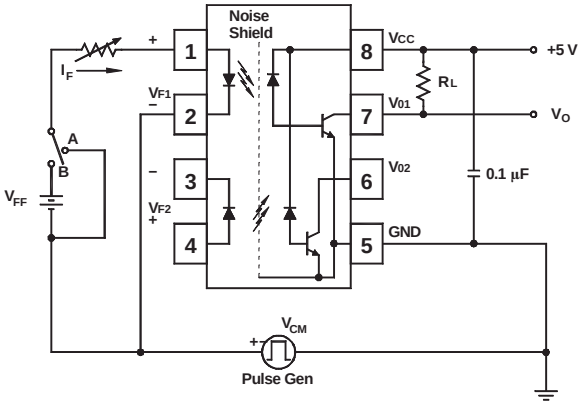


Figure 9. Switching Time Test Circuit



Test Circuit for HCPL0453, HCPL0500 and HCPL0501



Test Circuit for HCPL0531 and HCPL0534

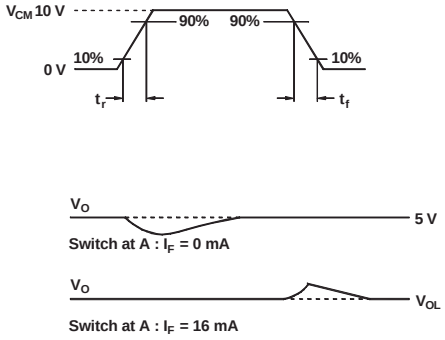


Figure 10. Common Mode Immunity Test Circuit

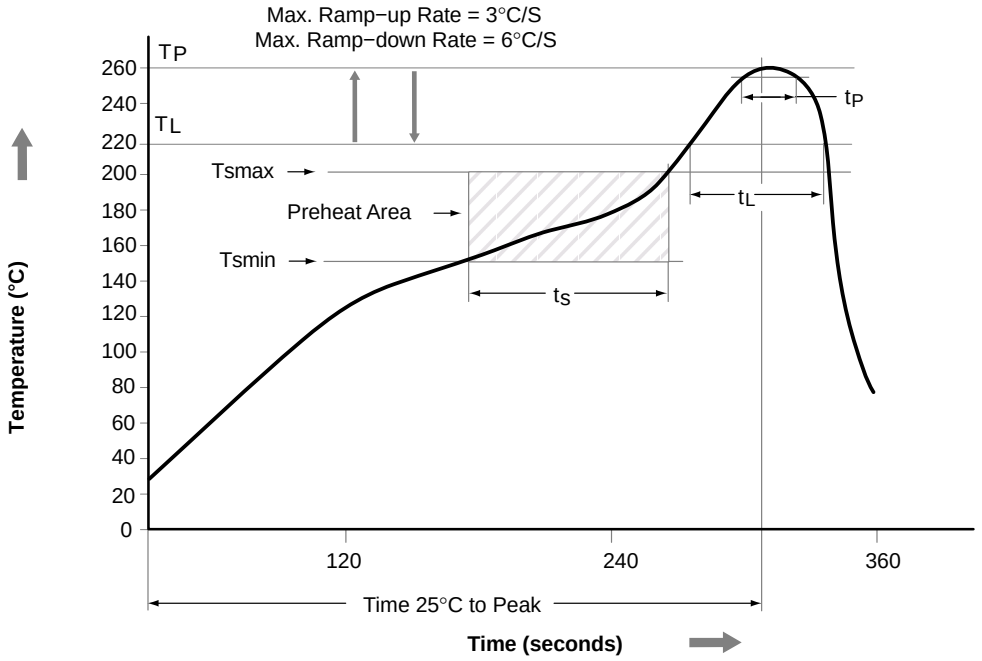
ORDERING INFORMATION

Part Nr./ Option (Note 7)	Order Entry Identifier	Package	Description	Packing Method†
HCPL0xxx**V**	V	SOIC8	VDE 0884 (approval pending for HCPL0531 & HCPL0534)	Tube (3000 Units)
HCPL0xxx**R2**	R2	SOIC8		Tape and Reel (2500 Units)
HCPL0xxx**R2V**	R2V	SOIC8	VDE 0884 (approval pending for HCPL0531 & HCPL0534)	Tape and Reel (2500 Units)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. The product orderable part number system listed in this table also applies to the HCPL0453, HCPL0500, HCPL0501, HCPL0531 and HCPL0534 product.

REFLOW PROFILE



Profile Freature	Pb−Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp−up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp−down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

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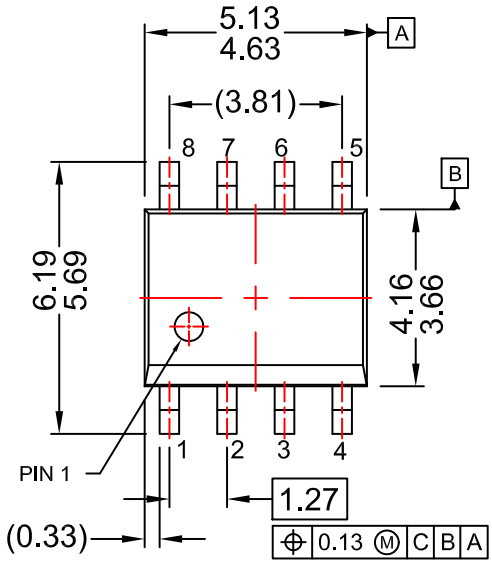
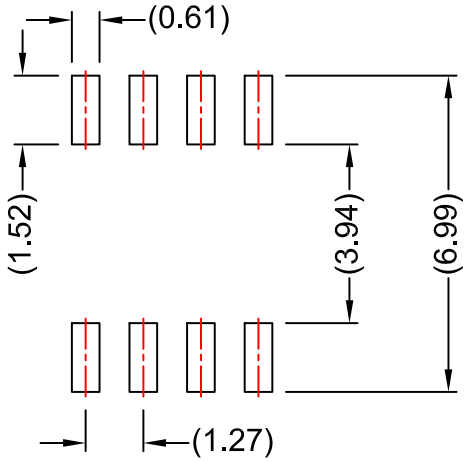
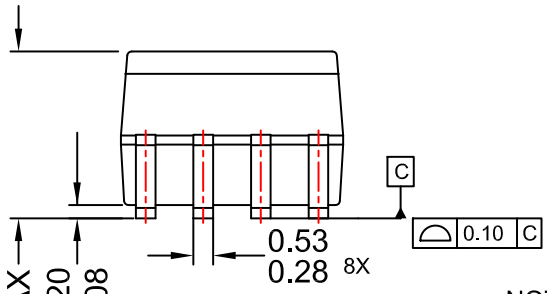
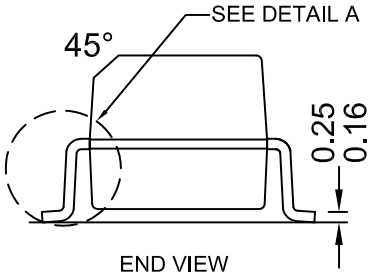


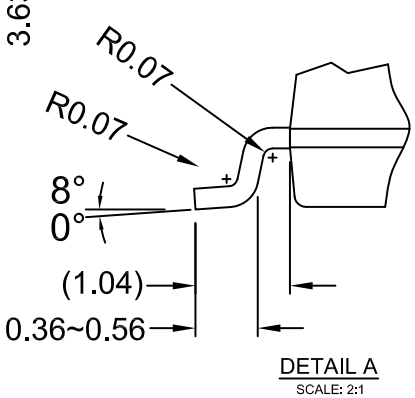


LAND PATTERN RECOMMENDATION





END VIEW



DETAIL A
SCALE: 2:1

NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.

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DESCRIPTION:	**SOIC8**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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