

P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
- 100	0.100 at V _{GS} = - 10 V	- 16	11.7			
- 100	0.120 at V _{GS} = - 4.5 V	- 15	11.7			

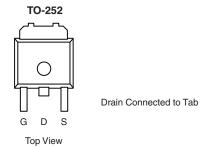
FEATURES

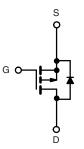
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_q and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- · Power Switch
- DC/DC Converters





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_C = 25 ^{\circ}C$, unless oth	erwise noted		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 100	V	
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 25 °C	L	- 16	
Continuous Diam Current (1) = 150 C)	T _C = 70 °C	I _D	- 14	
Pulsed Drain Current	I _{DM}	- 50	A	
Avalanche Current		I _{AS}	- 18	
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	16.2	mJ
M	T _C = 25 °C	В	32.1 ^b	10/
Maximum Power Dissipation ^a	T _A = 25 °C ^c	$ P_D$	2.5	W
Operating Junction and Storage Temperature Ra	nge	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	50	°C/W		
Junction-to-Case (Drain)	R _{thJC}	3.9	C/VV		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{DS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	- 100			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 2.5	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA
		V _{DS} = - 100 V, V _{GS} = 0 V			- 1	μА
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 100 V, V _{GS} = 0 V, T _J = 125 °C			- 50	
		V _{DS} = - 100 V, V _{GS} = 0 V, T _J = 150 °C			- 250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -10 \text{ V}, V_{GS} = -10 \text{ V}$	- 15			Α
	<u> </u>	V _{GS} = - 10 V, I _D = - 3.6 A		0.100		Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 3.4 A		0.120		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 3.6 A		12		S
Dynamic ^b	<u> </u>					
Input Capacitance	C _{iss}			1055		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V, V _{DS} = - 50 V, f = 1 MHz		65		
Reverse Transfer Capacitance	C _{rss}	1 "		41		
·		V _{DS} = - 50 V, V _{GS} = - 10 V, I _D = - 3.6 A		23.2	34.8	
Total Gate Charge ^c				11.7	17.6	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = -50 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -3.6 \text{ A}$		3.5		
Gate-Drain Charge ^c	Q _{gd}	1		4.8		
Gate Resistance	Rg	f = 1 MHz	1.2	5.7	11.5	Ω
Turn-On Delay Time ^c	t _{d(on)}			7	14	
Rise Time ^c	t _r	V _{DD} = - 50 V, R _I = 17.2 Ω		12	18	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong -2.9 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		33	50	ns ns
Fall Time ^c	t _f	1		9	18	
Drain-Source Body Diode Ratings ar	nd Character	stics T _C = 25 °C ^b				
Continuous Current	I _S	-			- 8.8	
Pulsed Current	I _{SM}				- 15	Α
Forward Voltage ^a	V _{SD}	I _F = - 2.9 A, V _{GS} = 0 V		- 0.8	- 1.5	V
Reverse Recovery Time	t _{rr}			50	75	ns
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = - 2.9 A, dl/dt = 100 A/μs		- 4	- 6	A
Reverse Recovery Charge	Q _{rr}	- · · · · · · · · · · · · · · · · · · ·		98	147	nC

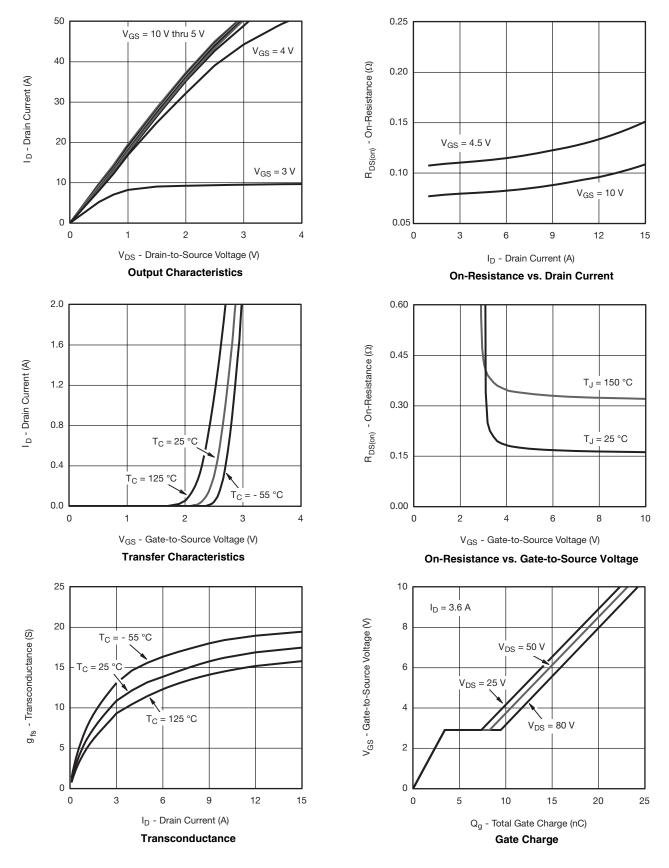
Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

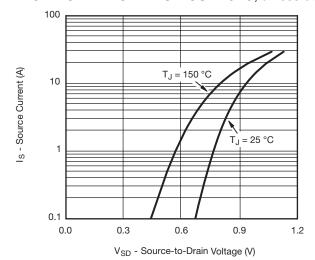


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

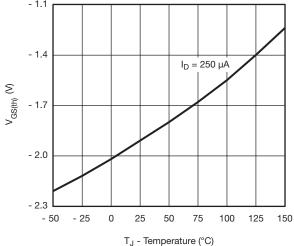




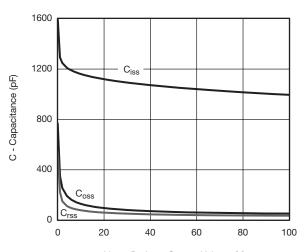
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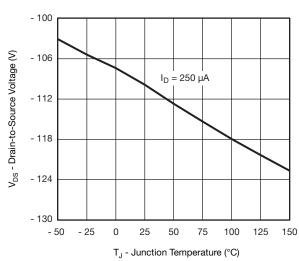
Source-Drain Diode Forward Voltage



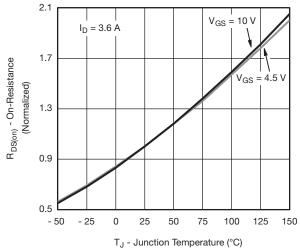
Threshold Voltage



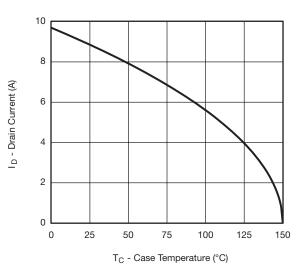
 V_{DS} - Drain-to-Source Voltage (V) $\label{eq:capacitance}$



Drain Source Breakdown vs. Junction Temperature



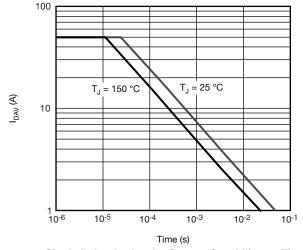
On-Resistance vs. Junction Temperature

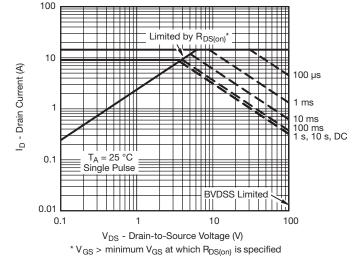


Current Derating

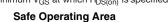


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

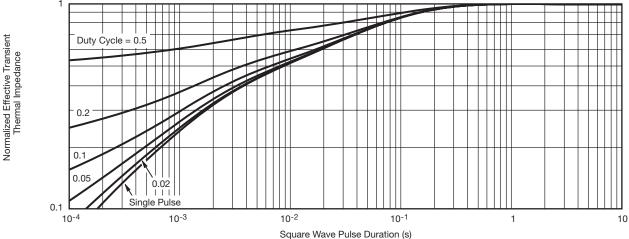




Single Pulse Avalanche Current Capability vs. Time



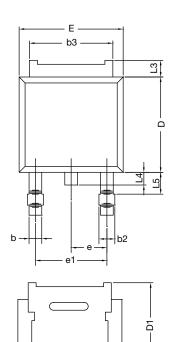


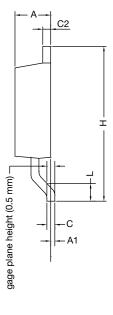


Normalized Thermal Transient Impedance, Junction-to-Case



TO-252AA Case Outline





	MILLIN	METERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28 BSC		0.090 BSC		
e1	4.56	BSC	0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T16-0236-Rev. P, 16-May-16					

ECN: T16-0236-Rev. P, 16-May-1

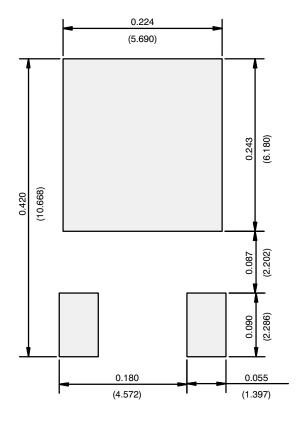
DWG: 5347

Notes

• Dimension L3 is for reference only.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)



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