

## N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY							
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)				
<u></u>	0.076 at V <sub>GS</sub> = 10 V	5.5	29 nC				
60	0.088 at V <sub>GS</sub> = 4.5 V	4.5	29110				

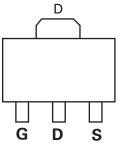
#### **FEATURES**

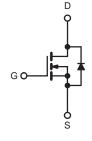
- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET

#### APPLICATIONS

· Load Switches for Portable Devices







N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_A = 25 \text{ °C}$ , unless otherwise noted							
Parameter		Symbol	Limit	Unit			
Drain-Source Voltage		V <sub>DS</sub>	60	V			
Gate-Source Voltage		V <sub>GS</sub>	± 20				
	T <sub>C</sub> = 25 °C		5.5 <sup>a</sup>				
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C		4 <sup>a</sup>				
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	4.7 <sup>a, b, c</sup>				
	T <sub>A</sub> = 70 °C		4 <sup>a, b, c</sup>	A			
Pulsed Drain Current	·	I <sub>DM</sub>	20				
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	5.2				
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	'5	5.1 <sup>b, c</sup>				
	T <sub>C</sub> = 25 °C		5.3				
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	4	w			
	T <sub>A</sub> = 25 °C	' U	2.5 <sup>b, c</sup>	v			
	T <sub>A</sub> = 70 °C	]	1.6 <sup>b, c</sup>				
Operating Junction and Storage Temperatur	e Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C			
Soldering Recommendations (Peak Temperation	ature) <sup>e, f</sup>		260				

#### THERMAL RESISTANCE BATINGS

Parameter	Symbol Typical		Maximum	Unit					
Maximum Junction-to-Ambient <sup>a, c, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	40	50	°C/W				
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	15	20	0/11				

Notes:

a. Package limited, T<sub>C</sub> = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 95 °C/W.

e. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

<b>SPECIFICATIONS</b> $T_J = 25 \text{ °C}$ , Parameter	Symbol	Min.	Typ	Max.	Unit		
Static	Symbol	Test Conditions	IVIIII.	Тур.	IVIAX.	Unit	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 µA	60			V	
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>		00	25			
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 4.0		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \ \mu A$	1.5	4.0	3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 12 V$	1.5		± 100	nA	
Gale-Source Leakage	GSS	$V_{\rm DS} = 60 \text{ V}, \text{ V}_{\rm GS} = 0 \text{ V}$			± 100		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 V, V_{GS} = 4.5 V$	25			A	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.3 A		0.088		Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A		0.076			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.3 A		45		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			800			
Output Capacitance	C <sub>oss</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz		120		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			100			
Tatal Cata Channe	0	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 6.3 \text{ A}$		22	33	nC	
Total Gate Charge	Qg			10	15		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 6.3 A		2.5			
Gate-Drain Charge	Q <sub>gd</sub>			1.7			
Gate Resistance	Rg	f = 1 MHz		2.4		Ω	
Turn-on Delay Time	t <sub>d(on)</sub>			15	25	- ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 1.5 $\Omega$		10	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ 6.7 A, $\text{V}_\text{GEN}$ = 4.5 V, $\text{R}_\text{g}$ = 1 $\Omega$		35	55		
Fall Time	t <sub>f</sub>			12	20		
Turn-on Delay Time	t <sub>d(on)</sub>			10	15		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 1.5 $\Omega$		12	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong\text{6.7}$ A, $\text{V}_\text{GEN}$ = 10 V, $\text{R}_\text{g}$ = 1 $\Omega$		25	40		
Fall Time	t <sub>f</sub>			10	15	1	
Drain-Source Body Diode Characteristic	s					<b>I</b>	
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	T <sub>C</sub> = 25 °C			7.2	А	
Pulse Diode Forward Current	I <sub>SM</sub>				25	A	
Body Diode Voltage	V <sub>SD</sub>	$I_{S} = 6.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			20	40	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	L = 6.7  A  dV/dt = 100  A/vs T = 25.90		10	20	nC	
		I <sub>F</sub> = 6.7 A, dl/dt = 100 A/µs, T <sub>J</sub> = 25 °C		10			
Reverse Recovery Rise Time	t <sub>a</sub> t <sub>b</sub>			10		ns	

Notes:

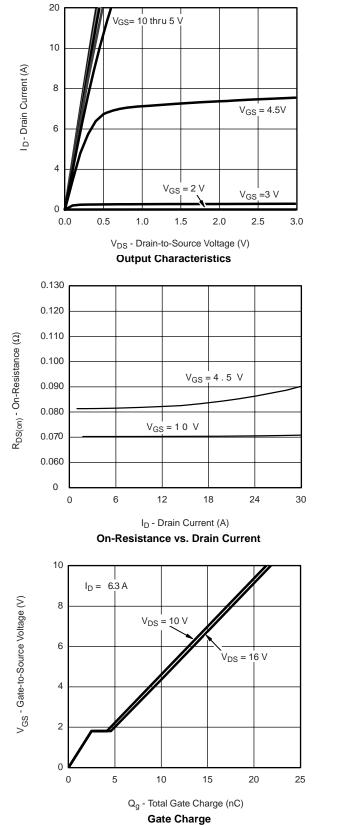
a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing.

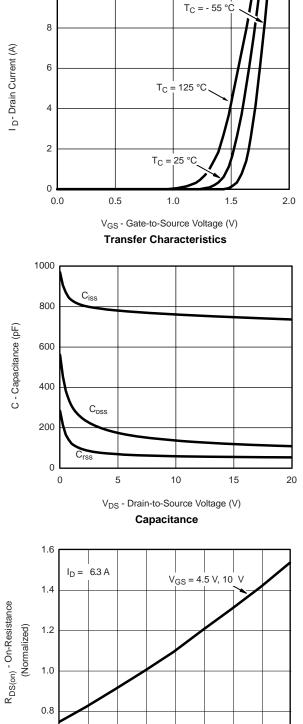
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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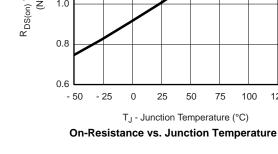




#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



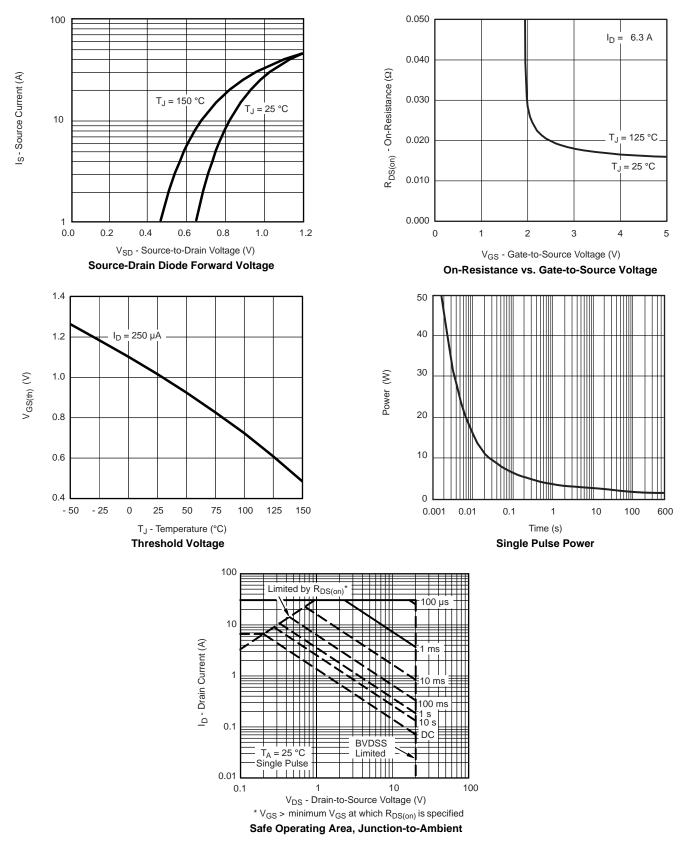
10



150

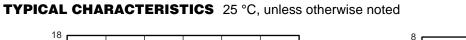
125

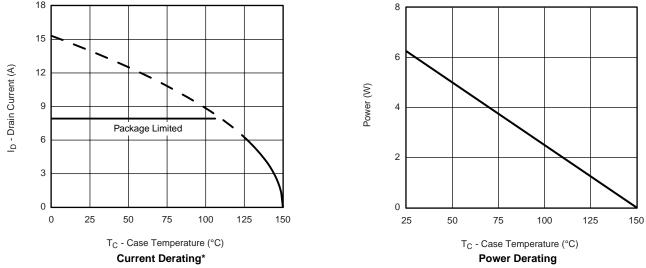




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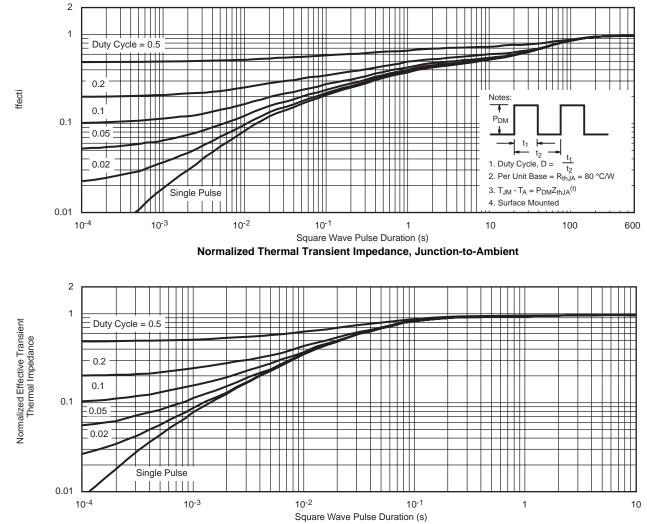






\* The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





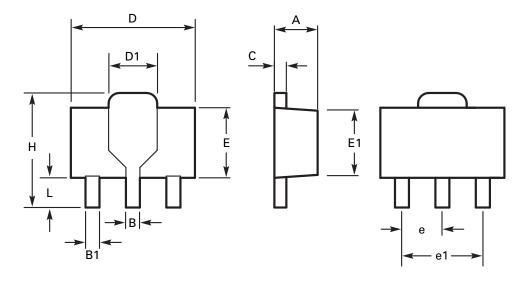
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## <u>K1273</u>



### Package outline - SOT89



DIM	Millim	neters	Inc	Inches DIM Millimeters Inch		Millimeters		hes	
	Min	Max	Min	Max		Min	Max	Min	Max
Α	1.40	1.60	0.550	0.630	E	2.29	2.60	0.090	0.102
В	0.44	0.56	0.017	0.022	E1	2.13	2.29	0.084	0.090
B1	0.36	0.48	0.014	0.019	е	1.50 BSC		0.059 BSC	
С	0.35	0.44	0.014	0.017	e1	3.00 BSC		0.118 BSC	
D	4.40	4.60	0.173	0.181	Н	3.94	4.25	0.155	0.167
D1	1.62	1.83	0.064	0.072	L	0.89	1.20	0.035	0.047

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches



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