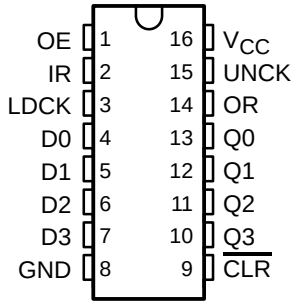
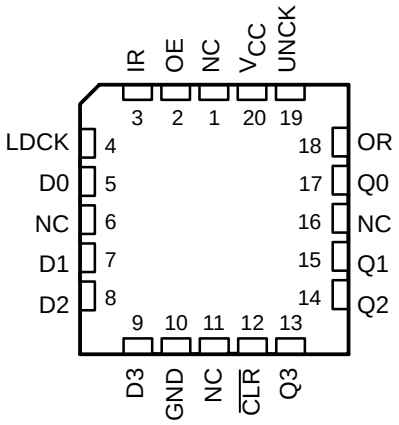
- **Independent Synchronous Inputs and Outputs**
- **16 Words by 4 Bits Each**
- **3-State Outputs Drive Bus Lines Directly**
- **Data Rates up to 10 MHz**
- **Fall-Through Time 50 ns Typical**
- **Data Terminals Arranged for Printed Circuit Board Layout**
- **Expandable, Using External Gating**
- **Packaged in Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Chip Carriers (FK)**

SN54LS224A . . . J PACKAGE
SN74LS224A . . . N PACKAGE
(TOP VIEW)



SN54LS224A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54LS224A and SN74LS224A 64-bit, low-power Schottky memories are organized as 16 words by 4 bits each. They can be expanded in multiples of 15m + 1 words or 4n bits, or both (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array); however, some external gating is required. For longer words, the input-ready (IR) signals of the first-rank packages and output-ready (OR) signals of the last-rank packages must be ANDed for proper synchronization.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written to and read from its array at independent data rates. These FIFOs are designed to process data at rates up to 10 MHz in a bit-parallel format, word by word.

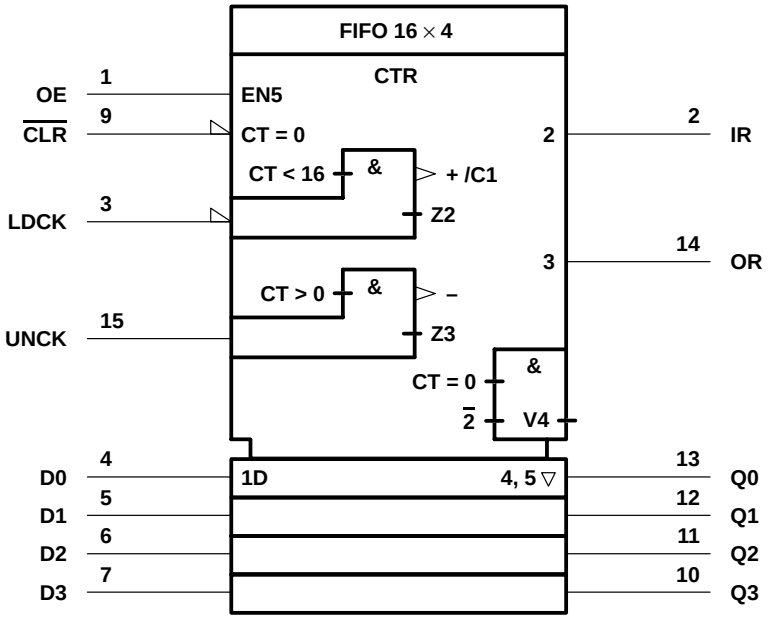
The load clock (LDCK) normally is held low, and data is written into memory on the high-to-low transition of LDCK. The unload clock (UNCK) normally is held high, and data is read out on the low-to-high transition of UNCK. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the IR and OR flags that indicate not-full and not-empty conditions. IR is high only when the memory is not full and LDCK is low. OR is high only when the memory is not empty and UNCK is high.

A low level on the clear ($\overline{\text{CLR}}$) input resets the internal stack-control pointers and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting, with respect to the data inputs, and are at high impedance when the output-enable (OE) input is low. OE does not affect the IR and OR outputs.

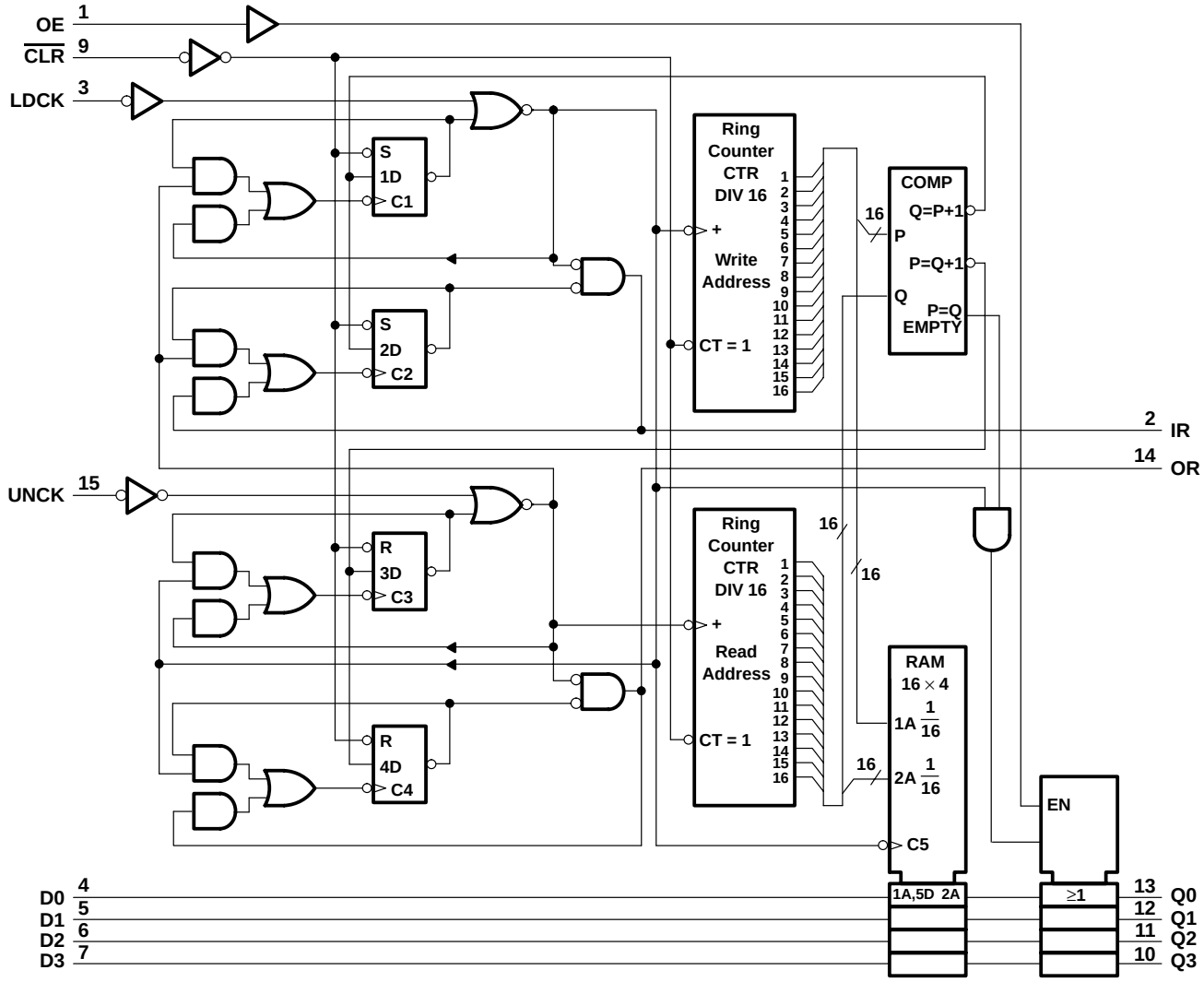
The SN74LS224A is characterized for operation from 0°C to 70°C. The SN54LS224A is characterized over the full military temperature range of –55°C to 125°C.

logic symbol†



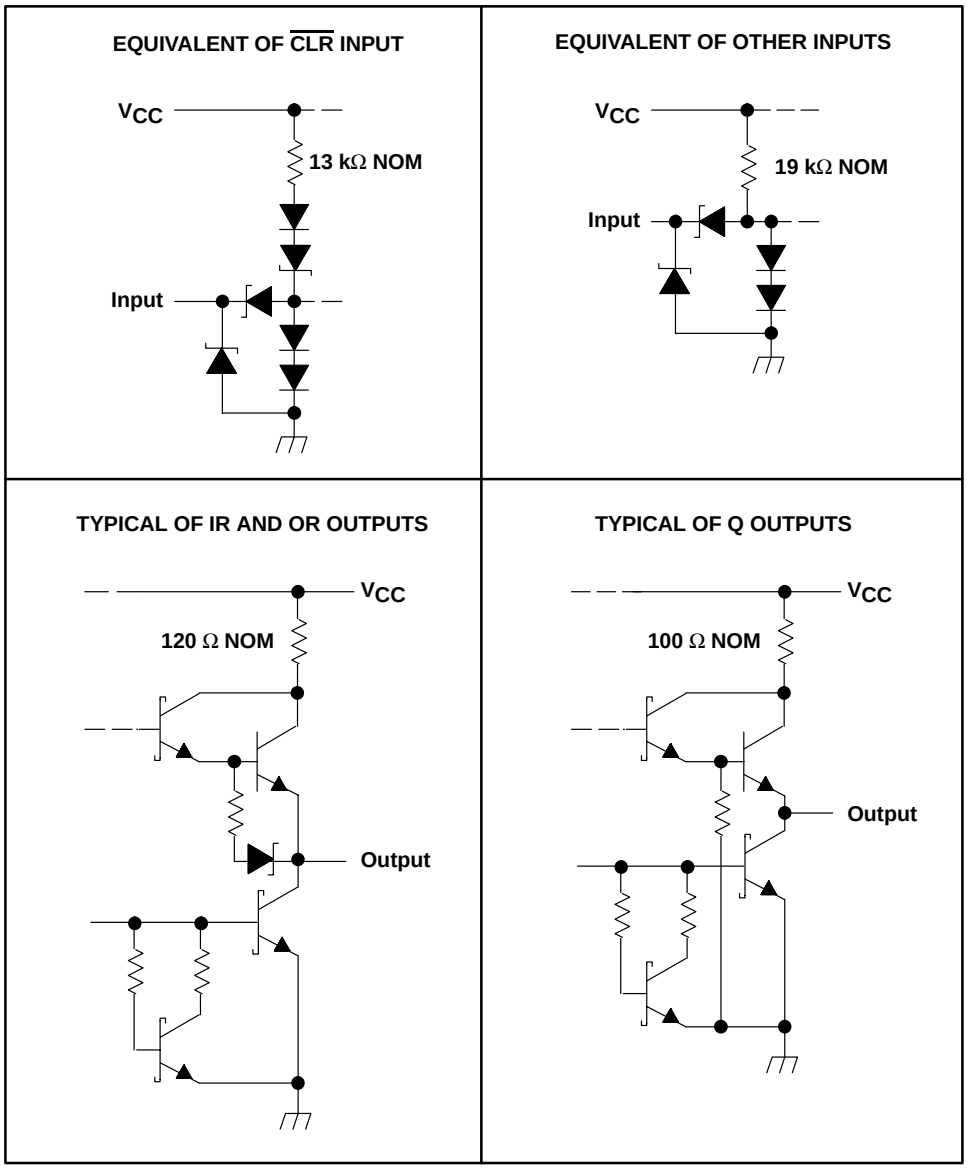
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. This symbol is functionally accurate, but does not show the details of implementation; for these details, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.
Pin numbers shown are for the J and N packages.

logic diagram (positive logic)

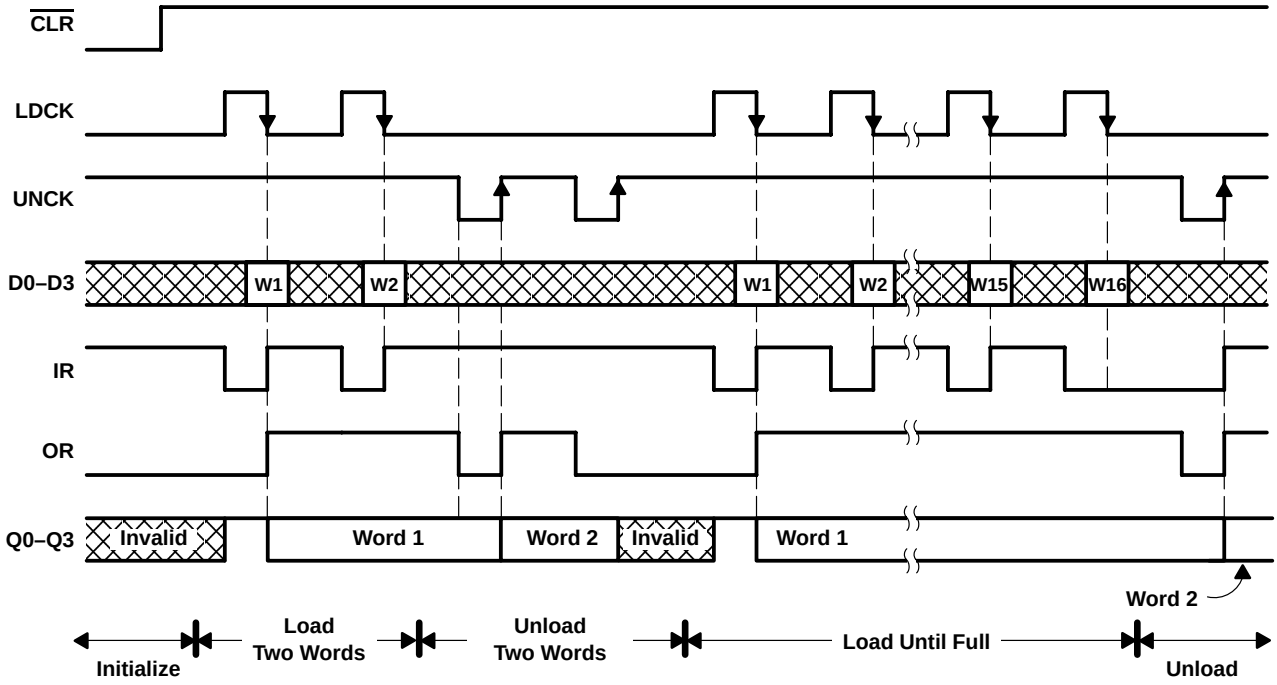


Pin numbers shown are for the J and N packages.

schematics of inputs and outputs



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Off-state output voltage range, V_O . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA}: N package (see Note 2) . . . . . 67°C/W
N package (see Note 3) . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-3.

recommended operating conditions (see Note 4)

			SN54LS224A			SN74LS224A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	Q outputs			–1			–2.6	mA
		IR, OR			–0.4			–0.4	
I_{OL}	Low-level output current	Q outputs			12			24	mA
		IR, OR			4			8	
T_A	Operating free-air temperature		–55		125	0		70	°C

NOTE 4: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS224A			SN74LS224A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	Q outputs	V_{CC} = MIN	I_{OH} = –2.6 mA				2.4	3.4		V
			I_{OH} = –1 μA	2.4	3.3					
	IR, OR	V_{CC} = MIN,	I_{OH} = –0.4 mA	2.5	3.4		2.7	3.4		
V_{OL}	Q outputs	V_{CC} = MIN	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
	IR, OR	V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Q outputs	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	Q outputs	V_{CC} = MAX,	V_O = 0.4 V			–20			–20	μA
I_I		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			–0.4			–0.4	mA
I_{OS}§	Q outputs	V_{CC} = MAX		–30		–130	–30		–130	mA
	IR, OR			–20		–100	–20		–100	
I_{CC}		V_{CC} = MAX	Outputs high		84	135		84	135	mA
			Outputs low		87	155		87	155	
			Outputs disabled		89	155		89	155	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

timing requirements over recommended operating conditions (see Note 4 and Figure 1)

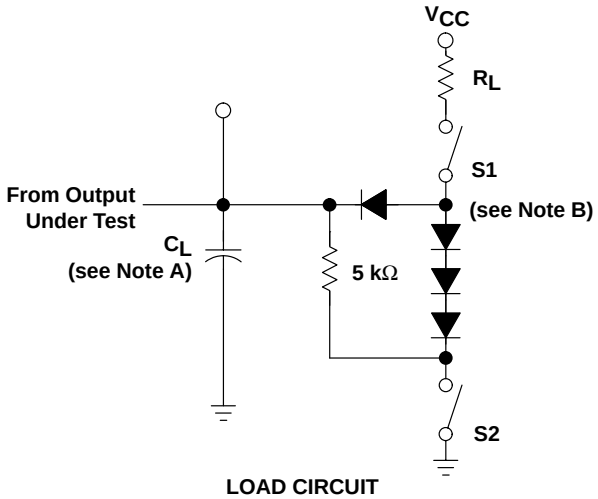
			SN54LS224A		SN74LS224A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	LDCK high	60		60		ns
		LDCK low	15		15		
		UNCK low	30		30		
		UNCK high	30		30		
		$\overline{CLR}$ low	20		20		
t_{su}	Setup time	Data to LDCK↓	50		50		ns
		LDCK↓ before UNCK↓	50		50		
		UNCK↑ before LDCK↑	50		50		
t_h	Hold time	Data from LDCK↓	10		10		ns

NOTE 4: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

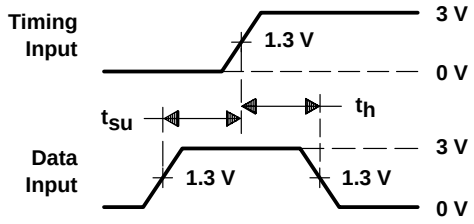
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	LDCK↓	IR	R_L = 2 kΩ, C_L = 15 pF		25	40	ns
t_{PHL}	LDCK↑				36	50	
t_{PLH}	LDCK↓	OR	R_L = 2 kΩ, C_L = 15 pF		48	70	ns
t_{PLH}	UNCK↑	OR	R_L = 2 kΩ, C_L = 15 pF		29	45	ns
t_{PHL}	UNCK↓				28	45	
t_{PLH}	UNCK↑	IR	R_L = 2 kΩ, C_L = 15 pF		49	70	ns
t_{PLH}	$\overline{CLR}$↓	IR	R_L = 2 kΩ, C_L = 15 pF		36	55	ns
t_{PHL}		OR			25	40	
t_{PHL}	LDCK↓	Q	R_L = 667 Ω, C_L = 45 pF		34	50	ns
t_{PLH}	UNCK↑	Q	R_L = 667 Ω, C_L = 45 pF		54	80	ns
t_{PHL}					45	70	
t_{PZL}	OE↑	Q	R_L = 667 Ω, C_L = 45 pF		22	35	ns
t_{PZH}					21	35	
t_{PLZ}	OE↓	Q	R_L = 667 Ω, C_L = 5 pF		16	30	ns
t_{PHZ}					18	30	

PARAMETER MEASUREMENT INFORMATION

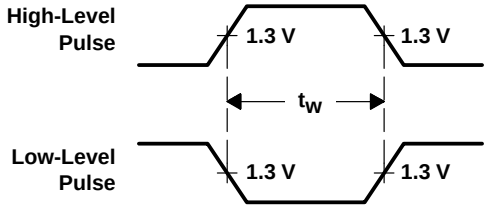


LOAD CIRCUIT

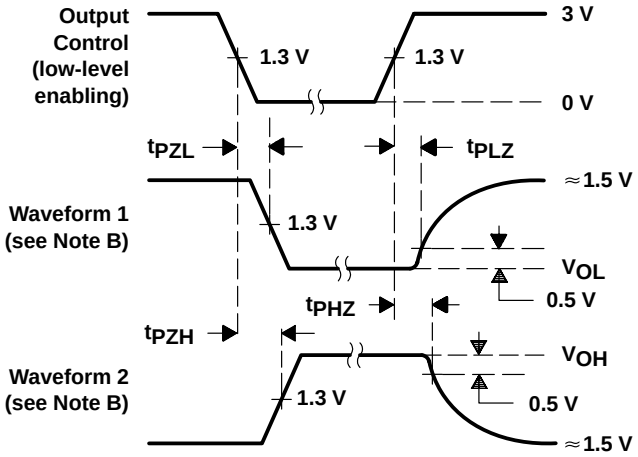
TEST	S1	S2
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed
t_{PLZ}/t_{PHZ}	Closed	Closed
t_{PLH}/t_{PHL}	Closed	Closed



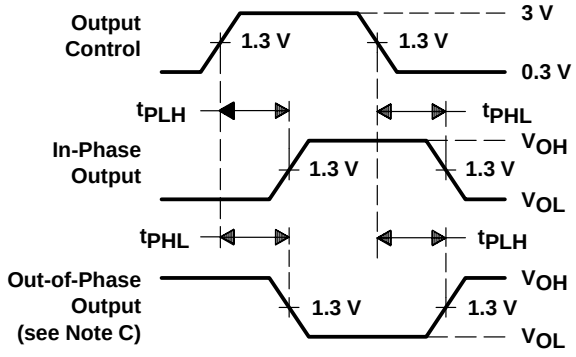
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r < 15 ns, t_f < 6 ns, Z_O ≈ 50 Ω.
D. All diodes are 1N916 or 1N3064.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN54LS224AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN74LS224AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS224AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SNJ54LS224AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS224AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF SN54LS224A, SN74LS224A :

- Catalog: SN74LS224A
- Military: SN54LS224A

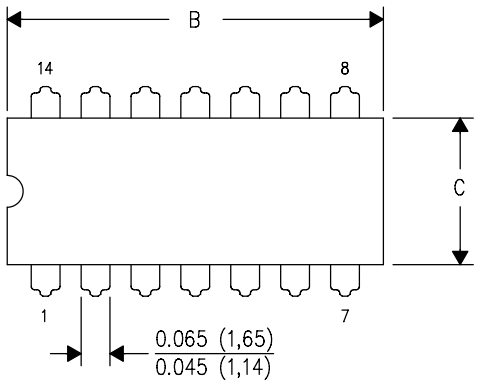
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

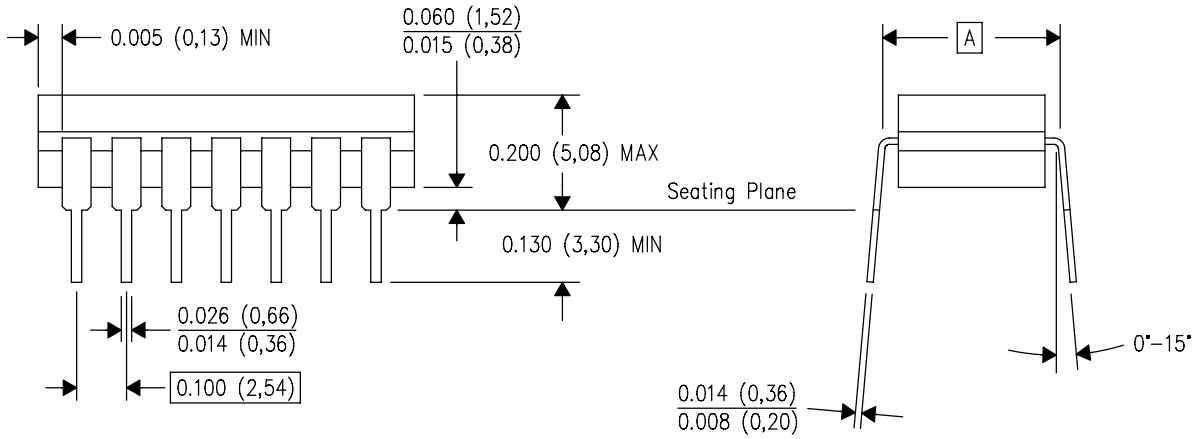
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

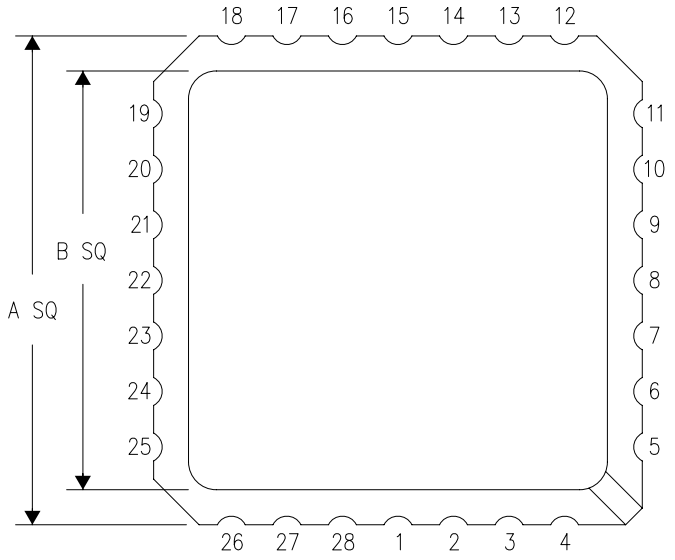


4040083/F 03/03

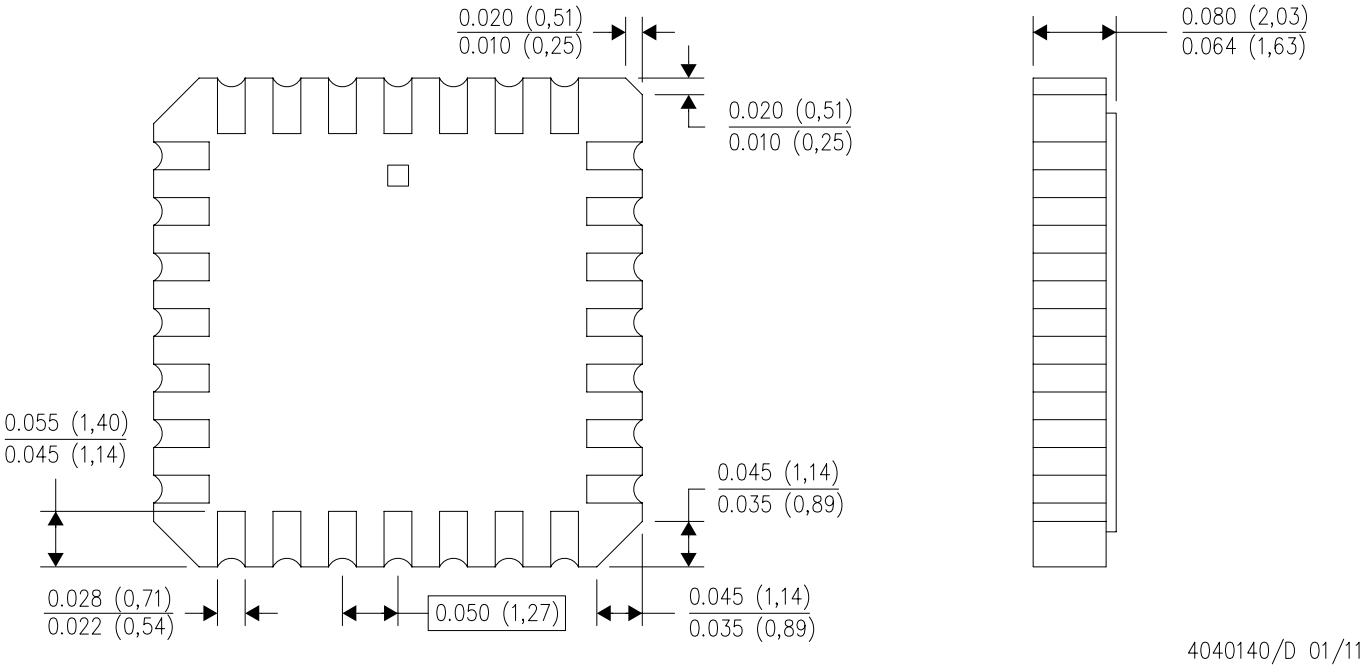
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



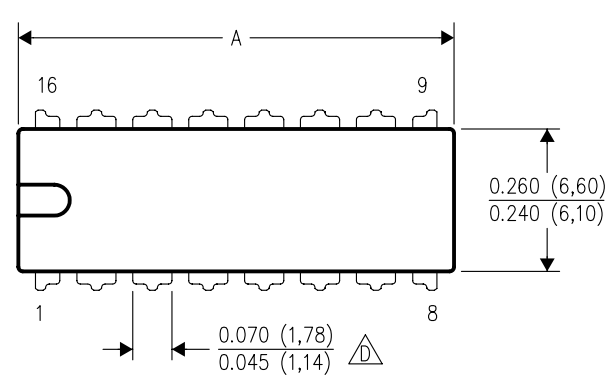
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

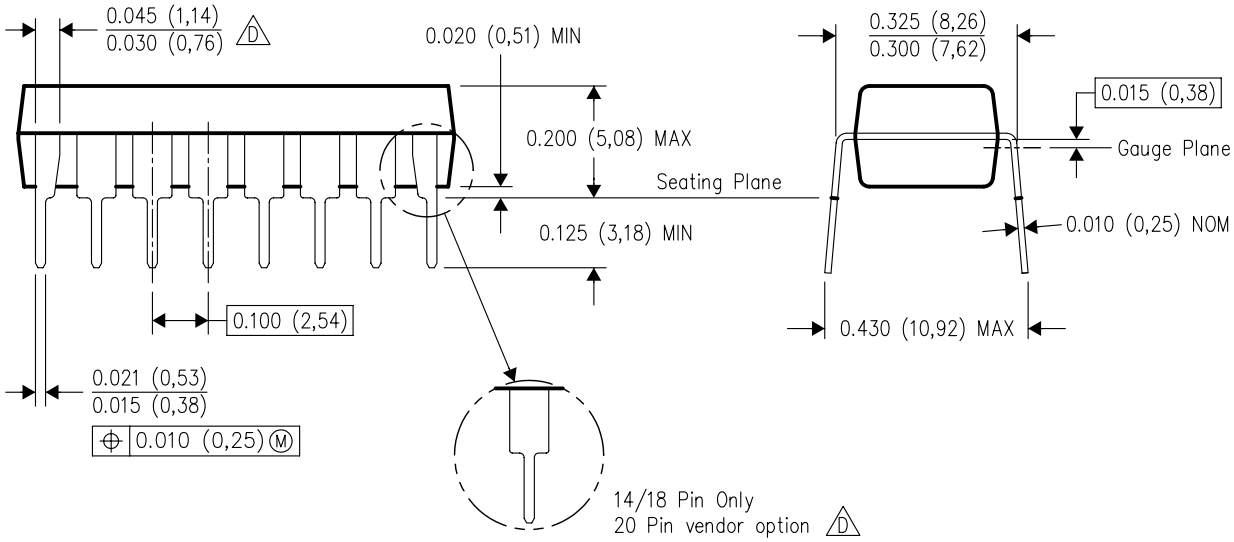
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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