- **Organization:**
  DRAM: 262144 Words × 16 Bits
  SAM: 256 Words × 16 Bits
- **Single 5.0-V Power Supply (±10%)**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and Serial-Address-Memory (SAM) Ports**
- **Write-per-Bit Function for Selective Write to Each I/O of the DRAM Port**
- **Byte-Write Function for Selective Write to Lower Byte (DQ0–DQ7) or Upper Byte (DQ8–DQ15) of the DRAM Port**
- **4-Column or 8-Column Block-Write Function for Fast Area-Fill Operations**
- **Enhanced Page Mode for Faster Access With Extended-Data-Output (EDO) Option for Faster System Cycle Time**
- **$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR) and Hidden Refresh Functions**
- **Long Refresh Period – Every 8 ms (Maximum)**
- **Full-Register-Transfer Function Transfers Data from the DRAM to the Serial Register**
- **Split-Register-Transfer Function Transfers Data from the DRAM to One-Half of the Serial Register While the Other Half is Outputing Data to the SAM Port**
- **256 Selectable Serial Register Starting Points**
- **Programmable Split-Register Stop Point**
- **Up to 55-MHz Uninterrupted Serial-Data Streams**
- **3-State Serial Outputs for Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Designed to Work With the Texas Instruments (TI™) Graphics Family**
- **Fabricated Using TI's Enhanced Performance Implanted CMOS (EPIC™) Process**

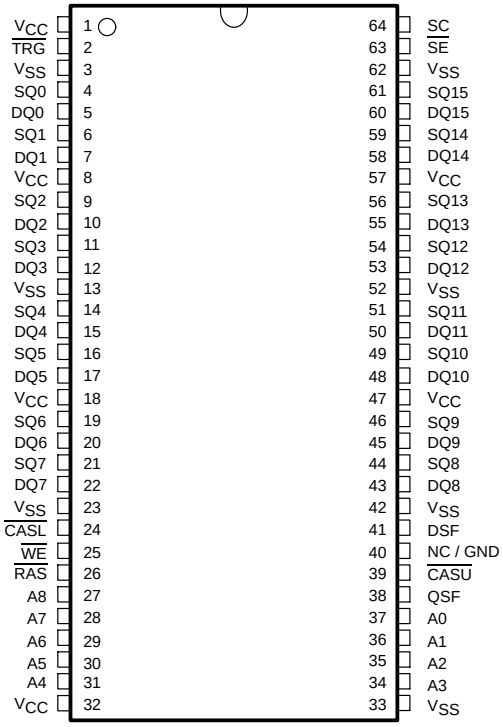
performance ranges

	ACCESS TIME ROW ENABLE t_{RAC} (MAX)	ACCESS TIME SERIAL DATA t_{SCA} (MIN)	DRAM PAGE CYCLE TIME t_{PC} (MIN)	DRAM EDO CYCLE TIME t_{PC} (MIN)	SERIAL CYCLE TIME t_{SCC} (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)
–60 Speed	60 ns	15 ns	35 ns	30 ns	18 ns	180 mA
–70 Speed	70 ns	20 ns	40 ns	30 ns	22 ns	165 mA

Table 1. Device Option Table

DEVICE	POWER SUPPLY VOLTAGE	BLOCK-WRITE CAPABILITY	PAGE/EDO OPERATION
55160	5.0 V ± 0.5 V	4-column	Page
55161	5.0 V ± 0.5 V	4-column	EDO
55170	5.0 V ± 0.5 V	8-column	Page
55171	5.0 V ± 0.5 V	8-column	EDO

DGH PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A8	Address Inputs
$\overline{RAS}$	Row-Address Strobe
$\overline{CASL}$, $\overline{CASU}$	Column-Address Strobe, Byte Select
DSF	Special-Function Select
$\overline{TRG}$	Output Enable, Transfer Select
$\overline{WE}$	Write Enable, Write Mask Select
DQ0 – DQ15	DRAM Data I/O
SC	Serial Clock
$\overline{SE}$	Serial Enable
SQ0 – SQ15	Serial Data Output
QSF	Special-Function Output
V_{CC}	Power Supply
V_{SS}	Ground
NC/GND	No Connect/Ground
	(Important: not connected internally to V_{SS})

description

The TMS551xx multiport video RAMs (VRAMs) are high-speed dual-ported memory devices. Each consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each interfaced to a serial-data register [serial-access memory (SAM)] organized as 256 words of 16 bits each. These devices support three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from the DRAM to the SAM. Except during transfer operations, these devices can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS551xx multiport VRAMs provide several functions designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports (see Table 2). On the DRAM port, greater pixel draw rates are achieved by the block-write function. The TMS5516x devices' 4-column block-write function allows 16 bits of data (present in an on-chip color-data register) to be written to any combination of four adjacent column-address locations, up to a total of 64 bits of data per $\overline{\text{CAS}}$x cycle time. Similarly, the TMS5517x devices' 8-column block-write function allows 16 bits of data to be written to any combination of eight adjacent column-address locations, up to a total of 128 bits of data per $\overline{\text{CAS}}$x cycle time. Also on the DRAM port, the write-per-bit (or write-mask) function allows masking of any combination of the 16 DQs on any write cycle. The persistent write-per-bit function uses a mask register that, once loaded, can be used on subsequent write cycles without reloading. All TMS551xx devices offer byte control. Byte control can be applied in write cycles, read cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The TMS551xx devices offer enhanced-page-mode operation that results in faster access time. The TMS551x1 devices also offer extended-data-output (EDO) mode. The EDO mode is effective in both the page-mode and the standard DRAM cycles.

The TMS551xx devices offer a split-register-transfer (DRAM to SAM) function. This feature enables real-time register load implementation for continuous serial-data streams without critical timing requirements. The serial register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the DRAM. For applications not requiring real-time register load (for example, loads done during CRT-retrace periods), the full-register-transfer operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 55 MHz. A separate output, QSF, is included to indicate which half of the serial register is active. Refreshing the SAM is not required because the data register that comprises the SAM is static.

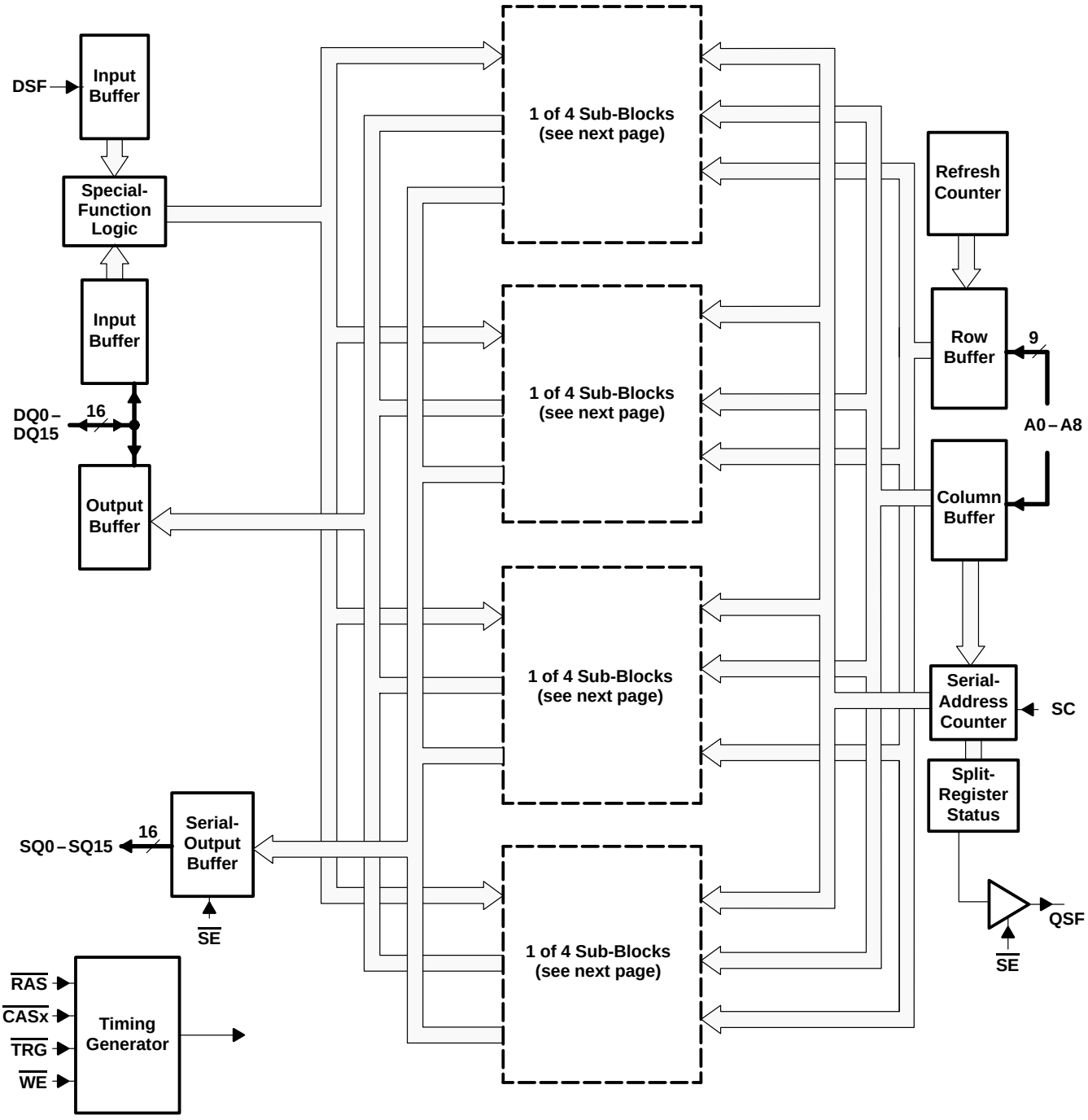
All inputs, outputs, and clock signals on the TMS551xx devices are compatible with Series 74 TTL. All address lines and data-in lines are latched on-chip to simplify system design. All data-out lines are unlatched to allow greater system flexibility.

All TMS551xx employ TI's state-of-the-art EPIC technology combining very high performance with improved reliability.

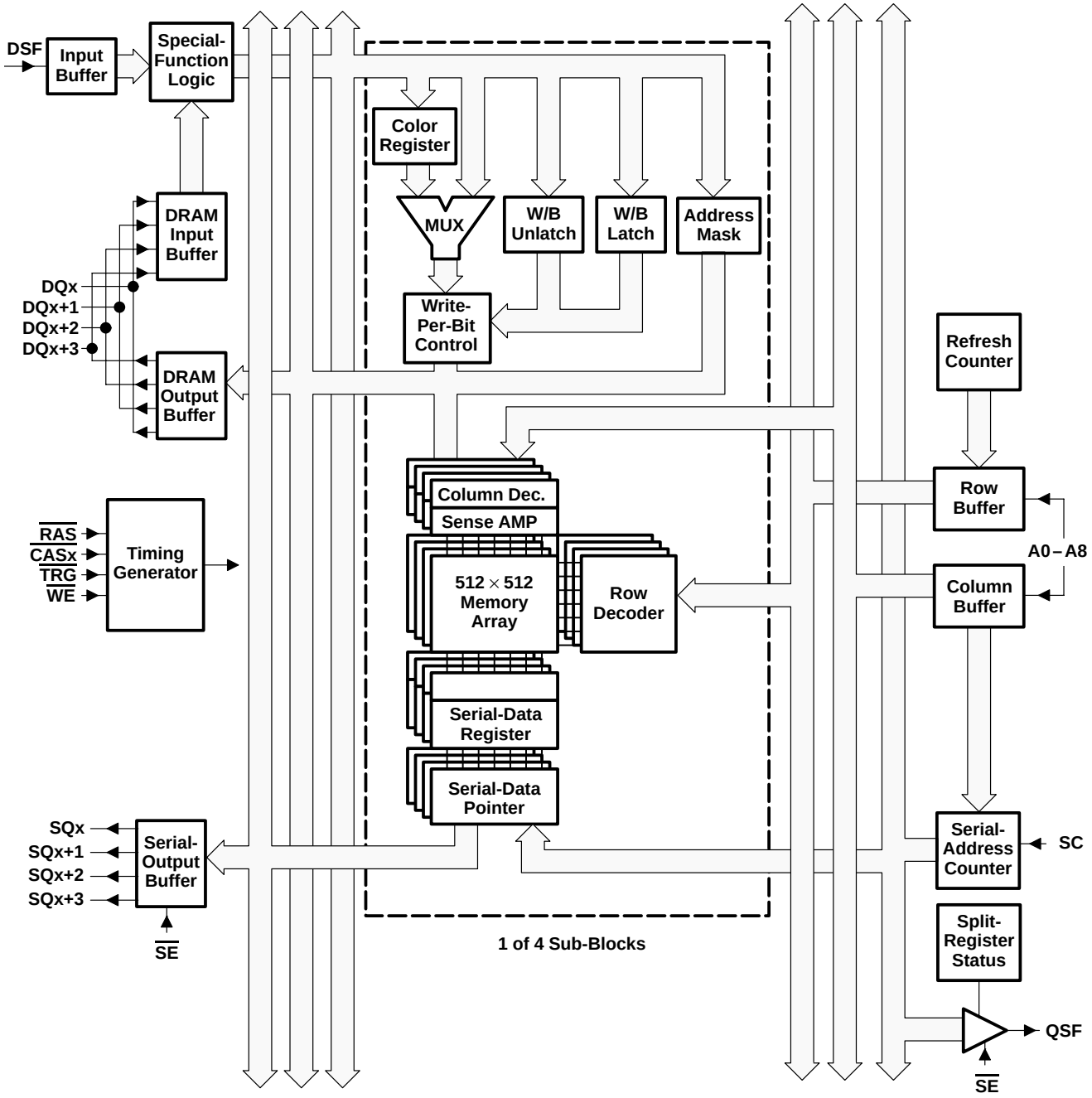
All TMS551xx are offered in a 64-pin small-outline gull-wing-leaded package (DGH suffix) for direct surface mounting.

The TMS551xx VRAMs and other TI multiport VRAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

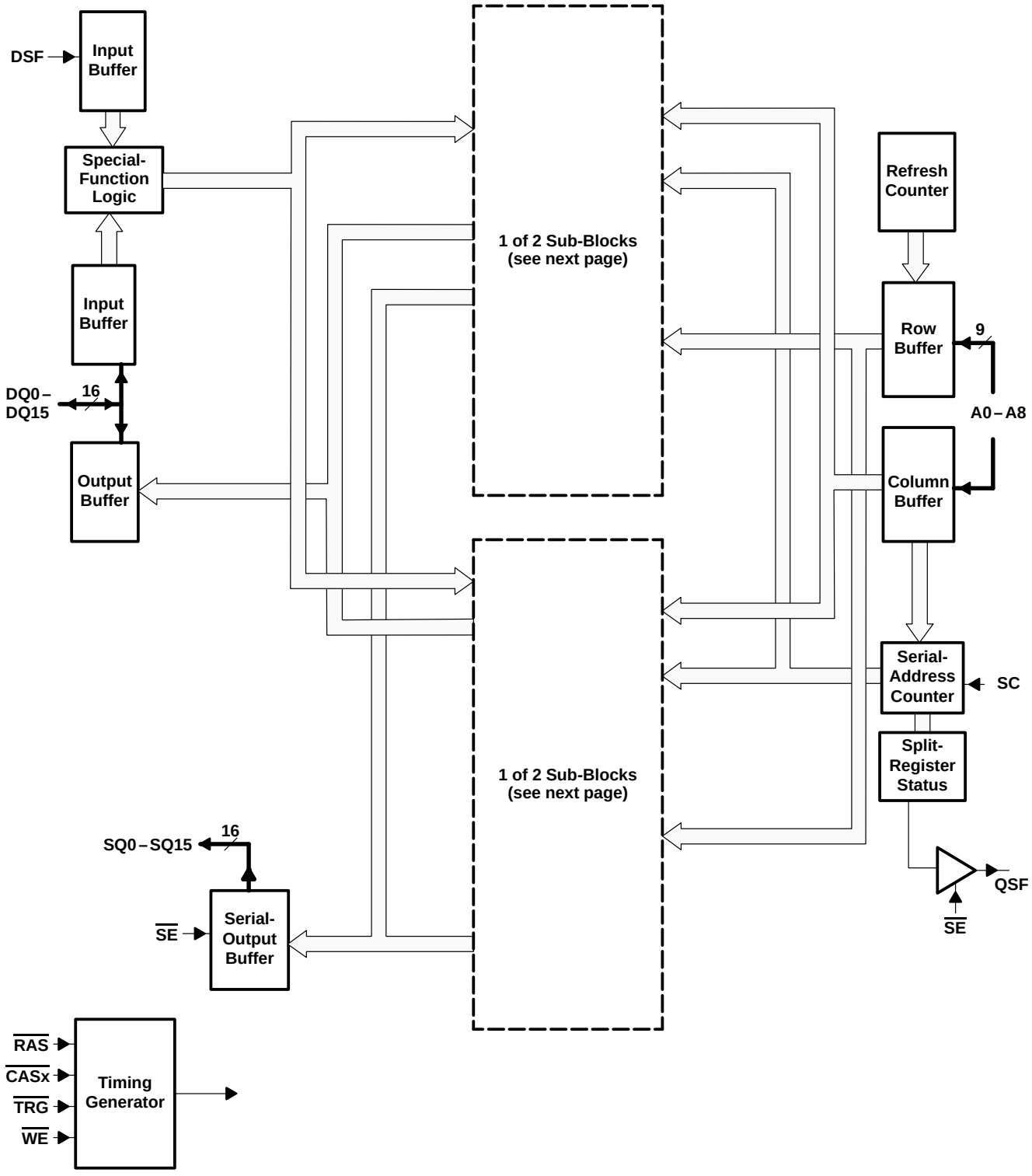
4-column functional block diagram (TMS5516x)



4-column functional block diagram (TMS5516x) (continued)



8-column functional block diagram (TMS5517x)



8-column functional block diagram (TMS5517x) (continued)

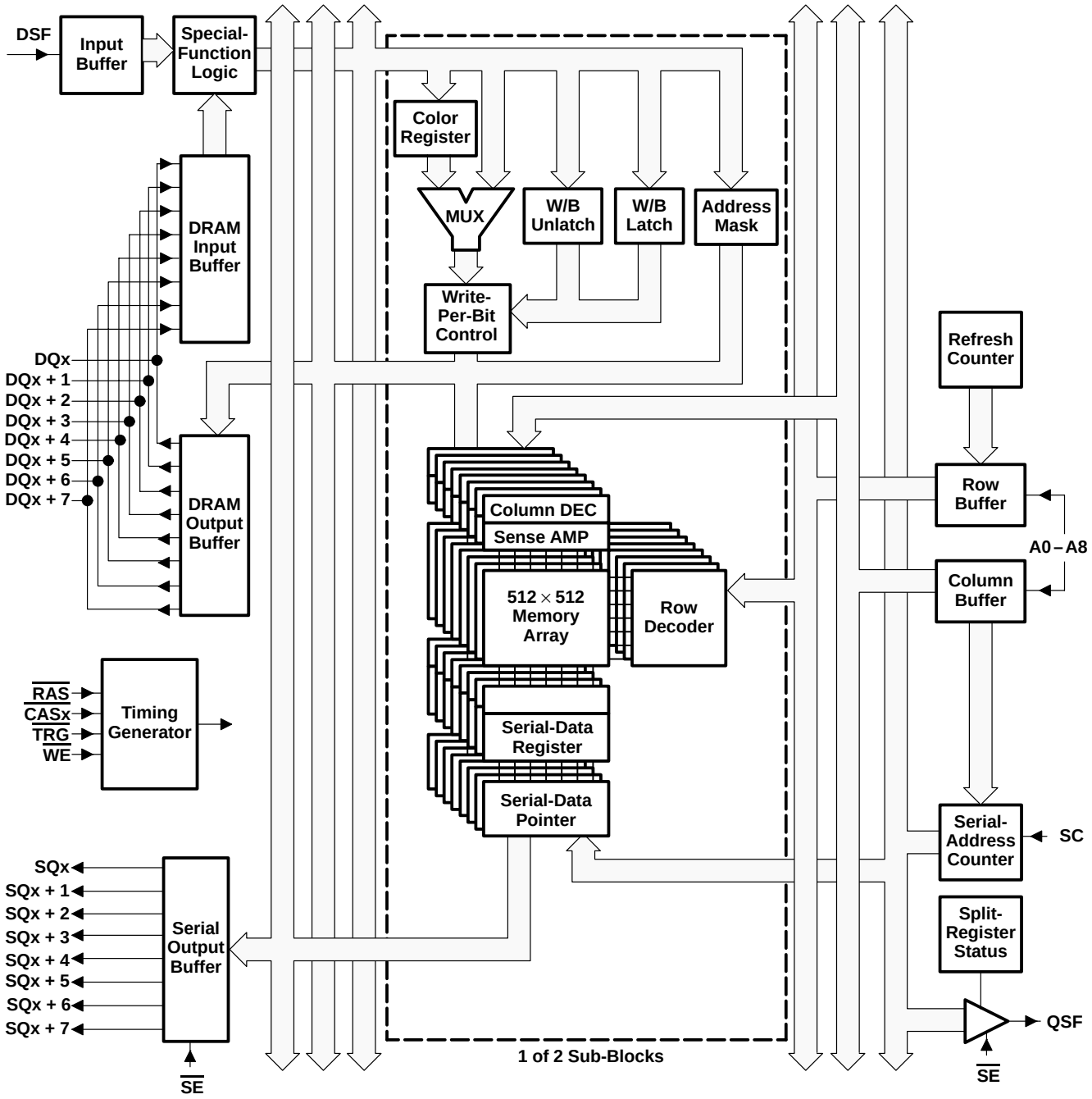


Table 2. Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0–DQ15†		MNEMONIC CODE
	$\overline{CASx}$‡	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$§	$\overline{RAS}$	$\overline{CASL}$ $\overline{CASU}$ $\overline{WE}$	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)☆	L	X	H	H	X	X	X	X	X	CBRN
Full-register transfer	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register transfer	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)□	H	H	H	L	H	Row Addr	Block Addr	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)□	H	H	L	L	H	Row Addr	Block Addr	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)□	H	H	L	L	H	Row Addr	Block Addr	X	Col Mask	BWM
Load write-mask register◊	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:

X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the falling edge of $\overline{WE}$ or the first falling edge of $\overline{CASx}$, whichever occurs later.
‡ Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
§ The column address, the block address, or the tap point is latched on the first falling edge of $\overline{CASx}$ depending upon which function is executed.
¶ CBRS cycle should be performed immediately after the power-up initialization for stop-point mode.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
☆ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ For 4-column block write (TMS5516x), block address is A2–A8; for 8-column block write (TMS5517x), block address is A3–A8.
◊ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

Table 3. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row address, tap point	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{CASL}$ $\overline{CASU}$	Column-address strobe, DQ output enable	Tap-address strobe	
DSF	Block-write enable Load-write-mask-register enable Load-color-register enable CBR (option reset)	Split-register-transfer enable	
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WE}$	Write enable, write-per-bit enable		
DQx	DRAM data I/O, write mask		
SC			Serial clock
$\overline{SE}$			SQ output enable, QSF output enable
SQx			Serial-data output
QSF			Serial-register status
V_{CC}†	Power supply		
V_{SS}†	Ground		
NC/GND	Make no external connection or tie to system GND		

† For proper device operation, all V_{CC} pins must be connected to a 5.0-V supply and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of $\overline{CAS}$x. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the first falling edge of $\overline{CAS}$x.

In 4-column block-write operations (TMS5516x), column-address bits A0–A1 are ignored. Column-address bits A2–A8 become the block address that selects one of the 128 blocks in the active row. In 8-column block write operations (TMS5517x), column-address bits A0–A2 are ignored. Column address bits A3–A8 become the block address that selects one of the 64 blocks in the active row.

In full-register operations, column-address bit A8 selects which half of the active row in the DRAM is transferred to the SAM. Column address bits A0–A7 select one of 256 tap points (starting positions) for the serial-data output.

In split-register-transfer operations, column address bit A8 selects the DRAM half row. Column-address bit A7 is ignored. The internal serial-address counter identifies which half of the SAM is in use. If the high half of the SAM is in use, the low half of the SAM is loaded with the low half of the DRAM half row, and vice versa. Column-address bits A0–A6 select one of 127 tap points (starting locations) for the serial output. Locations 127 and 255 are not valid tap points in split-register-transfer operations. In stop-point mode, stop-point locations are not valid tap points in split-register-transfer operations.

row-address strobe ($\overline{RAS}$)

The falling edge of $\overline{RAS}$ latches the states of the row address, $\overline{CASL}$, $\overline{CASU}$, DSF, $\overline{TRG}$, $\overline{WE}$, and the DQs onto the chip to initiate DRAM and transfer functions. $\overline{RAS}$ also functions as a DRAM output enable.

column-address strobe ($\overline{\text{CASL}}$, $\overline{\text{CASU}}$)

The first falling edge of $\overline{\text{CASx}}$ latches the states of the column address and DSF onto the chip to control DRAM and transfer functions. $\overline{\text{CASL}}$ and $\overline{\text{CASU}}$ provide byte control in DRAM operations. $\overline{\text{CASL}}$ controls the lower byte (DQ0–DQ7), and $\overline{\text{CASU}}$ controls the upper byte (DQ8–DQ15). Byte control can be applied in read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. $\overline{\text{CASx}}$ also functions as a DRAM output enable.

special-function select (DSF)

DSF is latched on the falling edge of $\overline{\text{RAS}}$ and the falling edge of $\overline{\text{CASx}}$ to determine which functions are invoked on a particular cycle (see Table 2).

output enable, transfer select ($\overline{\text{TRG}}$)

$\overline{\text{TRG}}$ selects either DRAM or transfer operation as $\overline{\text{RAS}}$ falls. Holding $\overline{\text{TRG}}$ high on the falling edge of $\overline{\text{RAS}}$ selects the DRAM operation. Dropping $\overline{\text{TRG}}$ low on the falling edge of $\overline{\text{RAS}}$ selects the transfer operation. $\overline{\text{TRG}}$ also functions as DRAM output enable.

write enable, write-per-bit select ($\overline{\text{WE}}$)

$\overline{\text{WE}}$ selects either the write mode or the read mode in a $\overline{\text{CASx}}$ cycle. Dropping $\overline{\text{WE}}$ low selects the write mode. Holding $\overline{\text{WE}}$ high selects the read mode. Holding $\overline{\text{WE}}$ low on the falling edge of $\overline{\text{RAS}}$ selects the write-per-bit operation.

DRAM data I/O, write mask, column mask (DQ0–DQ15)

DQ0–DQ15 function as the DRAM input/output port in DRAM operations. In normal DRAM write cycles, all 16 bits of write data are latched on either the falling edge of $\overline{\text{WE}}$ or the first falling edge of $\overline{\text{CASx}}$, whichever occurs later. Similarly, the DQs are latched as write mask in load-mask-register cycles, as color data in load-color-register cycles, and as column mask in block-write cycles. In non-persistent write-per-bit cycles, the DQs are latched as the write mask on the falling edge of $\overline{\text{RAS}}$.

Data out is in the same polarity as data in. The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of one Series 74 TTL load. The outputs are in the high-impedance (floating) state until $\overline{\text{RAS}}$, $\overline{\text{CASx}}$, and $\overline{\text{TRG}}$ have all been brought low in read cycles. For the TMS551x0 devices, the outputs remain valid until $\overline{\text{CASx}}$ is brought high, $\overline{\text{TRG}}$ is brought high, or $\overline{\text{WE}}$ is brought low. For the TMS551x1 devices, the outputs remain valid until both $\overline{\text{RAS}}$ and $\overline{\text{CASx}}$ are brought high, $\overline{\text{TRG}}$ is brought high, or $\overline{\text{WE}}$ is brought low.

serial clock (SC)

The rising edge of SC increments the internal serial-address counter and accesses serial data at the next SAM location.

serial enable ($\overline{\text{SE}}$)

$\overline{\text{SE}}$ functions as the output enable for SQ0–SQ15 and QSF. $\overline{\text{SE}}$ low enables the serial-data output. $\overline{\text{SE}}$ high disables the serial-data output. Holding $\overline{\text{SE}}$ high does not disable the serial clock SC. The rising edge of SC automatically increments the internal serial-address counter regardless of the state of $\overline{\text{SE}}$.

serial data outputs (SQ0–SQ15)

SQ0–SQ15 function as the SAM output port. The 3-state output buffer provides direct TTL compatibility (no pullup resistors) with a fan-out of one Series 74 TTL load. Serial data is accessed from the SAM on the rising edge of SC. $\overline{\text{SE}}$ low enables the outputs. The outputs are in the high-impedance (floating) state when disabled.

special-function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. QSF is low when the internal serial-address counter points to the lower (least significant) 128 bits of the SAM. QSF is high when the internal serial-address counter points to the higher (most significant) 128 bits of SAM. QSF is in the high-impedance state when $\overline{\text{SE}}$ is high.

functional operation description

random-access operation

Table 4. DRAM Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNEMONIC CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)☆	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)□	H	H	H	L	H	Row Addr	Block Addr	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)□	H	H	L	L	H	Row Addr	Block Addr	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)□	H	H	L	L	H	Row Addr	Block Addr	X	Col Mask	BWM
Load write-mask register ◊	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the falling edge of $\overline{WE}$ or the first falling edge of $\overline{CASx}$, whichever occurs later.
‡ Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
§ The column address, the block address, or the tap point is latched on the first falling edge of $\overline{CASx}$ depending upon which function is executed.
¶ CBRS cycle should be performed immediately after the power-up initialization for stop-point mode.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
☆ CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
□ For 4-column block write (TMS5516x), block address is A2–A8; for 8-column block write (TMS5517x), block address is A3–A8.
◊ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.

refresh

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) refresh

CBR refreshes are accomplished by bringing either or both $\overline{\text{CASL}}$ and $\overline{\text{CASU}}$ low earlier than $\overline{\text{RAS}}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN (no reset) and CBRS (no reset and stop point set) refreshes do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR type refresh cycles regardless of the state of $\overline{\text{TRG}}$.

hidden refresh

A hidden refresh is accomplished by holding either or both $\overline{\text{CASL}}$ and $\overline{\text{CASU}}$ low in the DRAM read cycle and cycling $\overline{\text{RAS}}$. The output data of the DRAM read cycle remains valid while the refresh is carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

$\overline{\text{RAS}}$-only refresh

A $\overline{\text{RAS}}$-only refresh is accomplished by cycling $\overline{\text{RAS}}$ at every row address. Unless $\overline{\text{CASx}}$ and $\overline{\text{TRG}}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{\text{RAS}}$-only refresh. Strobing each of the 512 row addresses with $\overline{\text{RAS}}$ causes all bits in each row to be refreshed.

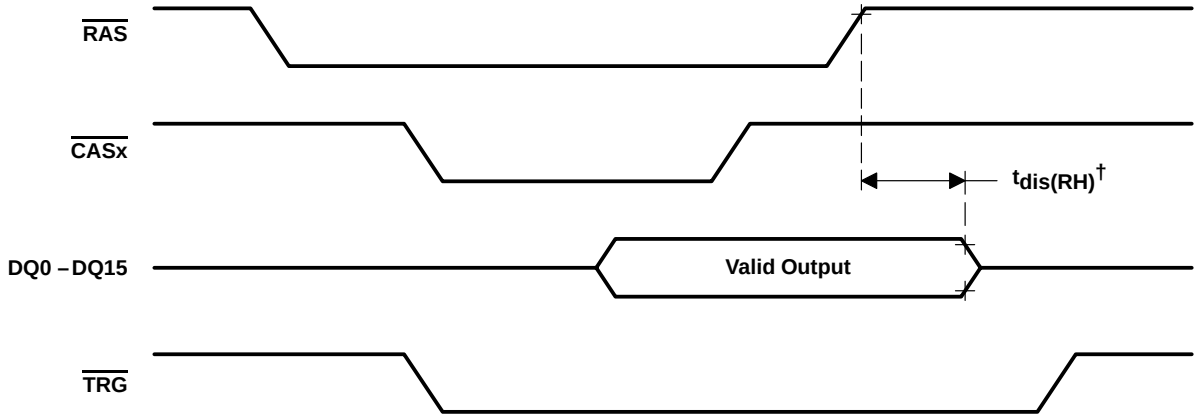
enhanced page mode (TMS551x0)

Enhanced page mode allows faster memory access by keeping the same row address while selecting random column addresses. The maximum $\overline{\text{RAS}}$ low time and minimum $\overline{\text{CASx}}$ page cycle time are used to determine the number of columns that can be accessed.

Unlike conventional page mode, the enhanced page mode allows the TMS551x0 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{\text{CASx}}$ goes low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{\text{CASx}}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{\text{CASx}}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

extended data output (TMS551x1)

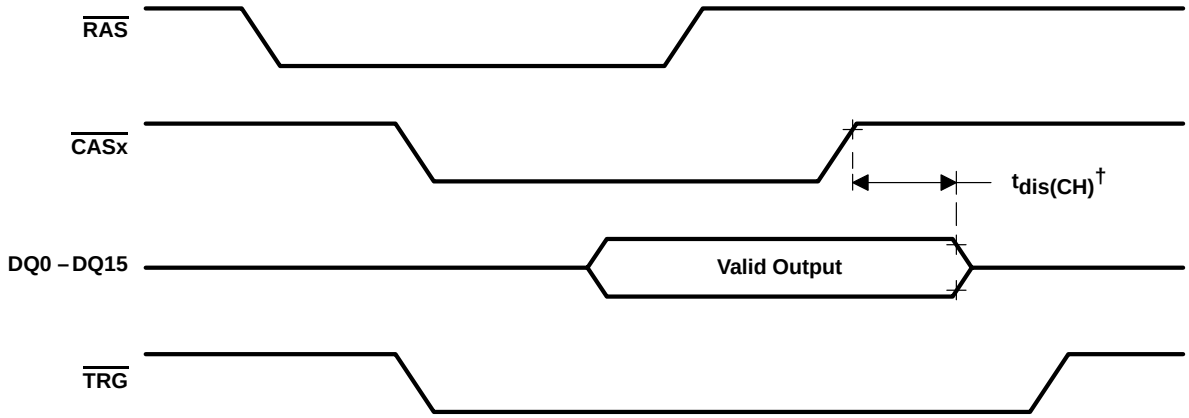
The TMS551x1 features extended data output during DRAM accesses. While $\overline{\text{RAS}}$ and $\overline{\text{TRG}}$ are low, the DRAM output remains valid even when $\overline{\text{CASx}}$ returns high. The output remains valid until $\overline{\text{WE}}$ is low, $\overline{\text{TRG}}$ is high, or both $\overline{\text{CASx}}$ and $\overline{\text{RAS}}$ are high (see Figure 1, Figure 2, and Figure 3). The extended data-output mode functions in all read cycles including DRAM read, page-mode read, and read-modify-write cycles.



† See “switching characteristics over recommended ranges of supply voltage and operating free-air temperature” table.

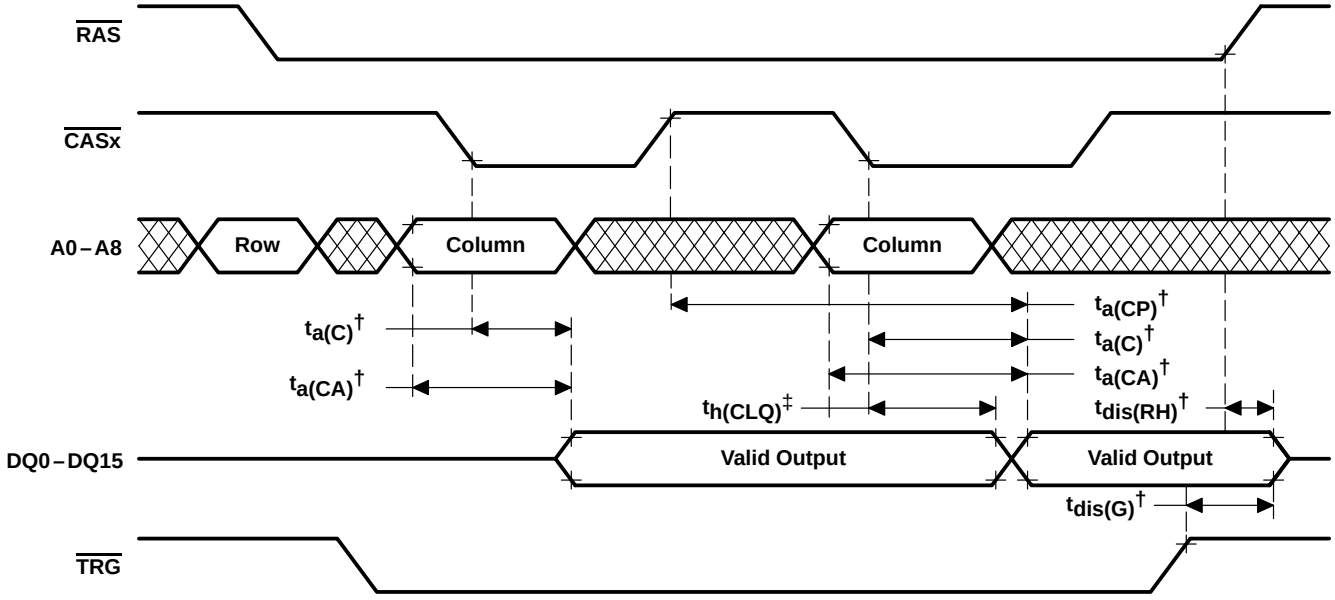
Figure 1. DRAM Read Cycle With $\overline{\text{RAS}}$-Controlled Output (TMS551x1)

extended data output (TMS551x1) (continued)



† See "switching characteristics over recommended ranges of supply voltage and operating free-air temperature" table.

Figure 2. DRAM Read Cycle With $\overline{CAS}$-Controlled Output (TMS551x1)

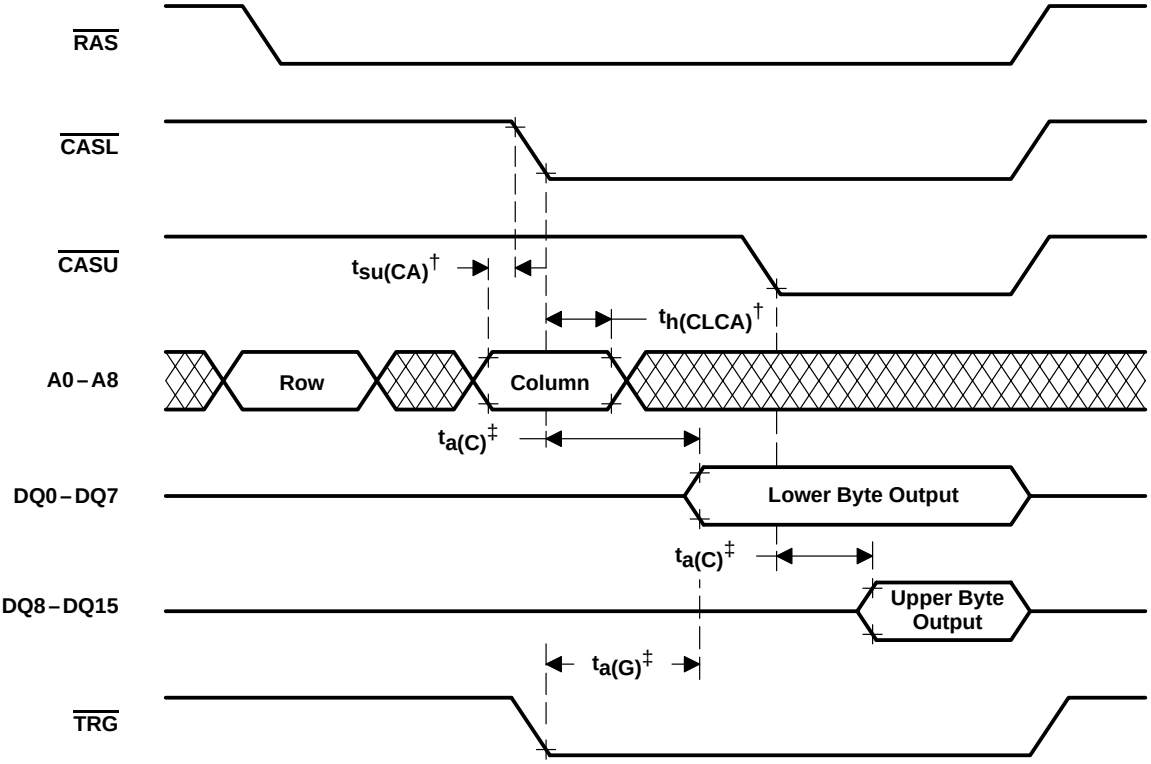


† See "switching characteristics over recommended ranges of supply voltage and operating free-air temperature" table.
‡ See "timing requirements over recommended ranges of supply voltage and operating free-air temperature" table.

Figure 3. DRAM Page-Read Cycle With Extended Data Output (TMS551x1)

byte operation

Byte operation can be applied in DRAM read cycles, write cycles, block-write cycles, load-write-mask-register cycles and load-color-register cycles. In byte operation, the column address (A0–A8) is latched at the first falling edge of $\overline{\text{CAS}}$x. In read cycles, $\overline{\text{CASL}}$ enables the lower byte (DQ0–DQ7) and $\overline{\text{CASU}}$ enables the upper byte (DQ8–DQ15) (see Figure 4).

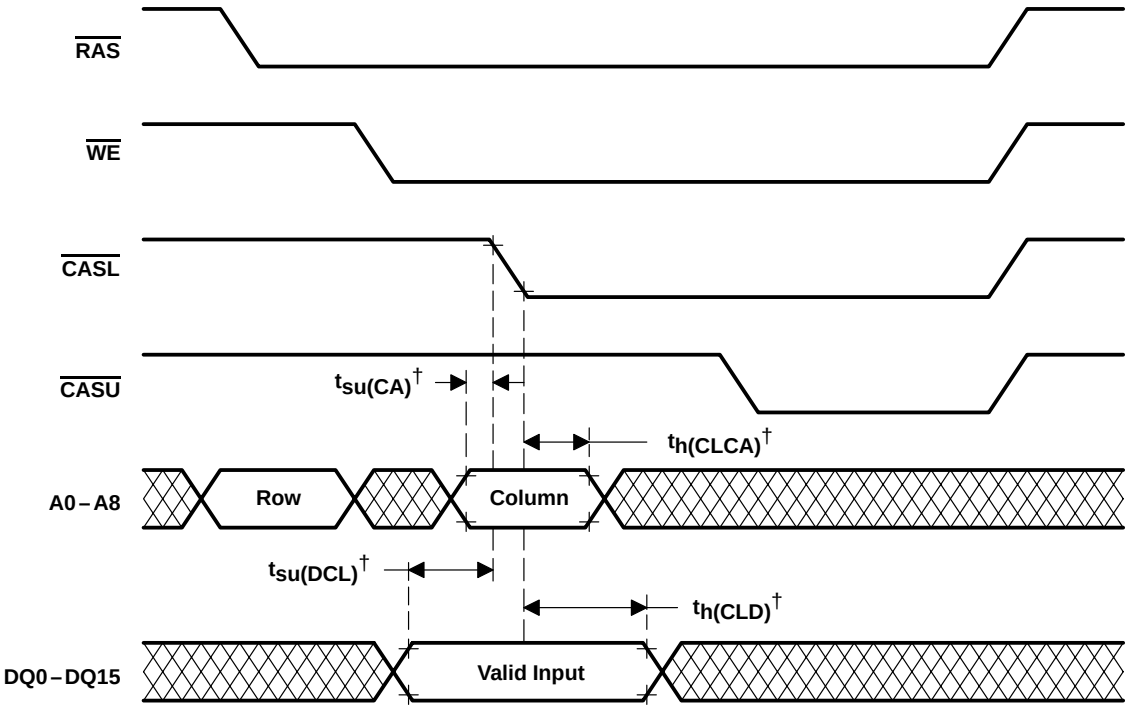


† See “switching characteristics over recommended ranges of supply voltage and operating free-air temperature” table.
‡ See “timing requirements over recommended ranges of supply voltage and operating free-air temperature” table.

Figure 4. Example of a Byte-Read Cycle

byte operation (continued)

In byte-write operation, $\overline{\text{CASL}}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{\text{CASU}}$ enables data to be written to the upper byte (DQ8–DQ15). In an early-write cycle, $\overline{\text{WE}}$ is brought low prior to both $\overline{\text{CASx}}$ signals. Data setup and hold times for DQ0–DQ15 are referenced to the first falling edge of $\overline{\text{CASx}}$ (see Figure 5).

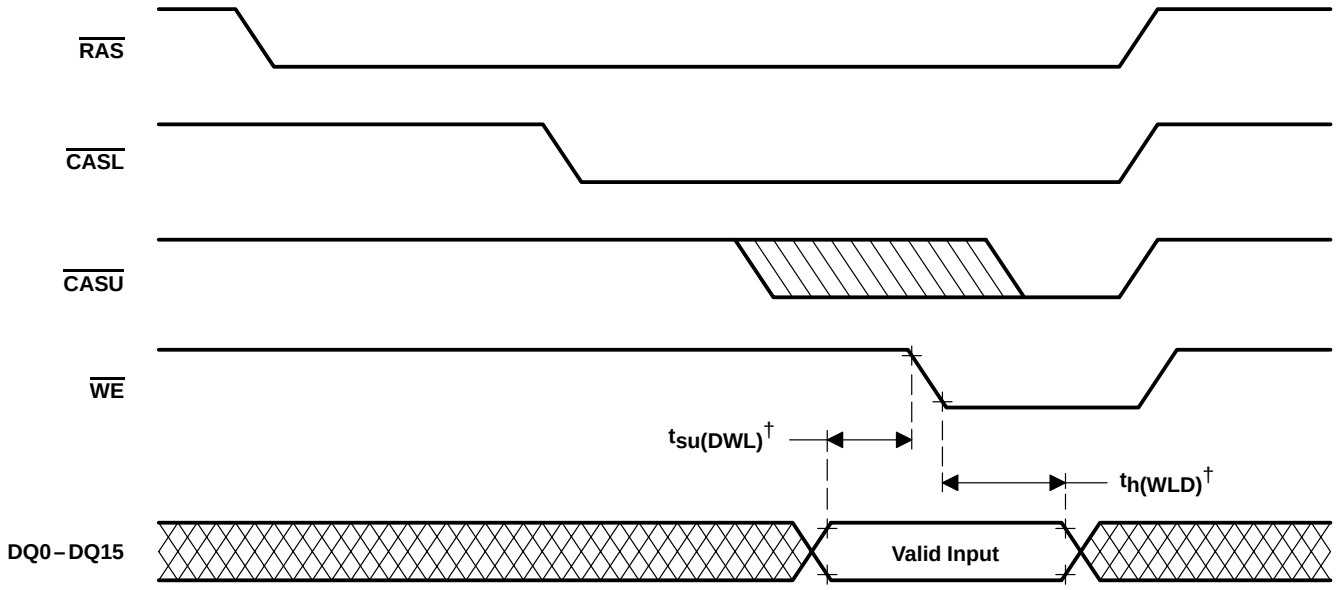


† See “switching characteristics over recommended ranges of supply voltage and operating free-air temperature” table.

Figure 5. Example of an Early-Write Cycle

byte operation (continued)

For late-write or read-modify-write cycles, $\overline{WE}$ is brought low after either or both $\overline{CASL}$ and $\overline{CASU}$ fall. The data is strobed in with data setup and hold times for DQ0 – DQ15 referenced to $\overline{WE}$ (see Figure 6).



† See “timing requirements over recommended ranges of supply voltage and operating free-air temperature” table.

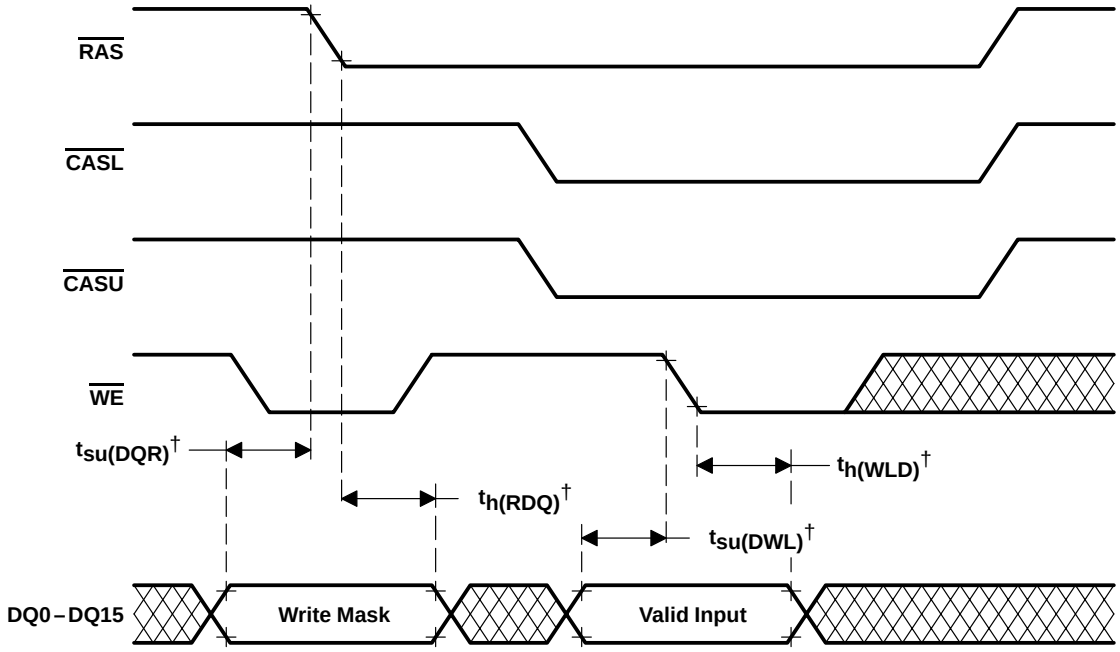
Figure 6. Example of a Late-Write Cycle

write-per-bit

The write-per-bit function allows the masking of any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. There are two write-per-bit modes: the nonpersistent write-per-bit and the persistent write-per-bit.

nonpersistent write-per-bit

When $\overline{WE}$ is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device through the DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 DQs are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the falling edge of $\overline{WE}$ or the first falling edge of $\overline{CASx}$, whichever occurs later. $\overline{CASL}$ enables the lower byte (DQ0–DQ7) to be written through the mask and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a write-mask-low (write mask = 0) is strobed into a particular DQ pin on the falling edge of $\overline{RAS}$, data is not written to that DQ. If a write-mask-high (write mask = 1) is strobed into a particular DQ pin on the falling edge of $\overline{RAS}$, data is written to that DQ (see Figure 7).



† See “timing requirements over recommended ranges of supply voltage and operating free-air temperature” table.

Figure 7. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load-write-mask-register (LMR) cycle first. In the persistent write-per-bit mode, the write-per-bit mask is not overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or until power is removed.

The LMR cycle is performed using DRAM write-cycle timing except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the first falling edge of $\overline{CAS}$x. A binary code is input to the write-mask register through the random I/O pins and latched on either the first falling edge of $\overline{CAS}$x or the falling edge of $\overline{WE}$, whichever occurs later. Byte-write control can be applied to the write mask during the LMR cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh with option reset cycle (see Figure 8).

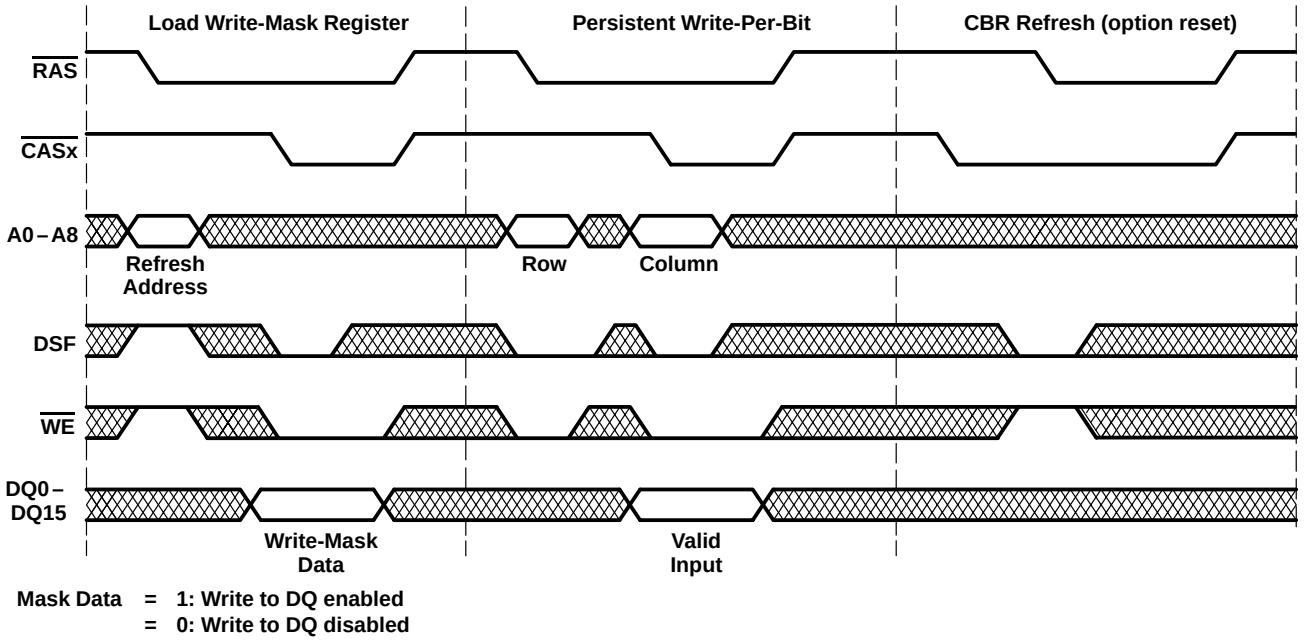


Figure 8. Example of a Persistent Write-Per-Bit Operation

4-column block write (TMS5516x)

The 4-column block-write function allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as 4 columns × 4 DQs and repeated in four quadrants. In this manner, each of the four one-megabit quadrants can have up to four consecutive columns written at a time with up to four DQs per column (see Figure 9).

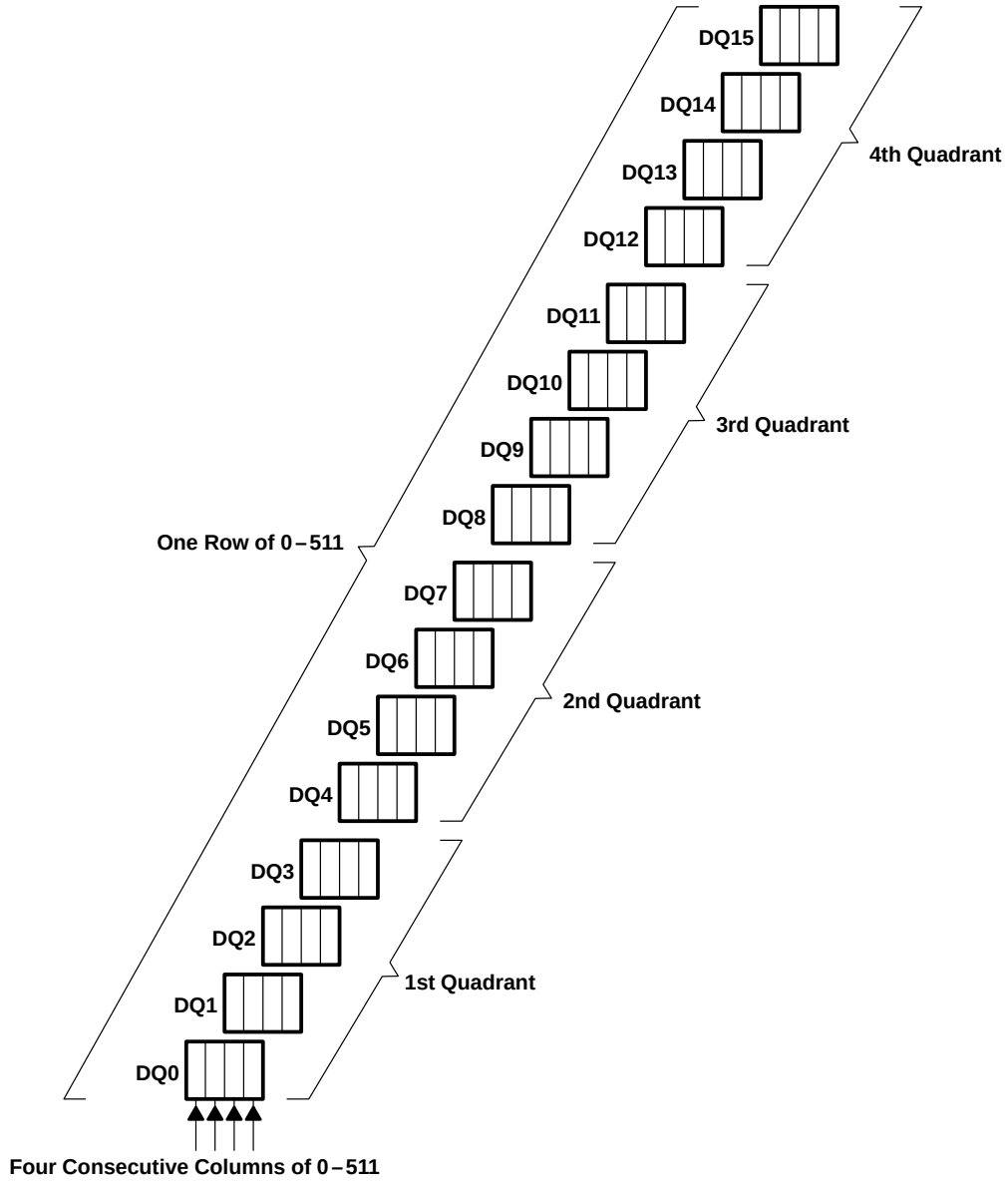


Figure 9. 4-Column Block-Write Operation

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. Write data (color data) is provided by four bits from the on-chip color register. Bits 0 – 3 from the 16-bit write-mask register, bits 0 – 3 from the 16-bit column-mask register, and bits 0 – 3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4 – 7, 8 – 11, and 12 – 15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 10).

4-column block write (continued)

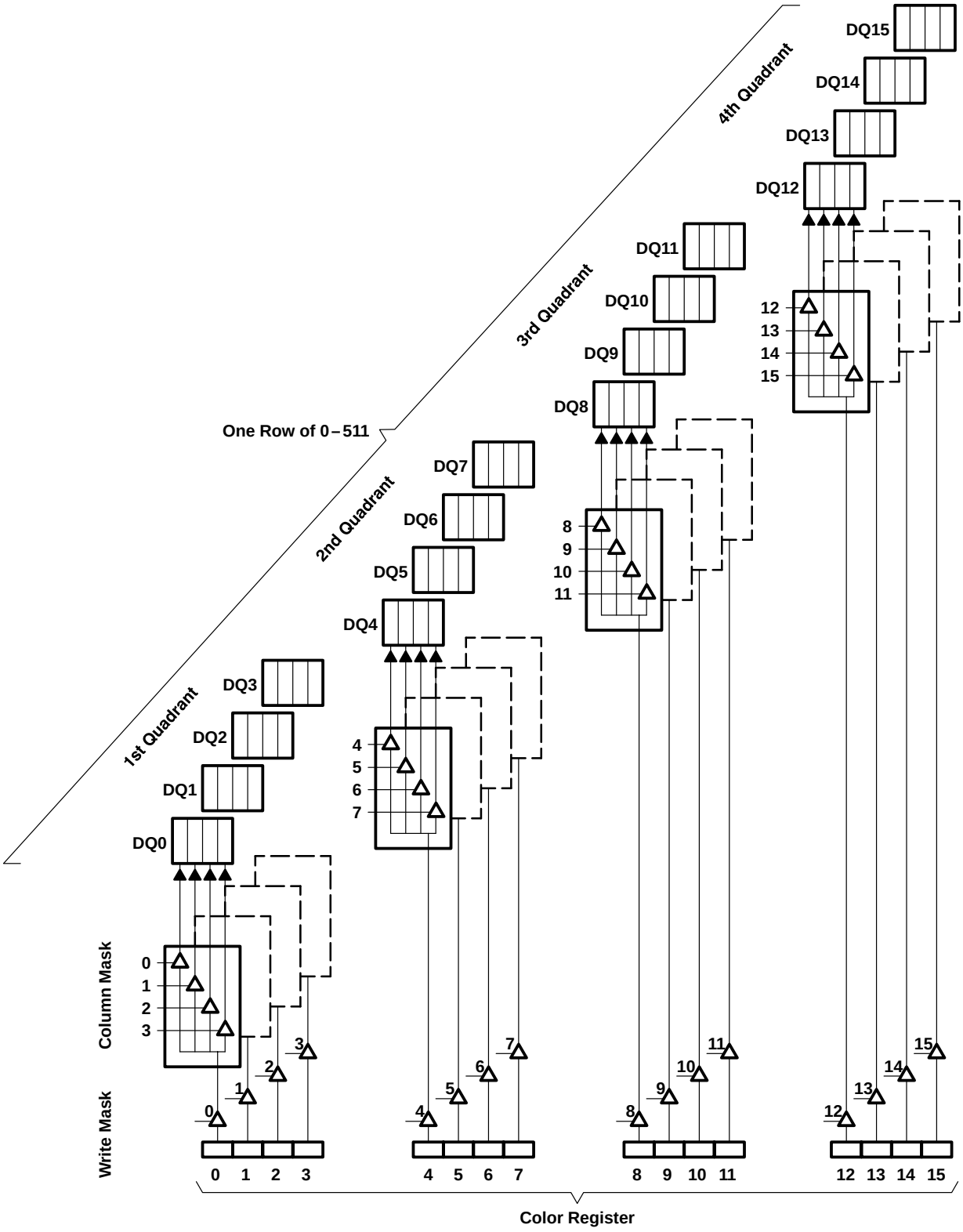


Figure 10. 4-Column Block Write With Masks

4-column block write (continued)

Every four adjacent columns makes a block, which results in 128 blocks along one row. Block 0 comprises columns 0 – 3, block 1 comprises columns 4 – 7, block 2 comprises columns 8 – 11, etc., as shown in Figure 11.

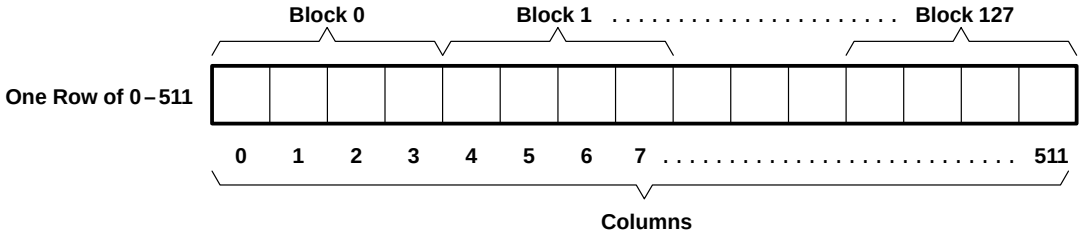


Figure 11. 4-Column-Block Column-Organization

During 4-column block-write cycles, only the seven most significant column addresses (A2 – A8) are latched on the falling edge of $\overline{CASx}$ to decode one of the 128 blocks. Address bits A0 – A1 are ignored. All one-megabit quadrants have the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the falling edge of $\overline{CASx}$. As in a DRAM write operation, $\overline{CASL}$ and $\overline{CASU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input through the DQs and is latched on either the falling edge of $\overline{WE}$ or the first falling edge of $\overline{CASx}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on the use of the write-mask capability, allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0 – A8 from left to right)

		bit 0			bit 15
color-data register	=	1011	1011	1100	0111
write-mask register	=	1110	1111	1111	1011
column-mask register	=	1111	0000	0111	1010
		1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0 – 3) is selected for all one-megabit quadrants. The first quadrant has DQ0 – DQ2 written with bits 0 – 2 from the color-data register to all four columns of block 0. DQ3 is not written and retains its previous data due to the write-mask bit 3 being a 0.

The second quadrant (DQ4 – DQ7) has all four columns masked off due to the column-mask bits 4 – 7 being 0, so that no data is written.

The third quadrant (DQ8 – DQ11) has its four DQs written with bits 8 – 11 from the color-data register to columns 1 – 3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to the column-mask bit 8 being 0.

The fourth quadrant (DQ12 – DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 12 after the 4-column block-write operation shown in the example.

4-column block write (continued)

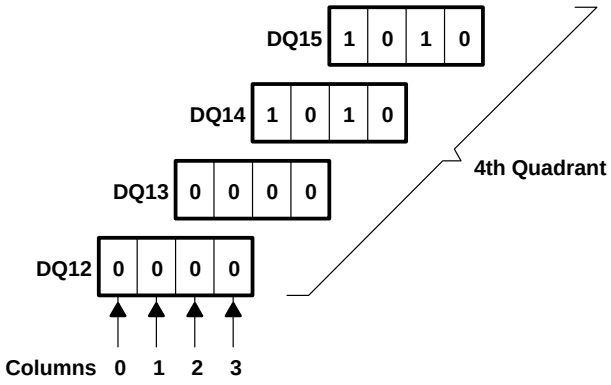


Figure 12. Example of Fourth Quadrant After 4-Column Block-Write Operation

8-column block write (TMS5517x)

The 8-column block-write function allows up to 128 bits of data to be written simultaneously to one row of the memory array. This function is implemented as 8 columns × 8 DQs and repeated in two bytes. In this manner, each of the two bytes can have up to eight consecutive columns written at a time with up to eight DQs per column (see Figure 13).

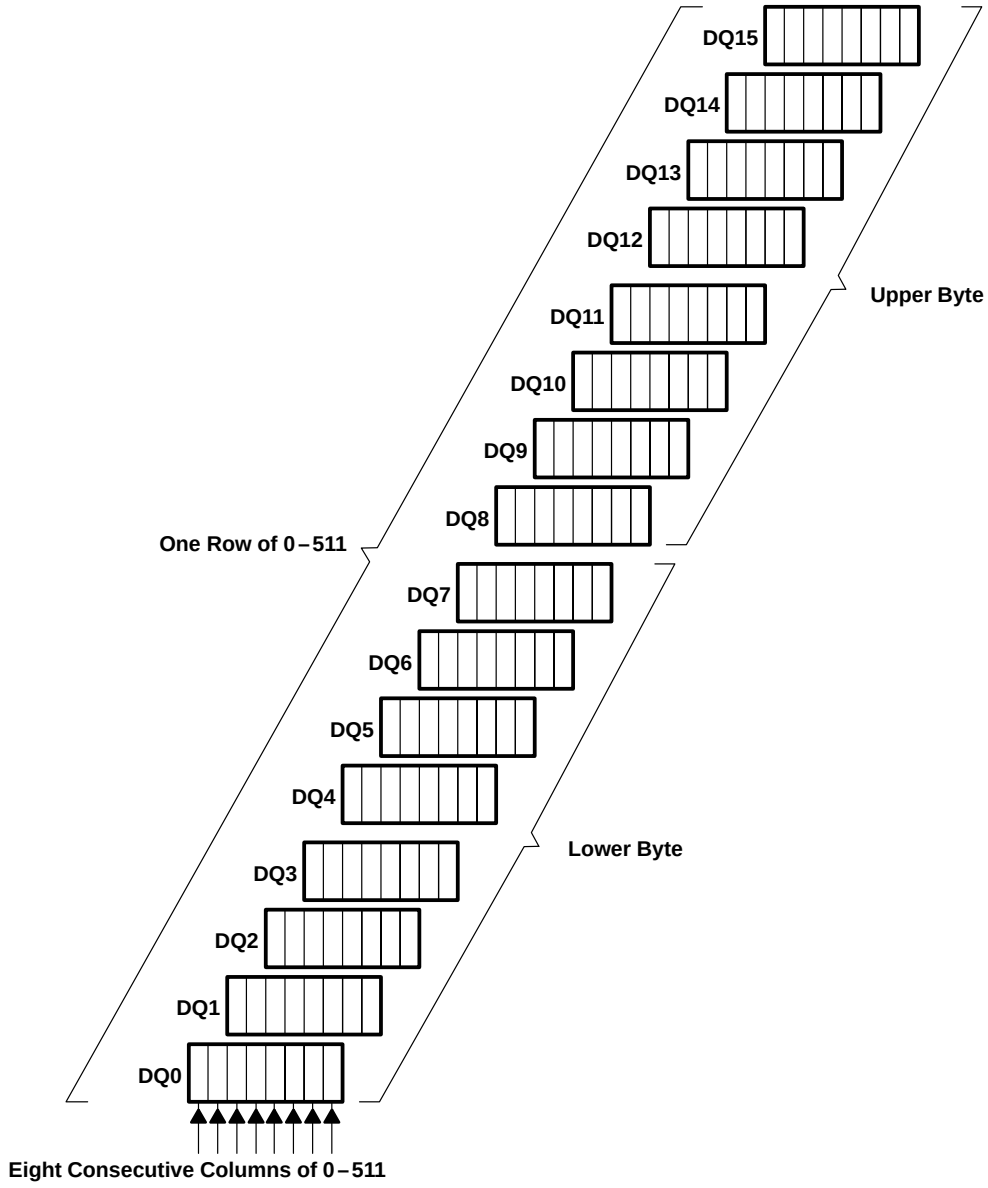


Figure 13. 8-Column Block-Write Operation

Each byte has an 8-bit column mask to mask off any or all of the eight columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. Write data (color data) is provided by eight bits from the on-chip color register. Bits 0 – 7 from the 16-bit write-mask register, bits 0 – 7 from the 16-bit column-mask register, and bits 0 – 7 from the 16-bit color-data register configure the block write for the lower byte, while bits 8 – 15 control the upper byte in a similar fashion (see Figure 14).

8-column block write (TMS5517x) (continued)

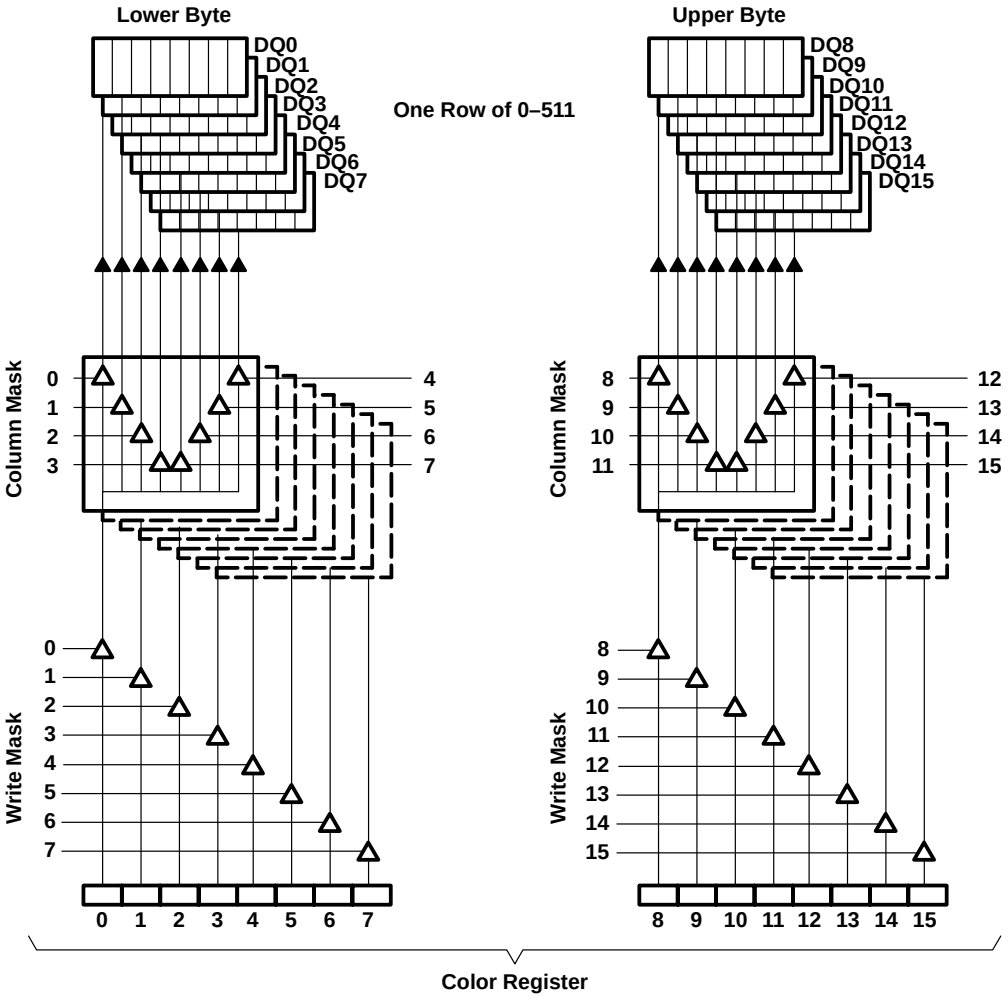


Figure 14. 8-Column Block Write With Masks

Every eight adjacent columns makes a block resulting in 64 blocks along one row. Block 0 comprises columns 0 – 7, block 1 comprises columns 8 – 15, block 2 comprises columns 16 – 23, etc., as shown in Figure 15.

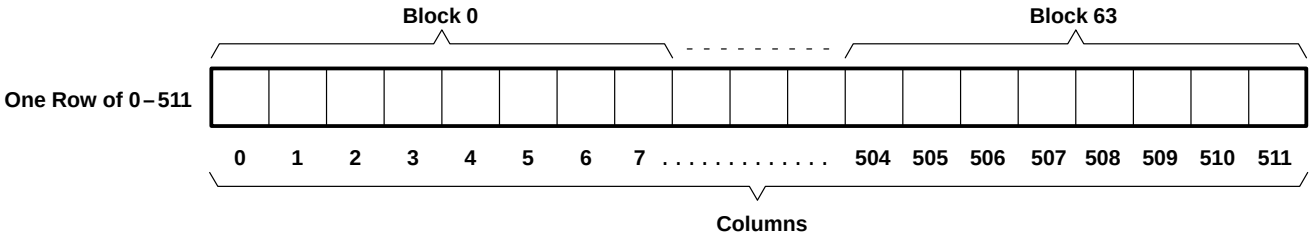


Figure 15. 8-Column-Block Column-Organization

During 8-column block-write cycles, only the six most significant column addresses (A3 – A8) are latched on the falling edge of $\overline{\text{CAS}}$x to decode one of the 64 blocks. Address bits A0 – A2 are ignored. Both bytes have the same block selected.

8-column block write (continued)

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{\text{CAS}}$x. As in a DRAM write operation, $\overline{\text{CASL}}$ and $\overline{\text{CASU}}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input through the DQs and is latched on either the falling edge of $\overline{\text{WE}}$ or the first falling edge of $\overline{\text{CAS}}$x, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability allowing additional performance options.

Example of block write:

block-write column address	=	110000000 (A0 – A8 from left to right)	
		bit 0	bit 15
color-data register	=	10111011	11000111
write-mask register	=	11101111	11111011
column-mask register	=	11110000	01111010
		Lower Byte	Upper Byte

Column-address bits A0 – A2 are ignored. Block 0 (columns 0 – 7) is selected for both bytes. The lower byte has DQ0 – DQ2 and DQ4 – DQ7 written with bits 0 – 2 and 4 – 7 from the color-data register to columns 0 – 3. Columns 4 – 7 are not written and retain their previous data due to the column-mask bits 4 – 7 being 0. DQ3 is not written and retains its previous data due to the write-mask bit 3 being 0.

The upper byte has DQ8 – DQ12 and DQ14 – DQ15 written with bits 8 – 12 and 14 – 15 from the color-data register to columns 1 – 4 and 6. Columns 0, 5, and 7 are not written and retain their previous data due to the column-mask bits 8, 13, and 15 being 0. DQ13 is not written and retains its previous data due to the write-mask-register bit 13 being 0. If the previous data was all 0s, the upper byte would contain the data pattern in Figure 16 after the 8-column block-write operation shown in the example.

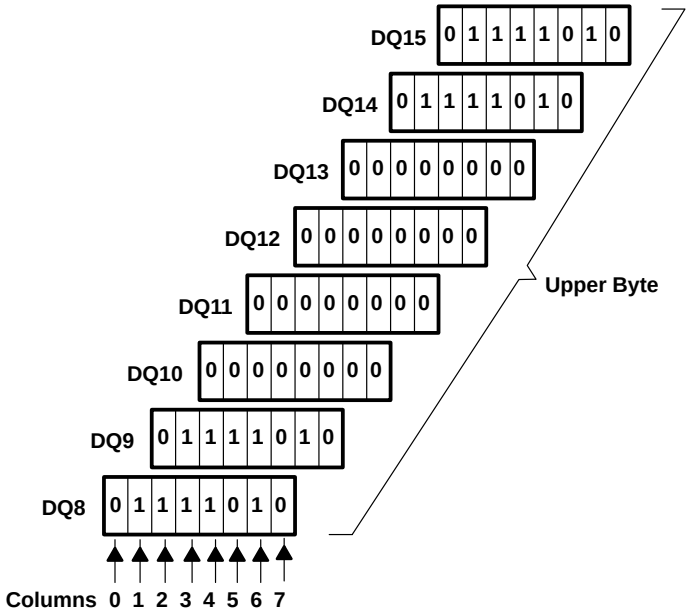
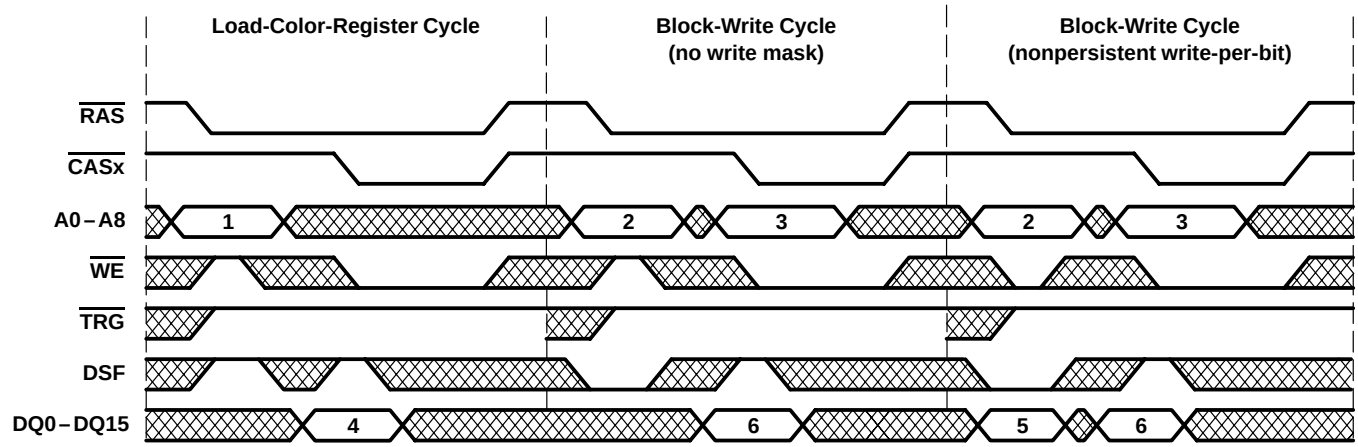


Figure 16. Example of Upper Byte After 8-Column Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and on the first falling edge of $\overline{CASx}$. The color register is loaded from pins DQ0 – DQ15, which are latched on either the falling edge of $\overline{WE}$ or the first falling edge of $\overline{CASx}$, whichever occurs later. If only one $\overline{CASx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figure 17 and Figure 18).



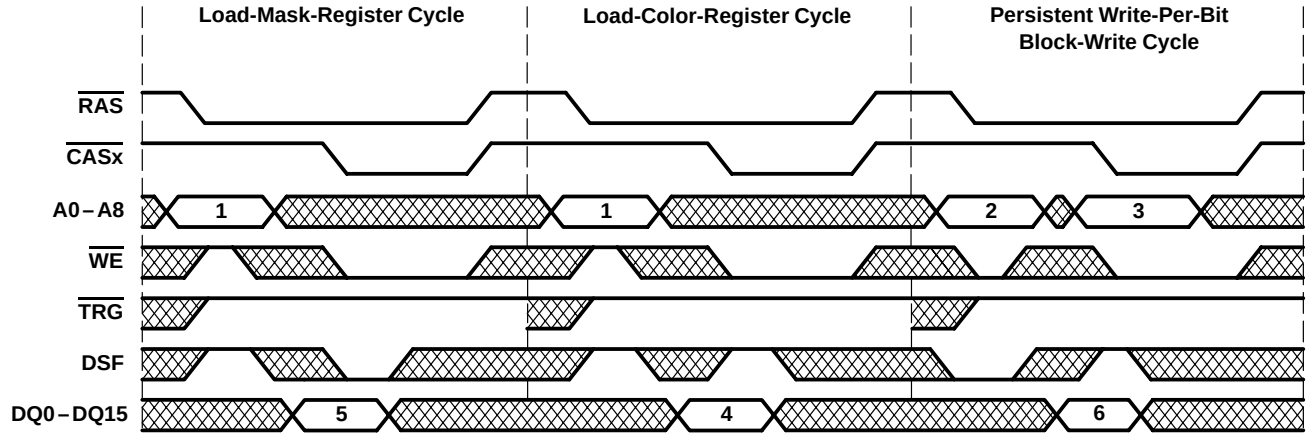
Legend:

1. Refresh address: A0 – A8 are latched on the falling edge of $\overline{RAS}$.
2. Row address: A0 – A8 are latched on the falling edge of $\overline{RAS}$.
3. Block address A2 – A8 (TMS5516x) or A3 – A8 (TMS5517x) are latched on the first falling edge of $\overline{CASx}$.
4. Color data: DQ0 – DQ15 are latched on the falling edge $\overline{WE}$ or on the first falling edge of $\overline{CASx}$, whichever occurs first.
5. Write-mask data: DQ0 – DQ15 are latched on the falling edge $\overline{RAS}$.
6. Column-mask data: DQ0 – DQ15 are latched on the falling edge $\overline{WE}$ or on the first falling edge of $\overline{CASx}$, whichever occurs first.

= don't care

Figure 17. Example of Block Writes

load color register (continued)



Legend:

1. Refresh address: A0 – A8 are latched on the falling edge of $\overline{\text{RAS}}$.
2. Row address: A0 – A8 are latched on the falling edge of $\overline{\text{RAS}}$.
3. Block address A2 – A8 (TMS5516x) or A3 – A8 (TMS5517x) are latched on the first falling edge of $\overline{\text{CAS}}$x.
4. Color data: DQ0 – DQ15 are latched on the falling edge $\overline{\text{WE}}$ or on the first falling edge of $\overline{\text{CAS}}$x, whichever occurs first.
5. Write-mask data: DQ0 – DQ15 are latched on the falling edge $\overline{\text{RAS}}$.
6. Column-mask data: DQ0 – DQ15 are latched on the falling edge $\overline{\text{WE}}$ or on the first falling edge of $\overline{\text{CAS}}$x, whichever occurs first.

= don't care

Figure 18. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one-half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by bringing $\overline{\text{TRG}}$ low and holding $\overline{\text{WE}}$ high on the falling edge of $\overline{\text{RAS}}$. The state of DSF, which is latched on the falling edge of $\overline{\text{RAS}}$, determines whether the full-register-transfer operation or the split-register-transfer operation is performed.

Table 5. SAM Function Table

FUNCTION	$\overline{\text{RAS}}$ FALL				$\overline{\text{CAS}}$x FALL	ADDRESS		DQ0 – DQ15		MNEMONIC CODE
	$\overline{\text{CAS}}$x†	$\overline{\text{TRG}}$	$\overline{\text{WE}}$	DSF	DSF	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$x	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$x $\overline{\text{WE}}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either or both $\overline{\text{CASL}}$ and $\overline{\text{CASU}}$ are low.

X = don't care

full-register-transfer read

A full-register-transfer operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0 – A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0 – A8) are latched at the first falling edge of $\overline{CASx}$, where address bit A8 selects which half of the row is transferred. Address bits A0 – A7 select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 19).

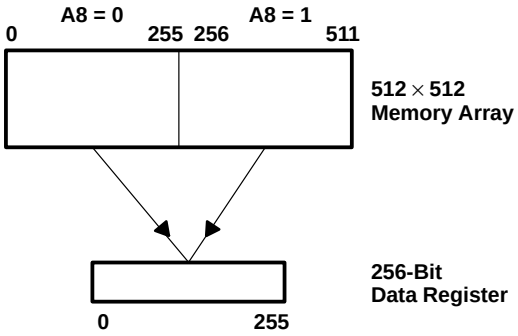


Figure 19. Full-Register-Transfer Read

A full-register transfer can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register-transfer cycle (see Figure 20).

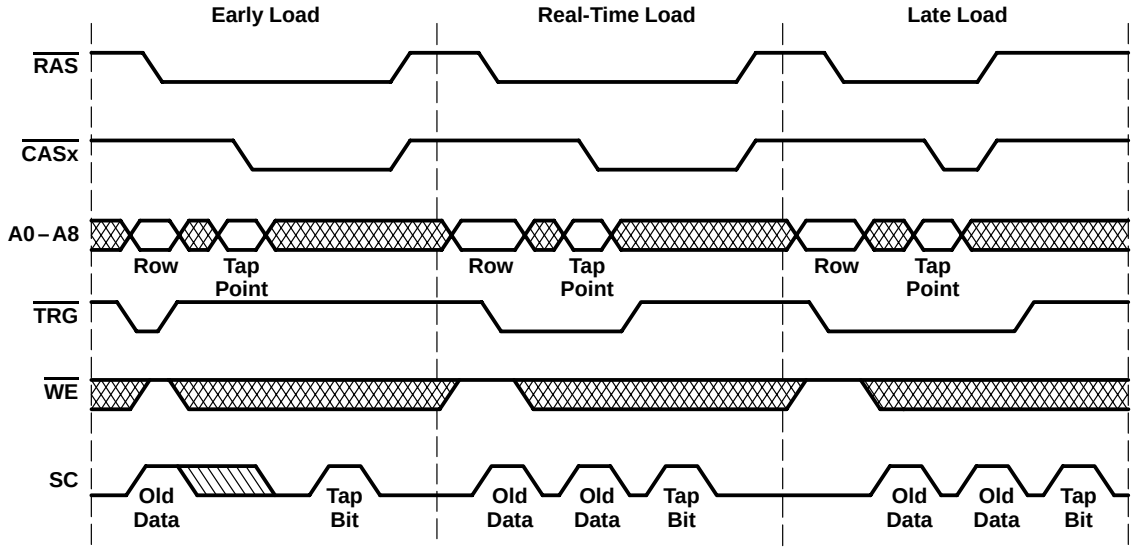


Figure 20. Example of Full-Register-Transfer Read Operations

split-register-transfer read

In split-register-transfer operations, the serial-data register is split into halves (see Figure 21). The low half contains bits 0 – 127, and the high half contains bits 128 – 255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

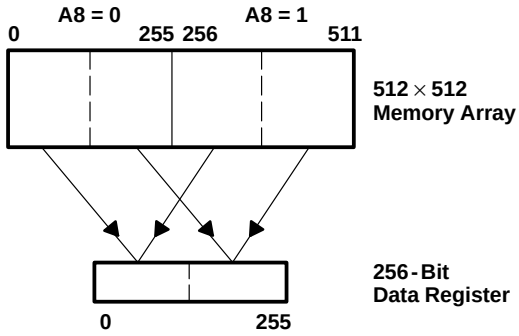
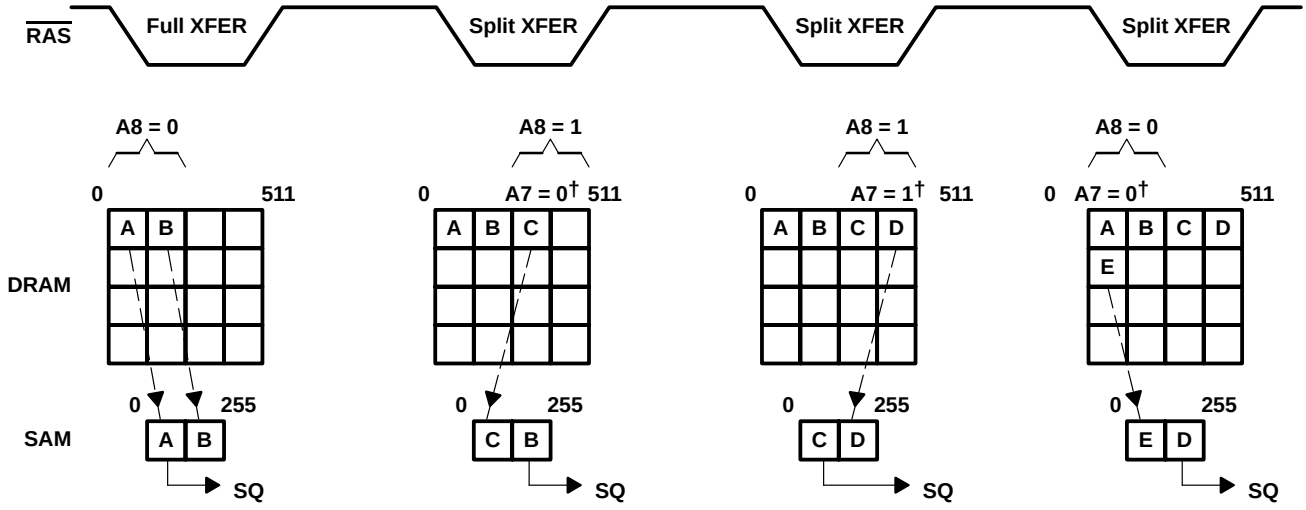


Figure 21. Split-Register-Transfer Read

To invoke a split-register-transfer cycle, DSF is brought high, $\overline{\text{TRG}}$ is brought low, and both are latched at the falling edge of $\overline{\text{RAS}}$ (see Figure 22). Nine row-address bits (A0 – A8) are also latched at the falling edge of $\overline{\text{RAS}}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0 – A6 and A8) are latched at the first falling edge of $\overline{\text{CAS}}$x. Column-address bit A8 selects which half of the row is to be transferred. Column-address bit A7 is ignored, and the split-register transfer is internally controlled to select the inactive half. Column-address bits A0 – A6 select one of 127 tap points in the specified half of SAM. Locations 127 and 255 are not valid tap points in split-register-transfer operations. In stop-point mode, stop-point locations are not valid tap points in split-register-transfer operations.



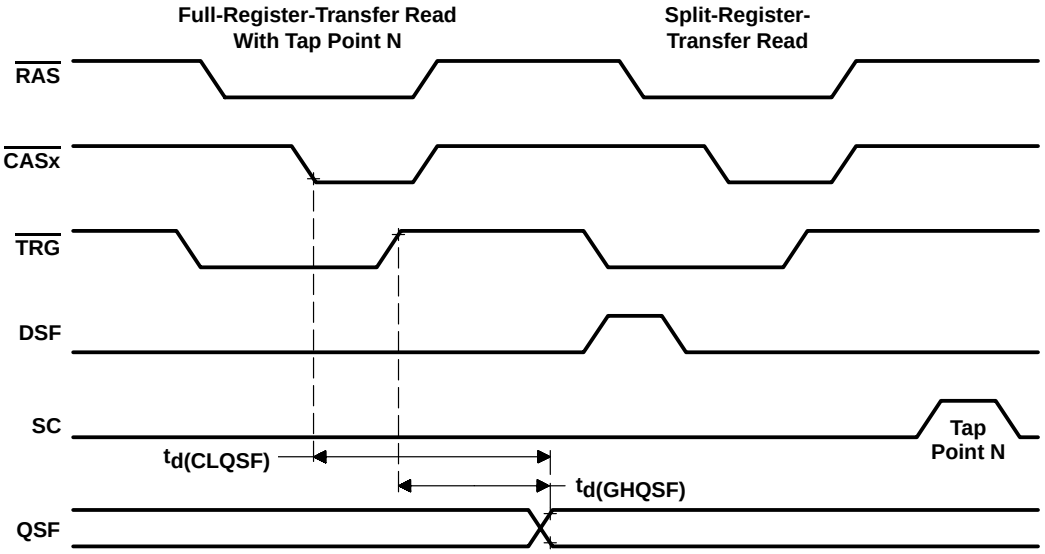
† A7 shown is internally controlled.

Figure 22. Example of a Split-Register-Transfer Read Operation

A full-register transfer must precede the first split-register transfer to ensure proper operation. After the full-register transfer cycle, the first split-register transfer can follow immediately without any minimum SC clock requirement.

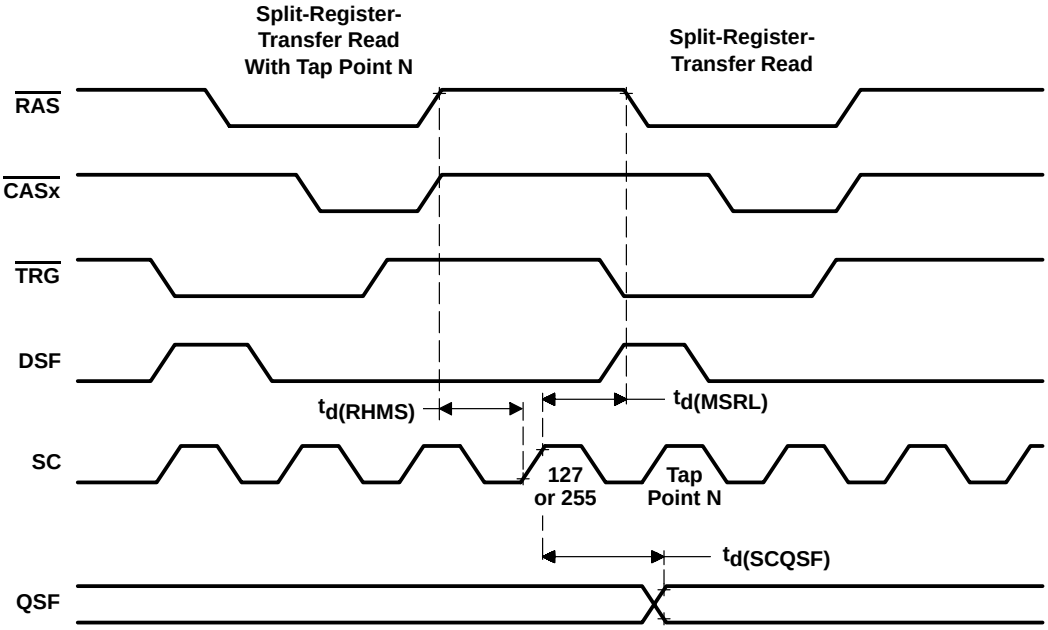
split-register-transfer read (continued)

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.



NOTE A: See “timing requirements over recommended ranges of supply voltage and operating free-air temperature” table.

Figure 23. Example of a Split-Register-Transfer Read After a Full-Register-Transfer Read



NOTE A: See “timing requirements over recommended ranges of supply voltage and operating free-air temperature” table.

Figure 24. Example of Successive Split-Register-Transfer Read Operations

serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data is accessed from the SAM at the rising edge of serial clock SC. $\overline{SE}$ low enables the outputs. $\overline{SE}$ high disables the outputs. Holding $\overline{SE}$ high does not disable SC. The rising edge of SC automatically increments the internal serial-address counter regardless of the state of $\overline{SE}$. In full-register-transfer operations, the counter proceeds sequentially to the most significant bit (bit 255), and then wraps around to the least significant bit (bit 0), as shown in Figure 25.

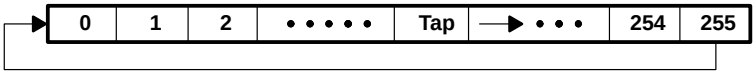


Figure 25. Serial-Pointer Direction for Serial Read

In split-register-transfer operations, serial data can be read out from the active half of SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer then proceeds sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register-transfer (see Figure 26).

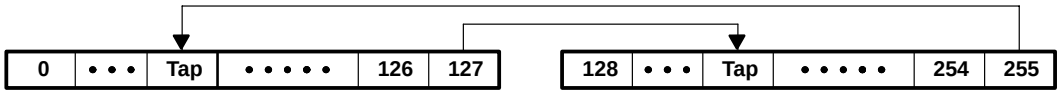


Figure 26. Serial Pointer for Split-Register Read – Case I

If there is no split-register transfer to the inactive half during this period, the serial pointer points to the next bit, bit 128 or bit 0, respectively (see Figure 27).

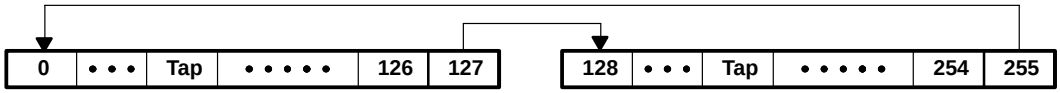


Figure 27. Serial Pointer for Split-Register Read – Case II

split-register programmable stop point

The TMS551xx offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve 2-D drawing performance in a nonscanline data format.

In split-register-transfer read operations, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed on row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 28).

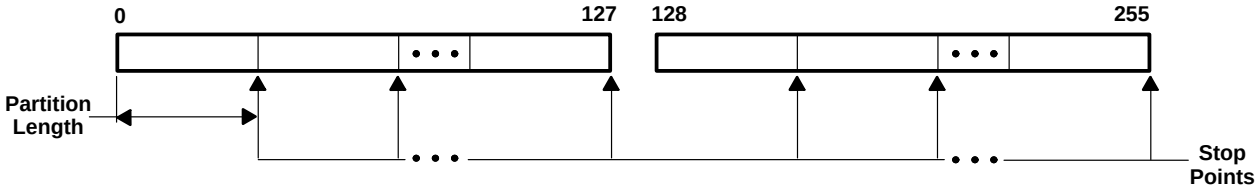


Figure 28. Example of SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$x low, $\overline{WE}$ low, and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ also latches row addresses A4–A7, which are used to define the SAM's partition length. The other row-address inputs are don't cares. Stop-point mode should be initiated immediately after the power-up initialization (see Table 6).

Table 6. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines in which SAM partition the serial output begins and at which stop point the serial output stops coming from one half of SAM and switches to the opposite half of SAM (see Figure 29).

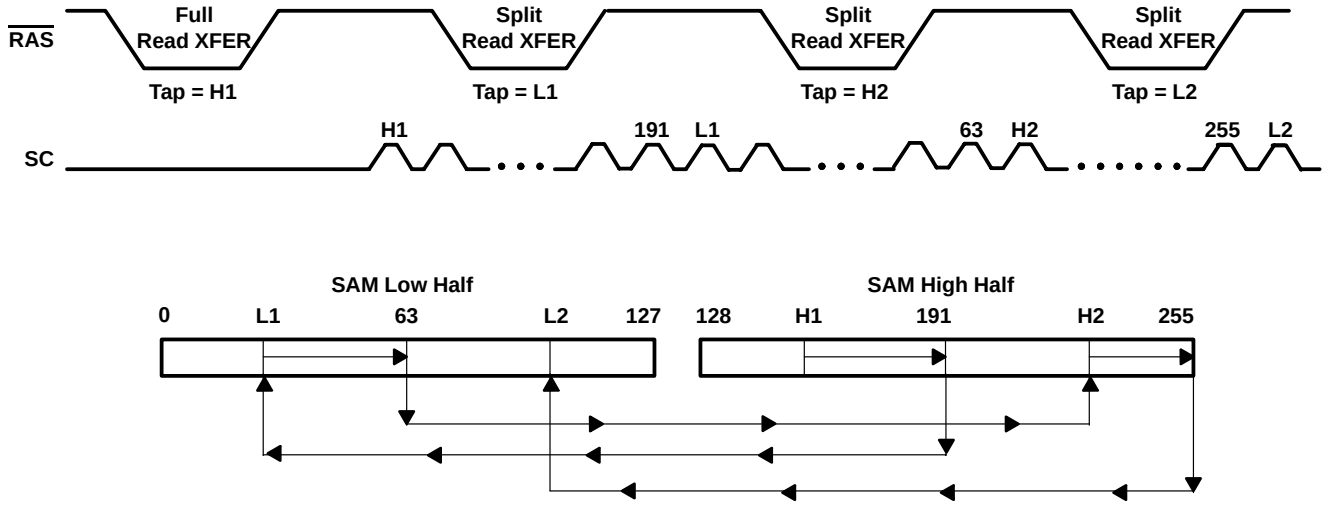


Figure 29. Example of Split-Register Operation With Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible with both 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are swapped internally to assure compatibility (see Figure 29). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register-transfer. During stop-point mode, a CBR (option reset) cycle is not recommended because this ends the stop-point mode and restores address bits AY7 and AY8 to their normal functions. Consistent use of CBR cycles ensures that the TMS551xx remains in nomal mode.

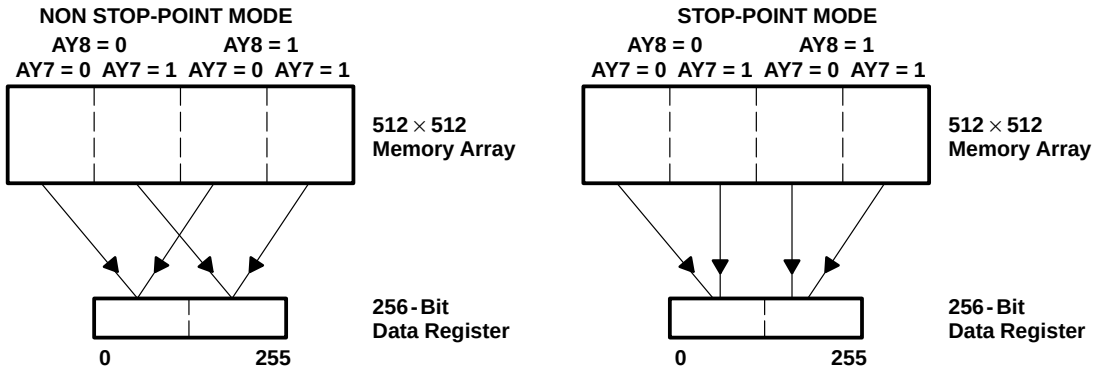


Figure 30. DRAM-to-SAM Mapping, Nonstop-Point Versus Stop Point

IMPORTANT: For proper device operation, a stop-point-mode (CBRS) cycle should be initiated immediately after the power-up initialization cycles are performed.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight $\overline{RAS}$ cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are required to initialize the SAM port.

After initialization, the internal state of the TMS551xx is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write-mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	TMS551xx
Supply voltage range, V_{CC} (see Note 1)	–1 V to 7 V
Voltage range on any pin	–1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	1.1 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS551xx			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1.0		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SAM PORT	’551xx-60		’551xx-70		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, See Note 3			±10		±10	µA
I_{CC1}	Operating current‡	See Note 4	Standby		180		165	mA
I_{CC1A}	Operating current‡	$t_{c(SC)}$ = MIN	Active		225		205	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5	mA
I_{CC2A}	Standby current‡	$t_{c(SC)}$ = MIN	Active		70		65	mA
I_{CC3}	$\overline{RAS}$ only refresh current	See Note 4	Standby		180		165	mA
I_{CC3A}	$\overline{RAS}$ only refresh current‡	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205	mA
I_{CC4}	Page-mode current‡	$t_{c(P)}$ = MIN, See Note 5	Standby	’551x0	135		115	mA
				’551x1	140		140	
I_{CC4A}	Page-mode current‡	$t_{c(SC)}$ = MIN, See Note 5	Active	’551x0	175		155	mA
				’551x1	185		185	
I_{CC5}	CBR current	See Note 4	Standby		180		165	mA
I_{CC5A}	CBR current‡	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		200		180	mA
I_{CC6A}	Data-transfer current‡	$t_{c(SC)}$ = MIN	Active		250		225	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}; $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN
5. Measured with one address change while $\overline{CASx}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, address strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS †	ALT. SYMBOL	’551xx-60		’551xx-70		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time, DQx from $\overline{CASx}$ low	$t_{d(RLCL)}$ = MAX	t_{CAC}		17		20	ns
$t_{a(CA)}$	Access time, DQx from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		30		35	ns
$t_{a(CP)}$	Access time, DQx from $\overline{CASx}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		35		40	ns
$t_{a(G)}$	Access time, DQx from $\overline{TRG}$ low		t_{OEA}		15		20	ns
$t_{a(R)}$	Access time, DQx from $\overline{RAS}$ low	$t_{d(RLCL)}$ = MAX	t_{RAC}		60		70	ns
$t_{a(SE)}$	Access time, SQx from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		12		15	ns
$t_{a(SQ)}$	Access time, SQx from SC high	C_L = 30 pF	t_{SCA}		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CASx}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	3	15	3	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	3	15	3	20	ns
$t_{dis(RH)}$	Disable time, random output from $\overline{RAS}$ high (see Note 8)	C_L = 50 pF		3	15	3	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	3	10	3	20	ns
$t_{dis(WL)}$	Disable time, random output from $\overline{WE}$ low (see Note 8)	C_L = 30 pF	t_{WEZ}	0	15	0	20	ns

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM-port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V. Switching times for SAM-port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial-data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

			ALT. SYMBOL	’551xx-60		’551xx-70		UNIT
				MIN	MAX	MIN	MAX	
$t_{c(P)}$	Cycle time, page-mode read, write	’551x0	t_{PC}	35		40		ns
		’551x1	t_{PC}	30		30		ns
$t_{c(rd)}$	Cycle time, read		t_{RC}	110		130		ns
$t_{c(rdW)}$	Cycle time, read-modify-write		t_{RMW}	150		175		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write		t_{PRMW}	80		90		ns
$t_{c(SC)}$	Cycle time, serial clock (see Note 9)		t_{SCC}	18		22		ns
$t_{c(TRD)}$	Cycle time, transfer read		t_{RC}	110		130		ns
$t_{c(W)}$	Cycle time, write		t_{WC}	110		130		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$x high		t_{CPN}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$x low (see Note 10)	’551x0	t_{CAS}	10	10 000	10	10 000	ns
		’551x1	t_{CAS}	17	10 000	20	10 000	ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high		t_{TP}	20		20		ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high		t_{RP}	40		50		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)		t_{RAS}	60	10 000	70	10 000	ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)		t_{RASP}	60	100 000	70	100 000	ns
$t_{w(SCH)}$	Pulse duration, SC high		t_{SC}	5		8		ns
$t_{w(SCL)}$	Pulse duration, SC low		t_{SCP}	5		8		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low			15		20		ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low		t_{WP}	10		10		ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$x low		t_{ASC}	0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CAS}$x low, early write		t_{DSC}	0		0		ns
$t_{su(DQR)}$	Setup time, write mask valid before $\overline{RAS}$ low, non-persistent write-per-bit		t_{MS}	0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WE}$ low, late write		t_{DSW}	0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low		t_{ASR}	0		0		ns
$t_{su(rd)}$	Setup time, $\overline{WE}$ high before first $\overline{CAS}$x low, read		t_{RCS}	0		0		ns
$t_{su(SFC)}$	Setup time, DSF before first $\overline{CAS}$x low		t_{FSC}	0		0		ns
$t_{su(SFR)}$	Setup time, DSF before $\overline{RAS}$ low		t_{FSR}	0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ before $\overline{RAS}$ low		t_{THS}	0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WE}$ low before both $\overline{CAS}$x high, write		t_{CWL}	15		15		ns
$t_{su(WCL)}$	Setup time, $\overline{WE}$ low before first $\overline{CAS}$x low, early write		t_{WCS}	0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WE}$ low before $\overline{RAS}$ low, write-per-bit		t_{WSR}	0		0		ns
$t_{su(WRH)}$	Setup time, $\overline{WE}$ low before $\overline{RAS}$ high, write		t_{RWL}	15		15		ns
$t_{h(CHrd)}$	Hold time, $\overline{WE}$ high after both $\overline{CAS}$x high, read (see Note 12)		t_{RCH}	0		0		ns
$t_{h(CLCA)}$	Hold time, column address after first $\overline{CAS}$x low		t_{CAH}	10		10		ns
$t_{h(CLD)}$	Hold time, data valid after first $\overline{CAS}$x low, early write		t_{DH}	15		15		ns
$t_{h(CLQ)}$	Hold time, DQ output after $\overline{CAS}$x low (TMS551x1)		t_{DHC}	4		5		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user’s transition times, this can require additional $\overline{CAS}$x low time [$t_{w(CL)}$].
11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user’s transition times, this can require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
12. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	’551xx-60		’551xx-70		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(CLW)}$	Hold time, $\overline{WE}$ low after first $\overline{CASx}$ low, early write	t_{WCH}	10		15		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(RDQ)}$	Hold time, write mask valid after $\overline{RAS}$ low, non-persistent write-per-bit	t_{MH}	10		10		ns
$t_{h(RHrd)}$	Hold time, $\overline{WE}$ high after $\overline{RAS}$ high, read (see Note 12)	t_{RRH}	0		0		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 13)	t_{AR}	30		30		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 13)	t_{DHR}	35		35		ns
$t_{h(RLW)}$	Hold time, $\overline{WE}$ low after $\overline{RAS}$ low, write	t_{WCR}	30		35		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low	t_{FHR}	30		35		ns
$t_{h(RWM)}$	Hold time, $\overline{WE}$ low after $\overline{RAS}$ low, write-per-bit	t_{RWH}	10		10		ns
$t_{h(SFC)}$	Hold time, DSF after first $\overline{CASx}$ low	t_{CFH}	10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low	t_{RFH}	10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ after SC high	t_{SOH}	4		5		ns
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low	t_{THH}	10		10		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WE}$ low, late write	t_{DH}	15		15		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WE}$ low (see Note 14)	t_{OEH}	10		10		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CASx}$ high	t_{CAL}	30		45		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time-load and late-load full-register transfer	t_{ATH}	20		20		ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high	t_{RAL}	30		35		ns
$t_{d(CASH)}$	Delay time, column address to first SC high after $\overline{TRG}$ high, early-load full-register transfer	t_{ASD}	25		25		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WE}$ low, read-modify-write	t_{AWD}	50		60		ns
$t_{d(CHRL)}$	Delay time, both $\overline{CASx}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high, read		17		20		ns
$t_{d(CLQSF)}$	Delay time, first $\overline{CASx}$ low to QSF switching, full-register transfer (see Note 15)	t_{CQD}		30		30	ns
$t_{d(CLRH)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high	t_{RSH}	17		20		ns
$t_{d(CLRL)}$	Delay time, first $\overline{CASx}$ low to $\overline{RAS}$ low, CBR refresh	t_{CSR}	0		0		ns
$t_{d(CLSH)}$	Delay time, first $\overline{CASx}$ low to first SC high after $\overline{TRG}$ high, early-load full-register transfer	t_{CSD}	20		20		ns
$t_{d(CLTH)}$	Delay time, first $\overline{CASx}$ low to $\overline{TRG}$ high, real-time-load and late-load full-register transfer	t_{CTH}	15		15		ns
$t_{d(CLWL)}$	Delay time, $\overline{CASx}$ low to $\overline{WE}$ low, read-modify-write (see Note 16)	t_{CWD}	37		45		ns
$t_{d(CLZ)}$	Delay time, first $\overline{CASx}$ low to DQ in the low-impedance state	t_{CLZ}	3		2		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CASx}$ low	t_{DZC}	0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{OED}	10		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
13. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
16. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF, and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	’551xx-60		’551xx-70		UNIT
				MIN	MAX	MIN	MAX	
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching, full-register transfer (see Note 16)		t_{TQD}		25		30	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high		t_{ROH}	10		15		ns
$t_{d(GLZ)}$	Delay time, $\overline{TRG}$ low to DQ in the low-impedance state		t_{OELZ}	3		3		ns
$t_{d(MSRL)}$	Delay time, last SC high at boundary (127 or 255) to $\overline{RAS}$ low, split-register transfer			15		20		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to first $\overline{CAS}$x low, CBR refresh		t_{RPC}	0		0		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last SC high at boundary (127 or 255), split-register-transfer			15		20		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid		t_{RAD}	15	30	15	35	ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$x high	’551x0	t_{CSH}	60		70		ns
		’551x1	t_{CSH}	53		60		ns
		CBR	t_{CHR}	10		10		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to first $\overline{CAS}$x low (see Note 17)		t_{RCD}	20	43	20	50	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching, full-register transfer (see Note 16)		t_{RQD}		65		70	ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high, early-load full-register transfer		t_{RSD}	65		70		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 18)		t_{RTH}	50		55		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low, read-modify-write		t_{RWD}	80		95		ns
$t_{d(SCQSF)}$	Delay time, last SC high at boundary (127 or 255) to QSF switching, split-register transfer (see Note 16)		t_{SQD}		20		25	ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high, full-register transfer		t_{TSL}	5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 18)		t_{TRD}	−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 18)		t_{TRP}	40		50		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 18)		t_{TSD}	20		25		ns
$t_{rf(MA)}$	Refresh time interval, memory		t_{REF}		8		8	ms
t_t	Transition time		t_T	3	50	3	50	ns

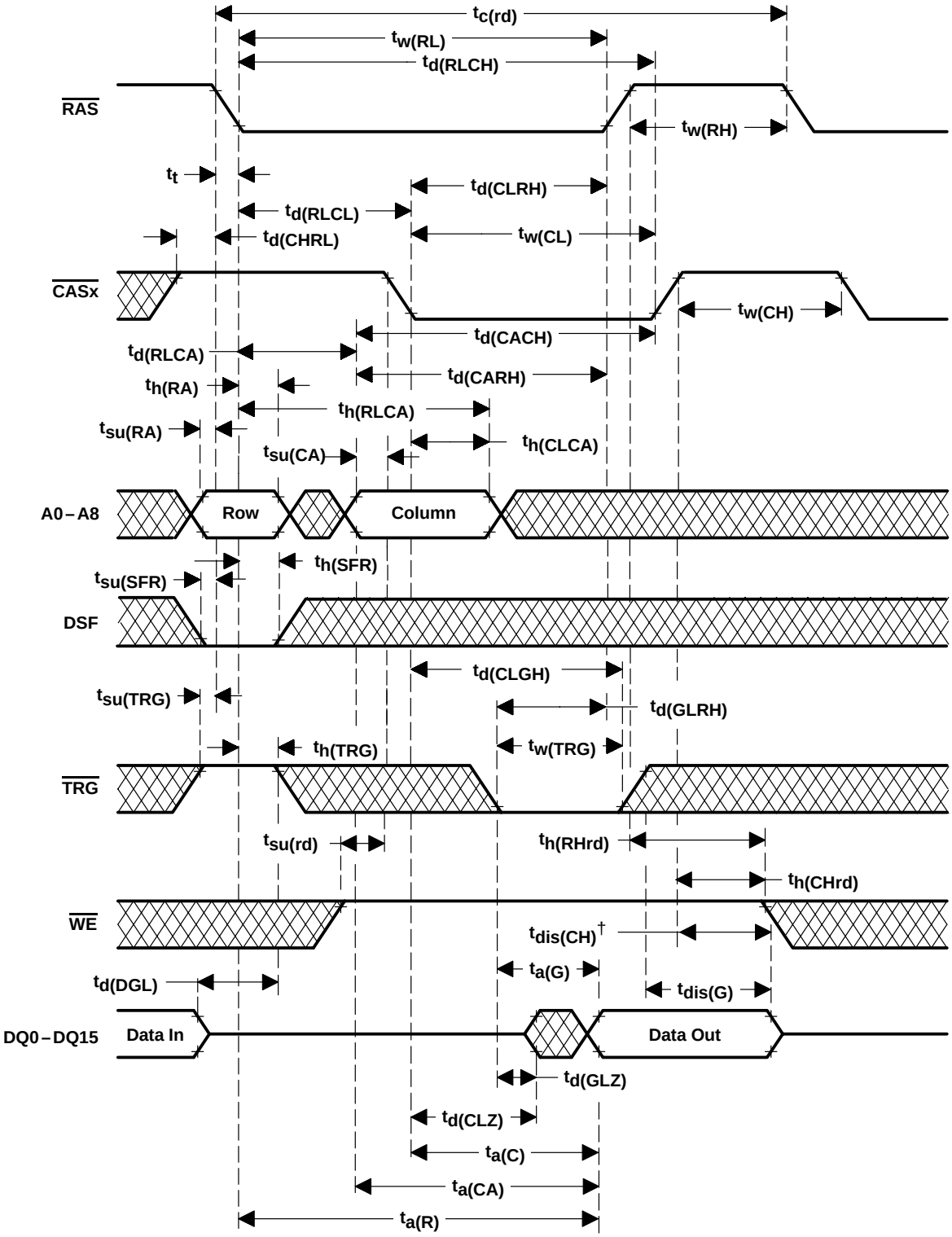
† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 16. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF, and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

17. The maximum value is specified only to assure $\overline{RAS}$ access time.

18. Real-time-load and late-load full-register transfer

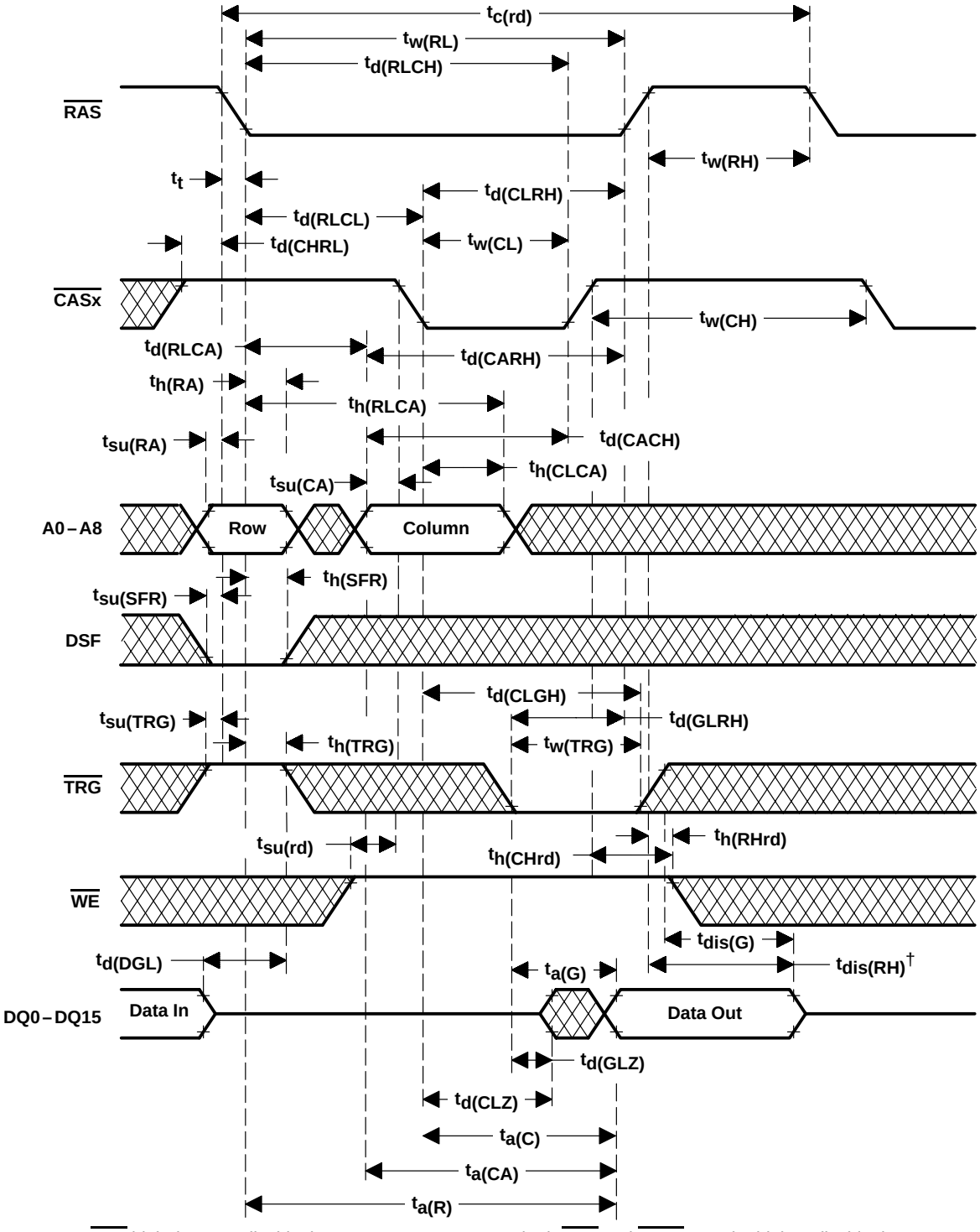
PARAMETER MEASUREMENT INFORMATION



† For TMS551x0, $\overline{\text{CASx}}$ high disables the output regardless of the state of $\overline{\text{RAS}}$. For TMS551x1, both $\overline{\text{RAS}}$ and $\overline{\text{CASx}}$ must be high to disable the output.

Figure 31. Read-Cycle Timing With $\overline{\text{CASx}}$-Controlled Output

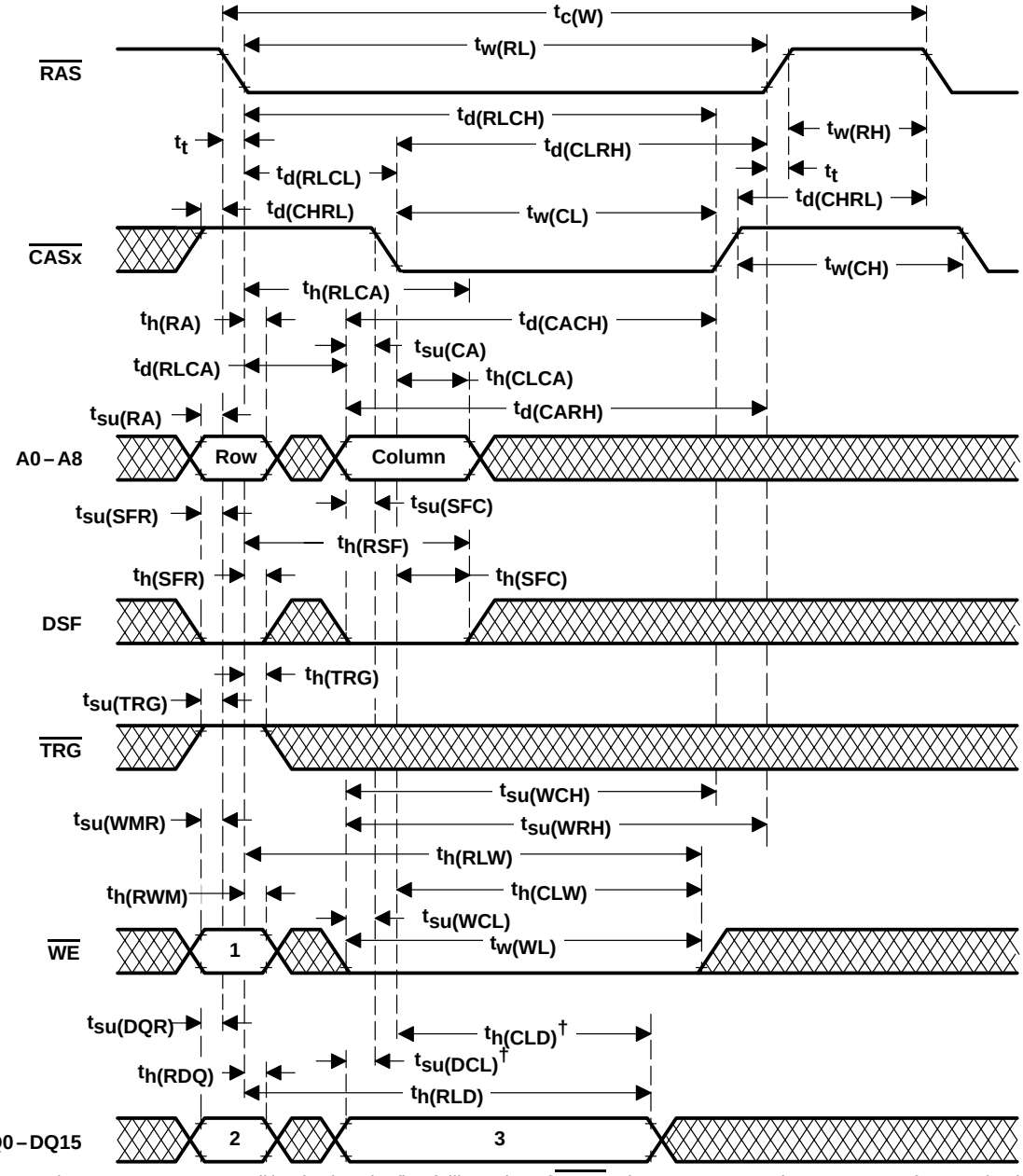
PARAMETER MEASUREMENT INFORMATION



† For TMS551x0, $\overline{\text{RAS}}$ high does not disable the output. For TMS551x1, both $\overline{\text{RAS}}$ and $\overline{\text{CASx}}$ must be high to disable the output.

Figure 32. Read-Cycle Timing With $\overline{\text{RAS}}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION



† In early-write operations, DQ0 – DQ15 are all latched on the first falling edge of $\overline{\text{CASx}}$. Thus, $t_{su(DCL)}$ and $t_{h(CLD)}$ are referenced only to the first falling edge of $\overline{\text{CASx}}$.

Figure 33. Early-Write-Cycle Timing

Table 7. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

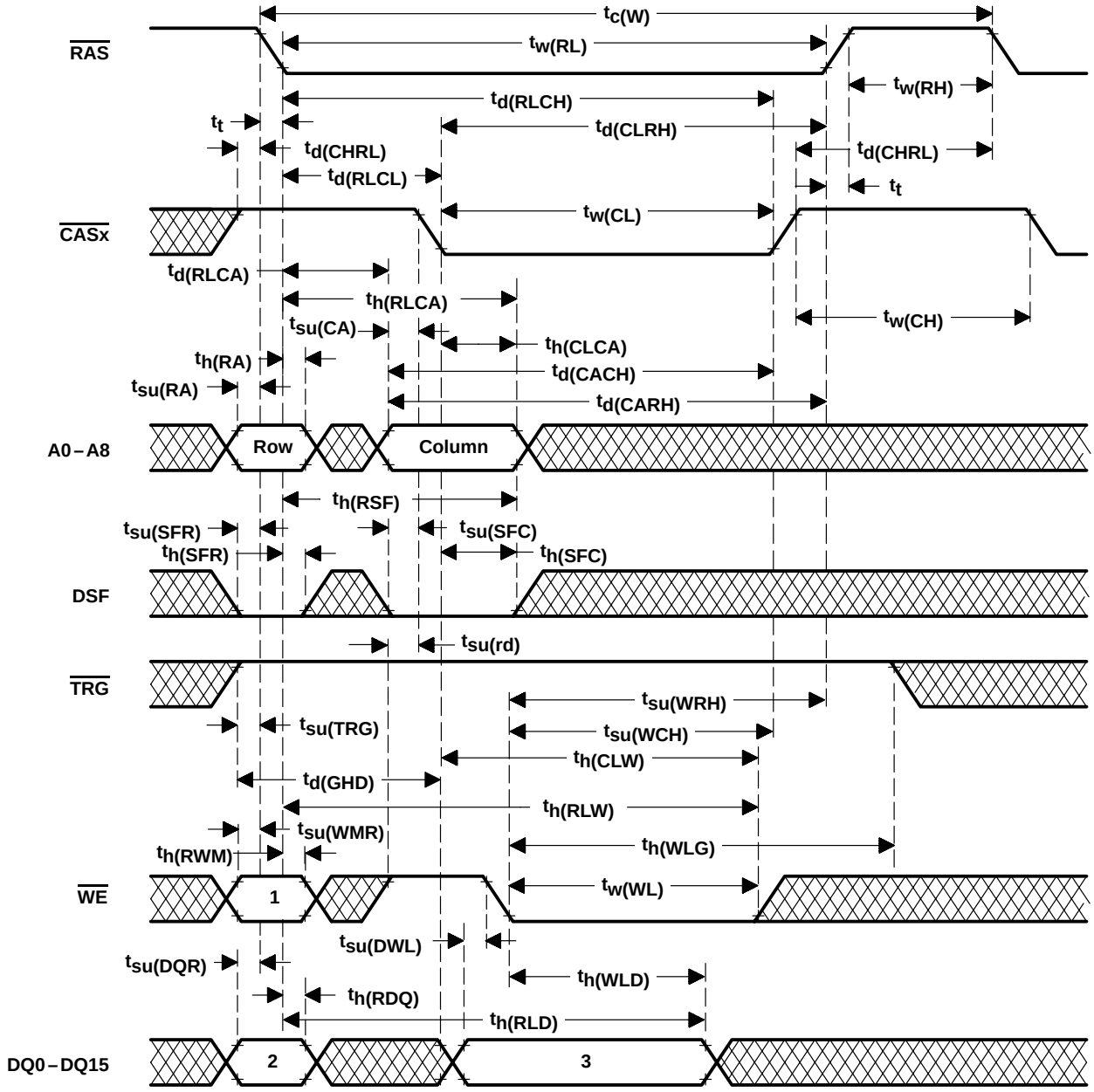


Figure 34. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 8. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

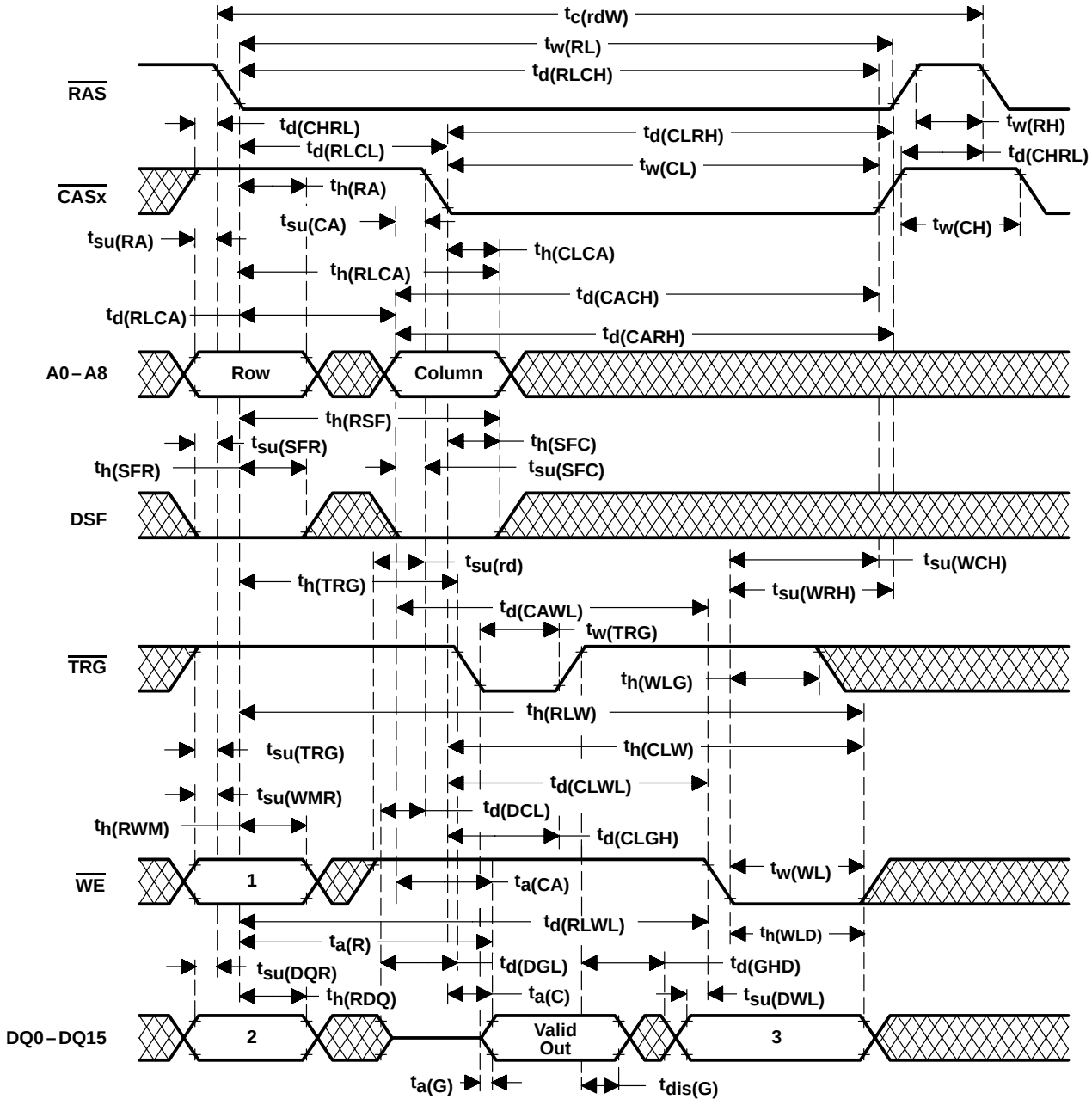
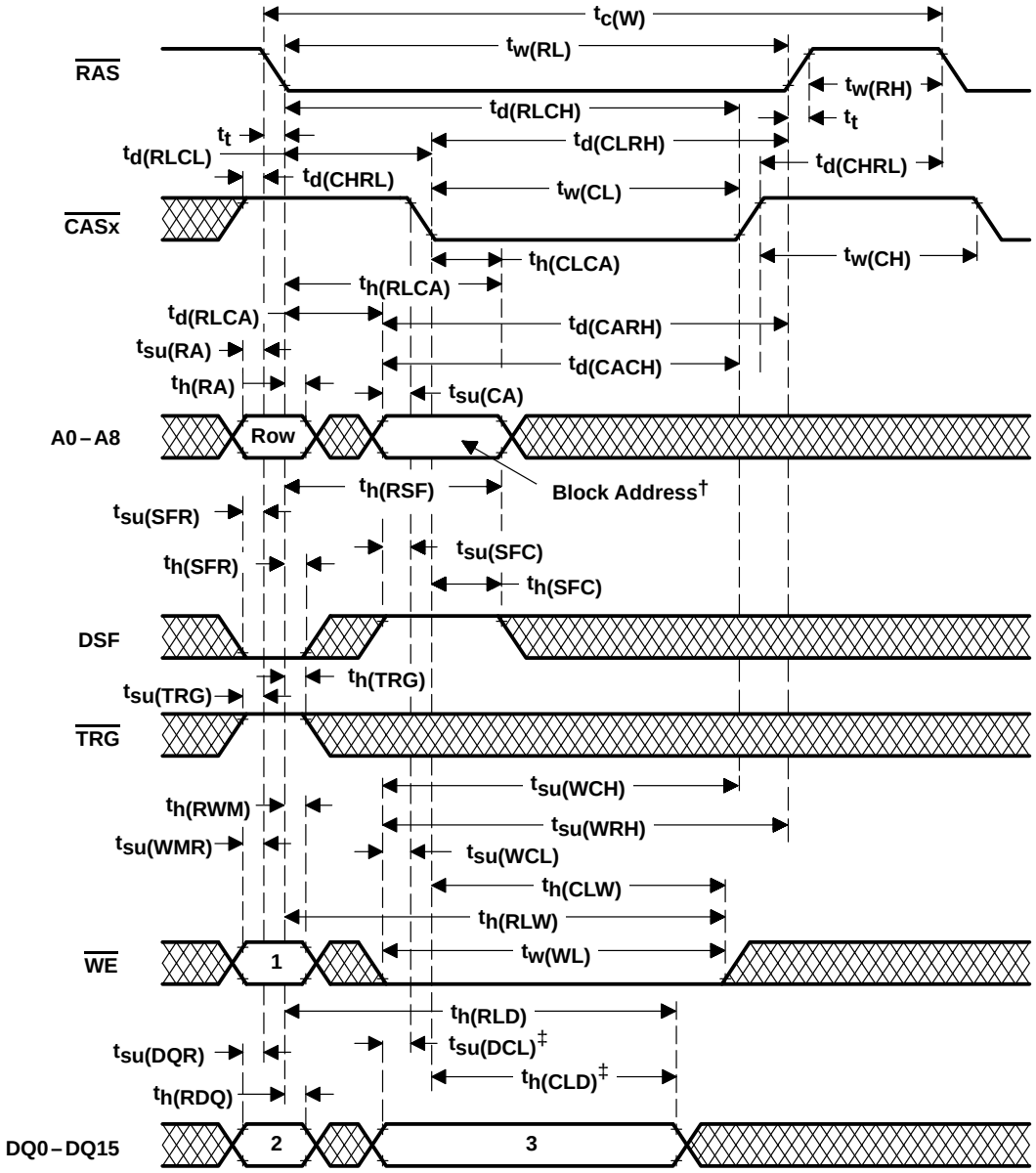


Figure 35. Read-Modify-Write-Cycle Timing

Table 9. Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION



† For 4-column block write (TMS5516x), block address is A2 – A8; for 8-column block write (TMS5517x), block address is A3 – A8.

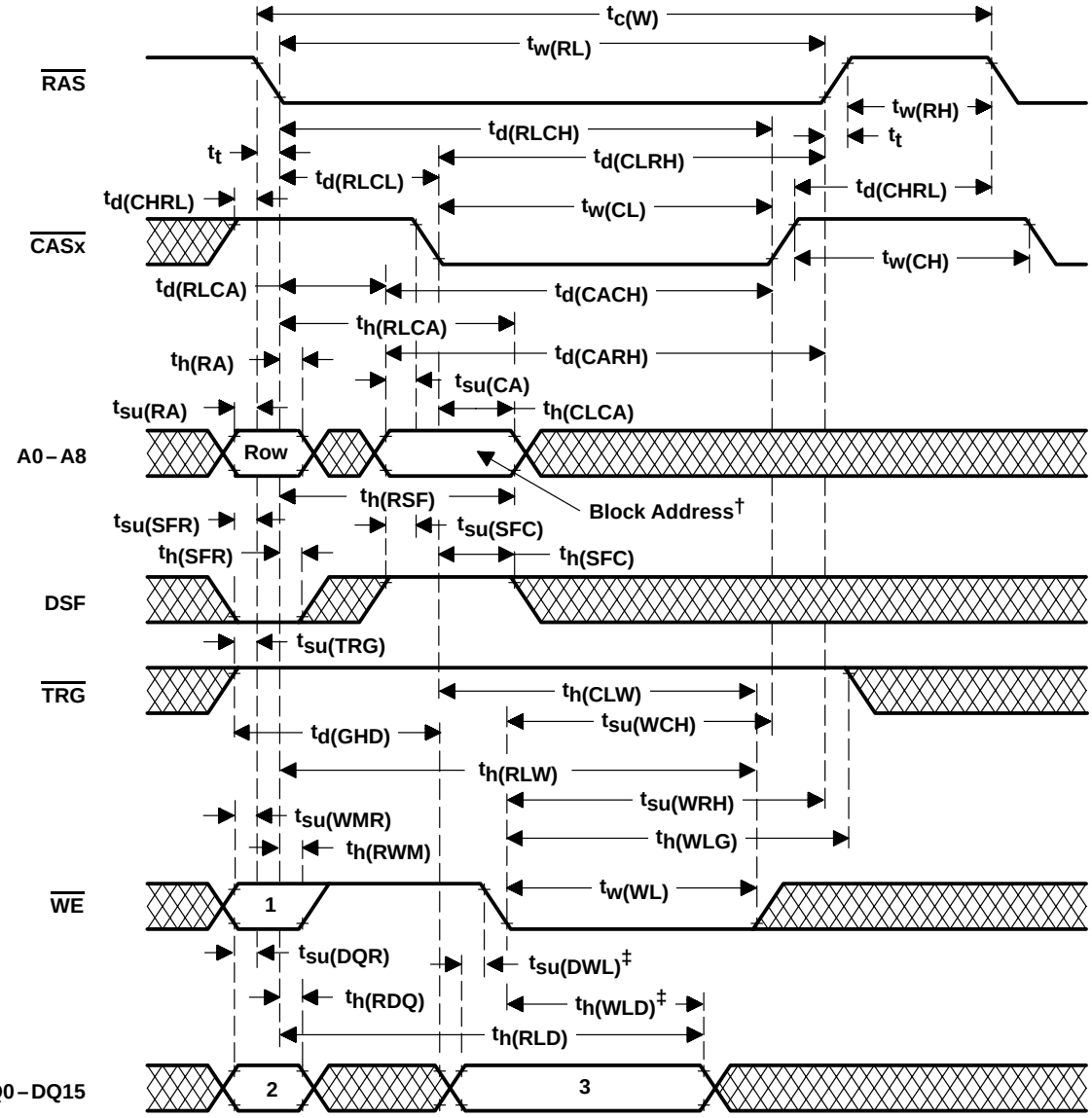
‡ In early-write operations, DQ0 – DQ15 are all latched on the first falling edge of $\overline{\text{CASx}}$. Thus, $t_{su(DCL)}$ and $t_{h(CLD)}$ are referenced only to the first falling edge of $\overline{\text{CASx}}$.

Figure 36. Block-Write-Cycle Timing (Early Write)

Table 10. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

PARAMETER MEASUREMENT INFORMATION



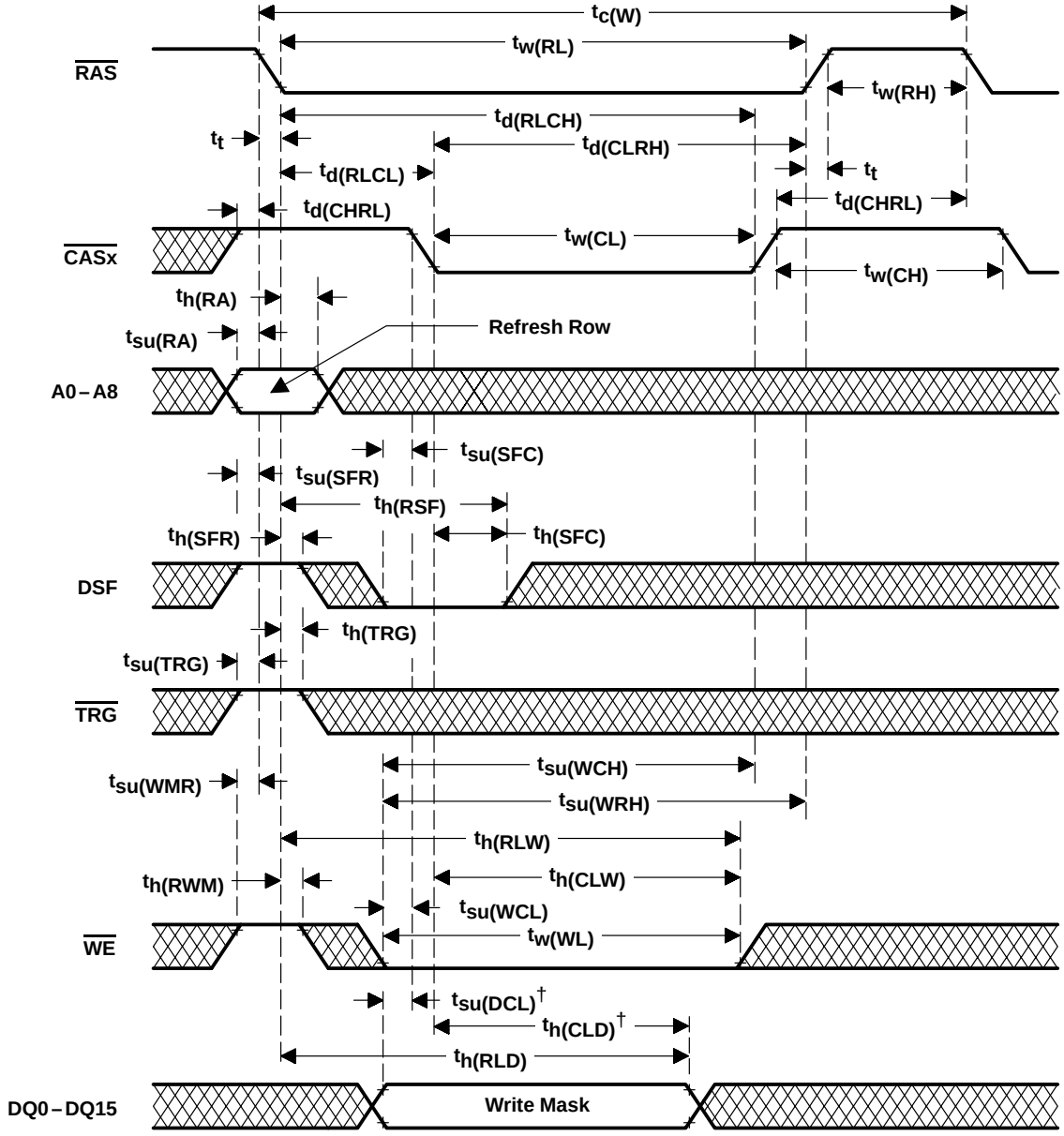
† For 4-column block write (TMS5516x), block address is A2–A8; for 8-column block write (TMS5517x), block address is A3–A8.
‡ In late-write operations, DQ0–DQ15 are all latched on the first falling edge of $\overline{WE}$. Thus $t_{su(DWL)}$ and $t_{h(WLD)}$ are referenced only to the first falling edge of $\overline{WE}$.

Figure 37. Block-Write-Cycle Timing (Late Write)

Table 11. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

PARAMETER MEASUREMENT INFORMATION



† In early-write operations, DQ0 – DQ15 are all latched on the first falling edge of CASx. Thus, $t_{su(DCL)}$ and $t_{h(CLD)}$ are referenced only to the first falling edge of CASx.

Figure 38. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

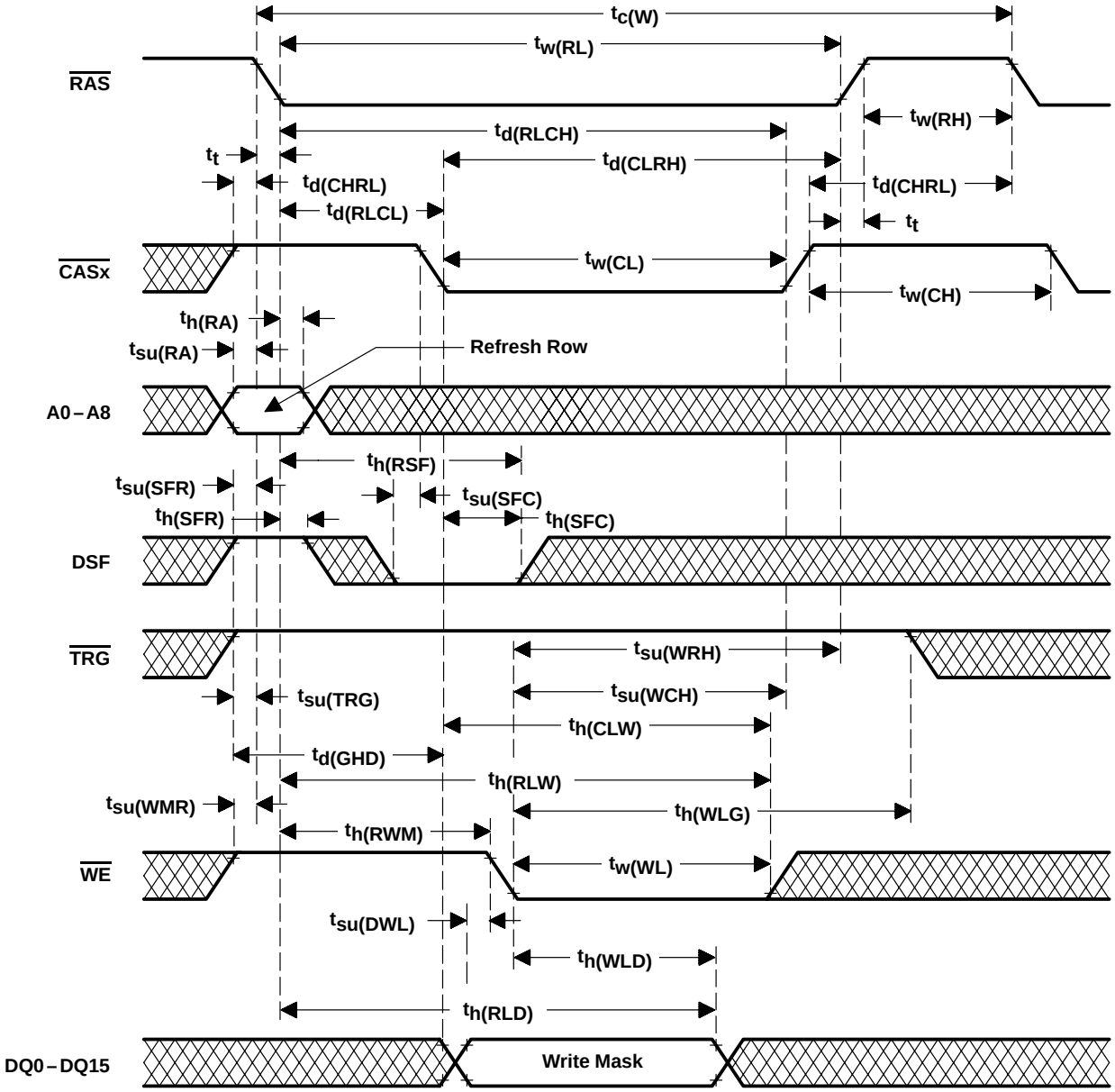
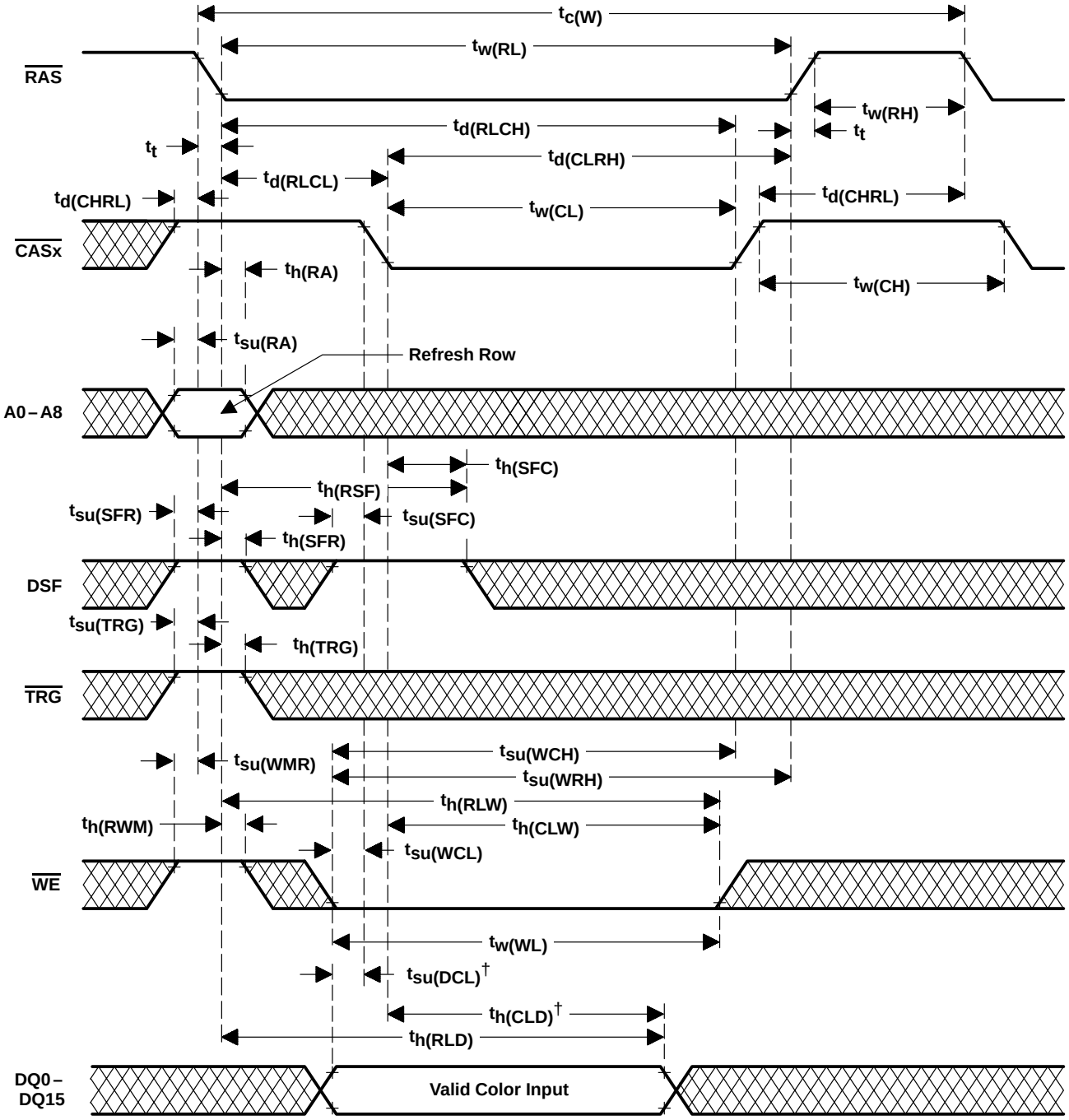


Figure 39. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION



† In early-write operations, DQ0 – DQ15 are all latched on the first falling edge of CASx. Thus, $t_{su(DCL)}$ and $t_{h(CLD)}$ are referenced only to the first falling edge of CASx.

Figure 40. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

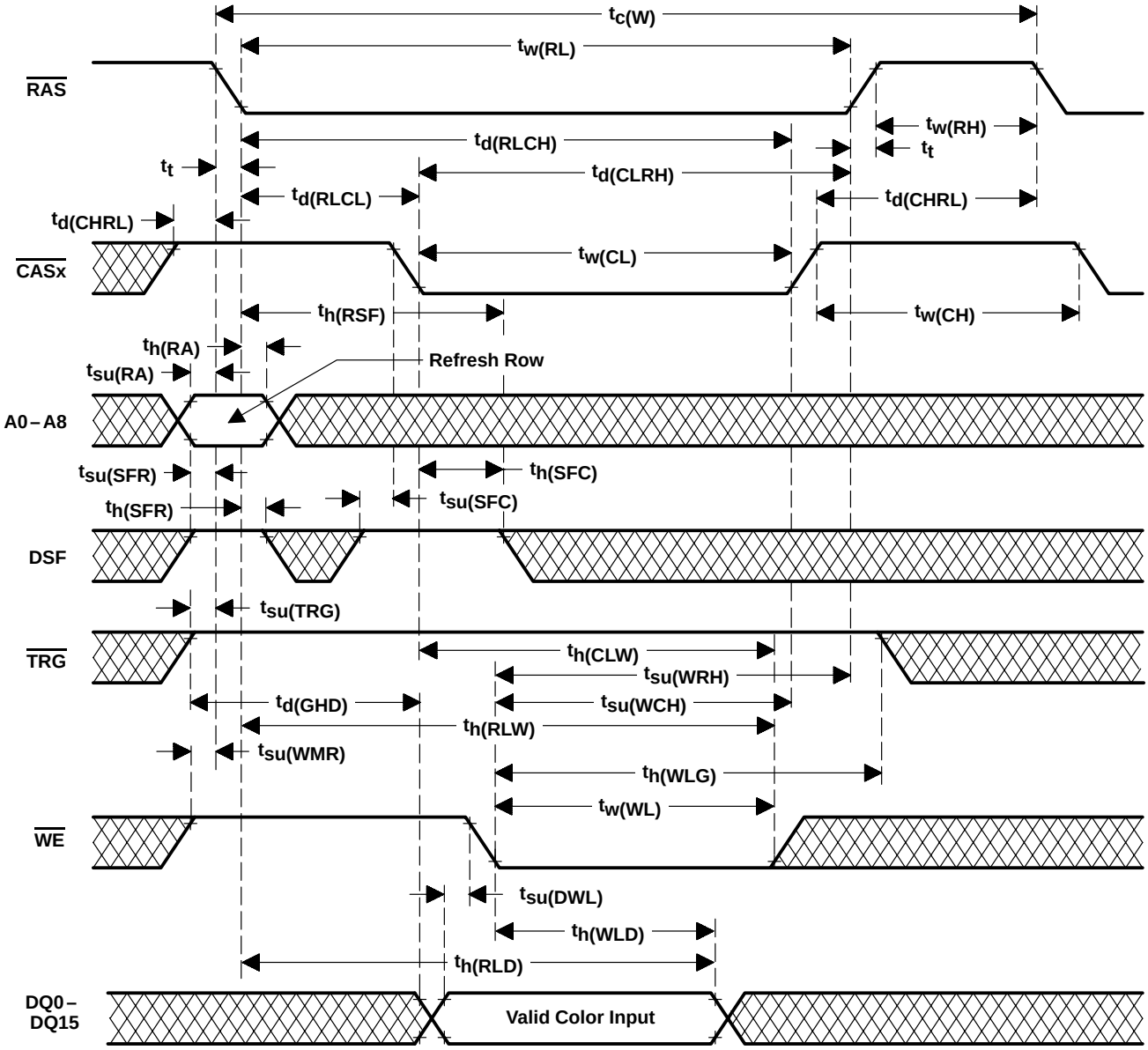
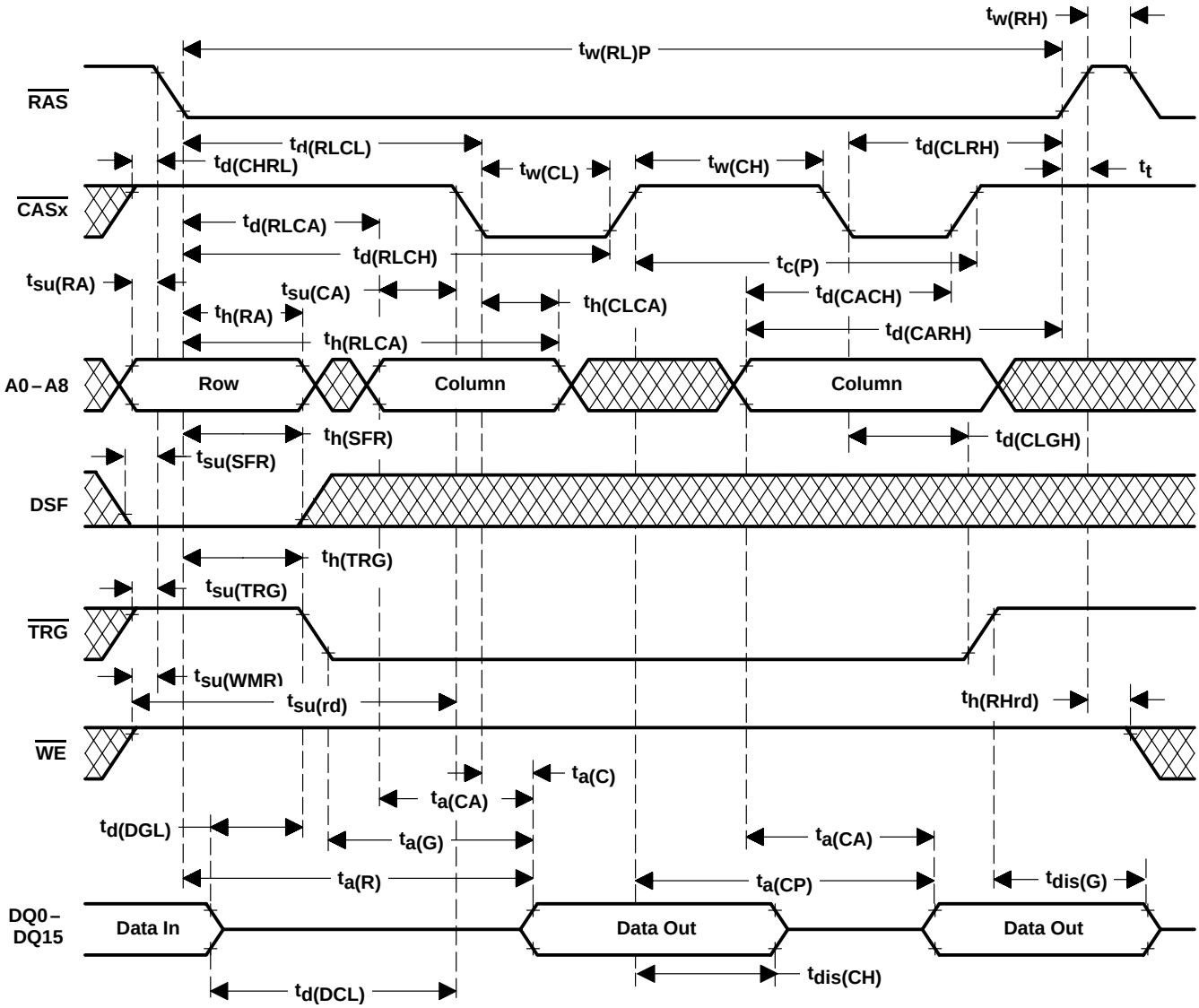


Figure 41. Load-Color-Register-Cycle Timing (Late-Write Load)

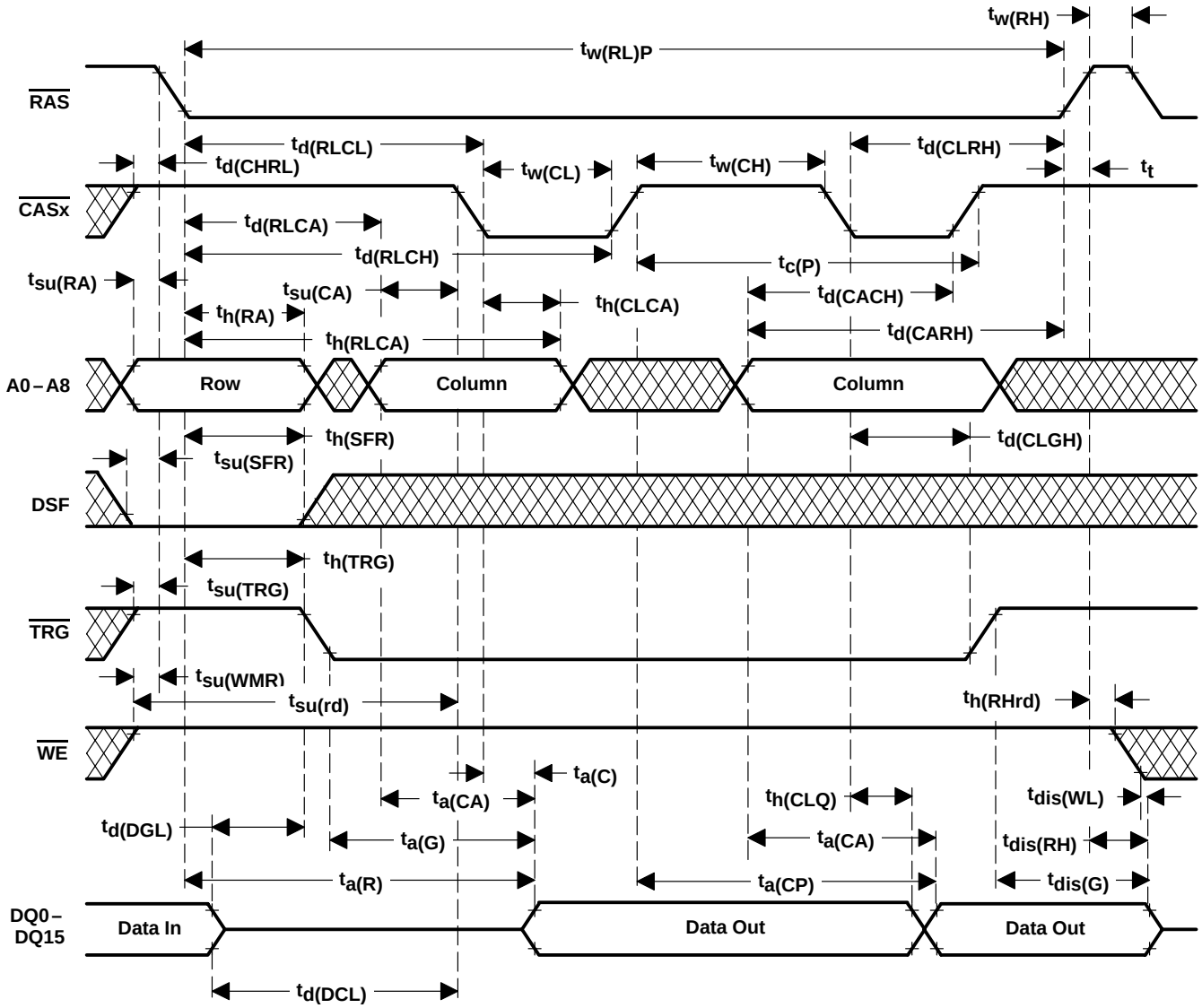
PARAMETER MEASUREMENT INFORMATION



NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper state of DSF is latched on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.).

Figure 42. Enhanced-Page-Mode Read-Cycle Timing (TMS551x0)

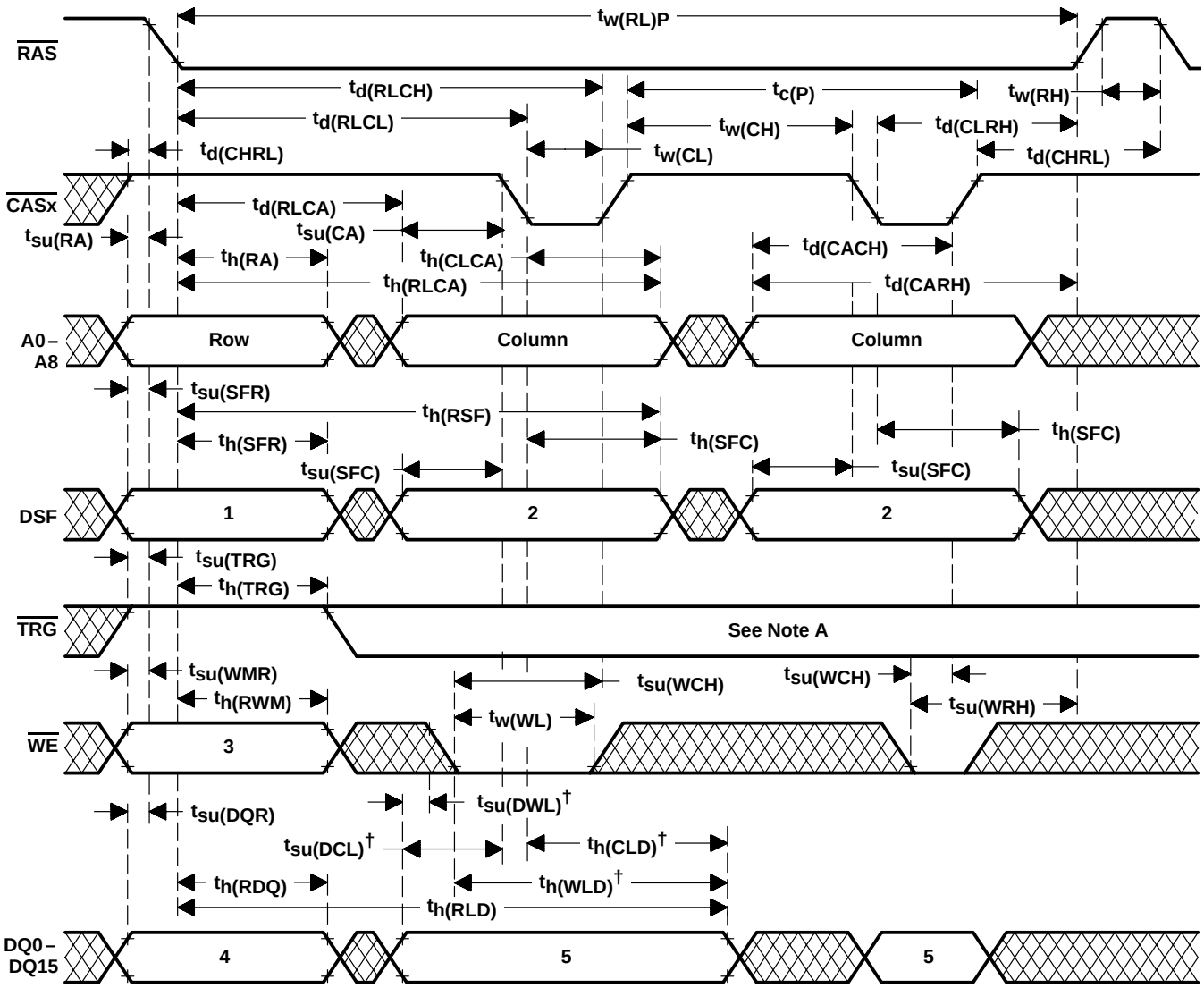
PARAMETER MEASUREMENT INFORMATION



NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write timing specifications are not violated and the proper state of DSF is latched on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.).

Figure 43. Extended-Data-Output Read-Cycle Timing (TMS551x1)

PARAMETER MEASUREMENT INFORMATION



† DQ0 – DQ15 are latched on either the falling edge of $\overline{WE}$ or the first falling edge of $\overline{CASx}$, whichever occurs later. In early-write operations, $t_{su(DWL)}$ and $t_{h(WLD)}$ are not applicable; $t_{su(DCL)}$ and $t_{h(CLD)}$ are referenced only to the first falling edge of $\overline{CASx}$. In late-write operations, $t_{su(DCL)}$ and $t_{h(CLD)}$ are not applicable.

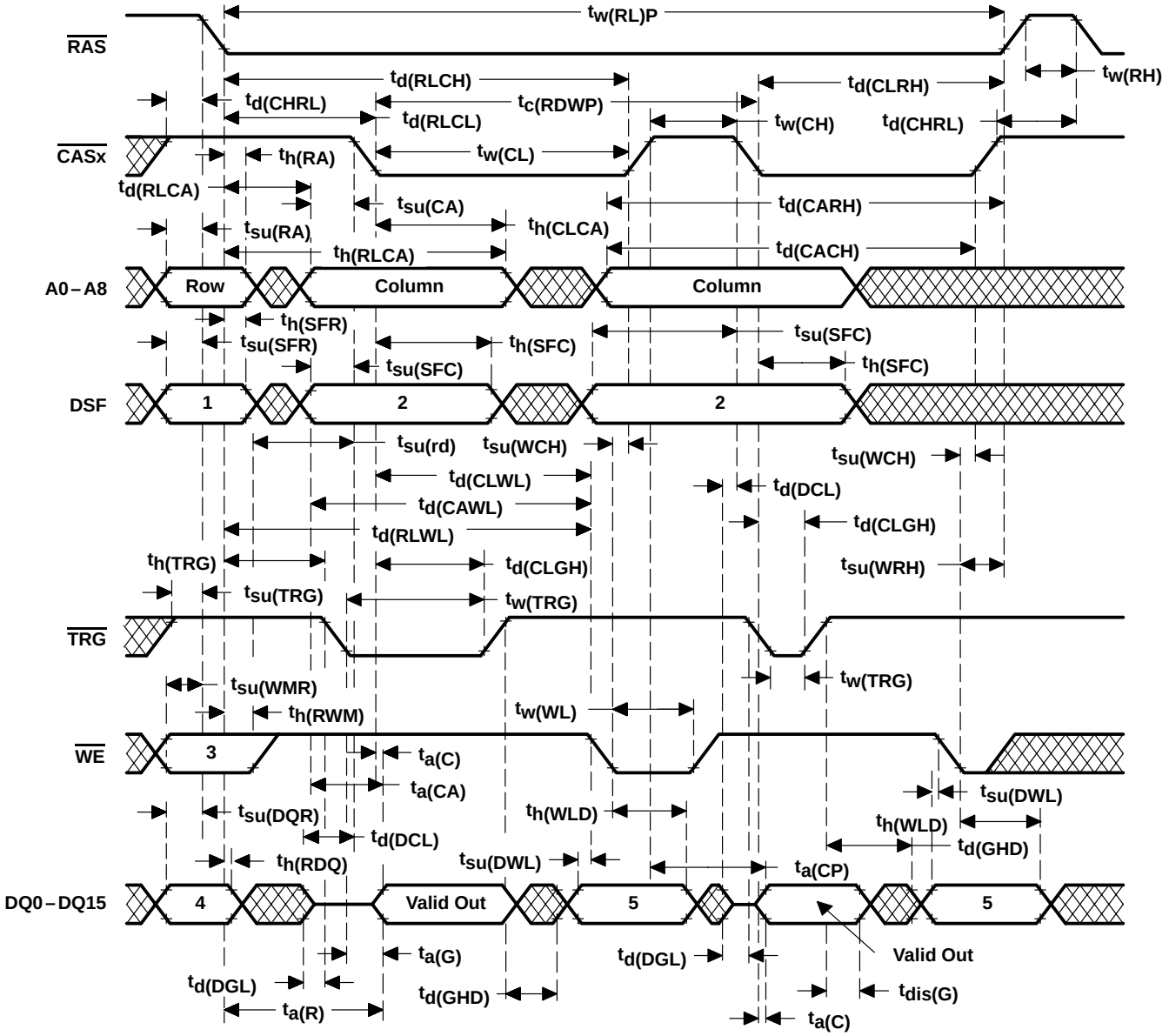
NOTE A: A read cycle or a read-modify-write cycle can be mixed with write cycles as long as read- and read-modify-write timing specifications are not violated.

Figure 44. Enhanced-Page-Mode Write-Cycle Timing

Table 12. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write-mask register on either the first falling edge of $\overline{WE}$ or the falling edge of $\overline{CASx}$, whichever occurs later.	H	L	H	Don't care	Write mask

PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a write cycle can be mixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 45. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 13. Enhanced Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write-mask register on either the first falling edge of $\overline{WE}$ or the falling edge of $\overline{CAS}$x, whichever occurs later.	H	L	H	Don't care	Write mask

PARAMETER MEASUREMENT INFORMATION

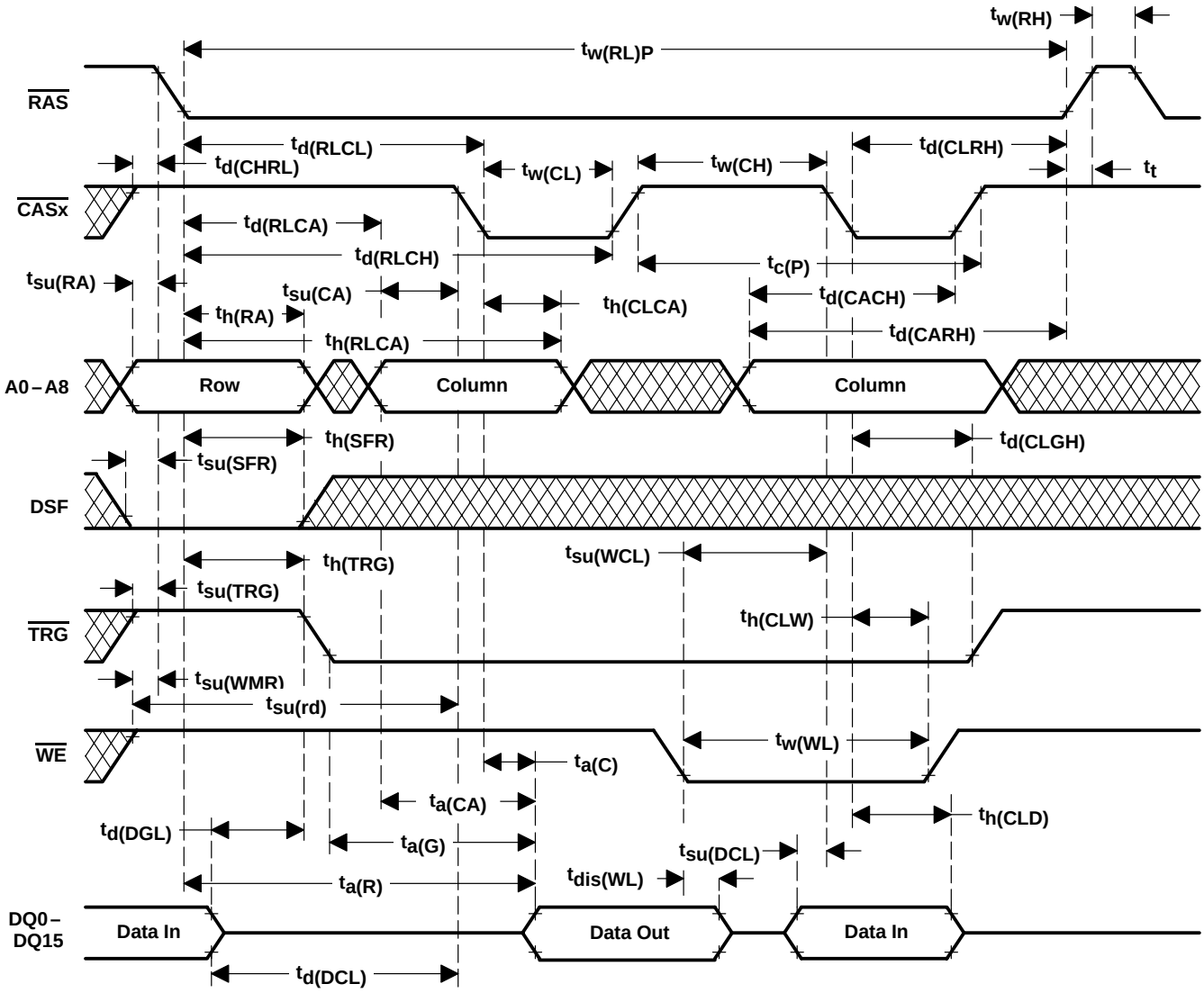
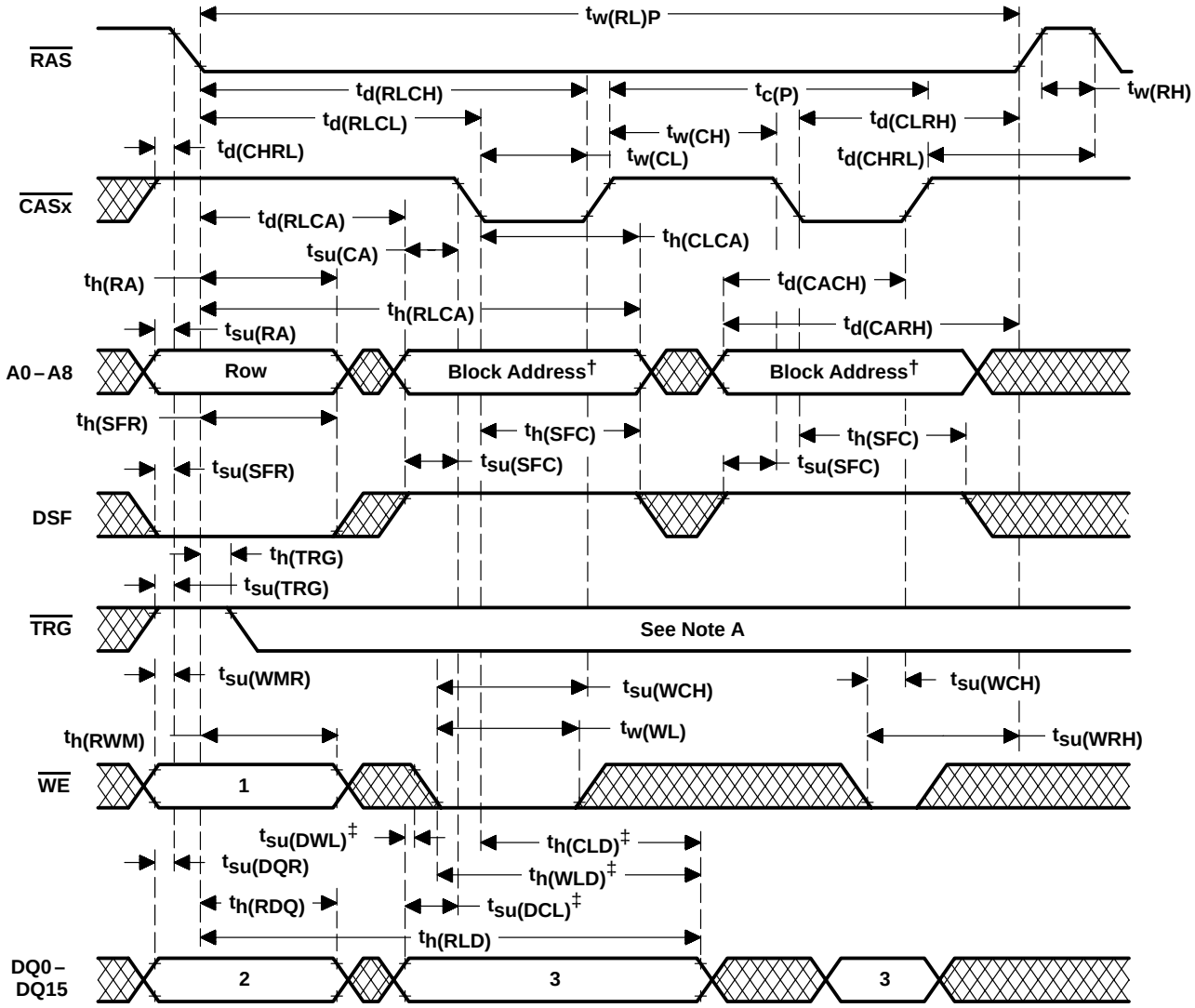


Figure 46. Extended-Data-Output Read-Followed-by-Write-Cycle Timing (TMS551x1)

PARAMETER MEASUREMENT INFORMATION



† For 4-column block write (TMS5516x), block address is A2 – A8; for 8-column block write (TMS5517x), block address is A3 – A8.

‡ DQ0 – DQ15 are latched on either the falling edge of $\overline{WE}$ or the first falling edge of $\overline{CASx}$, whichever occurs later. In early-write operations, $t_{su(DWL)}$ and $t_{h(WLD)}$ are not applicable; $t_{su(DCL)}$ and $t_{h(CLD)}$ are referenced only to the first falling edge of $\overline{CASx}$. In late-write operations, $t_{su(DCL)}$ and $t_{h(CLD)}$ are not applicable.

NOTE A: A read cycle or a read-modify-write cycle can be mixed with write cycles as long as read- and read-modify-write timing specifications are not violated.

Figure 47. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 14. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

PARAMETER MEASUREMENT INFORMATION

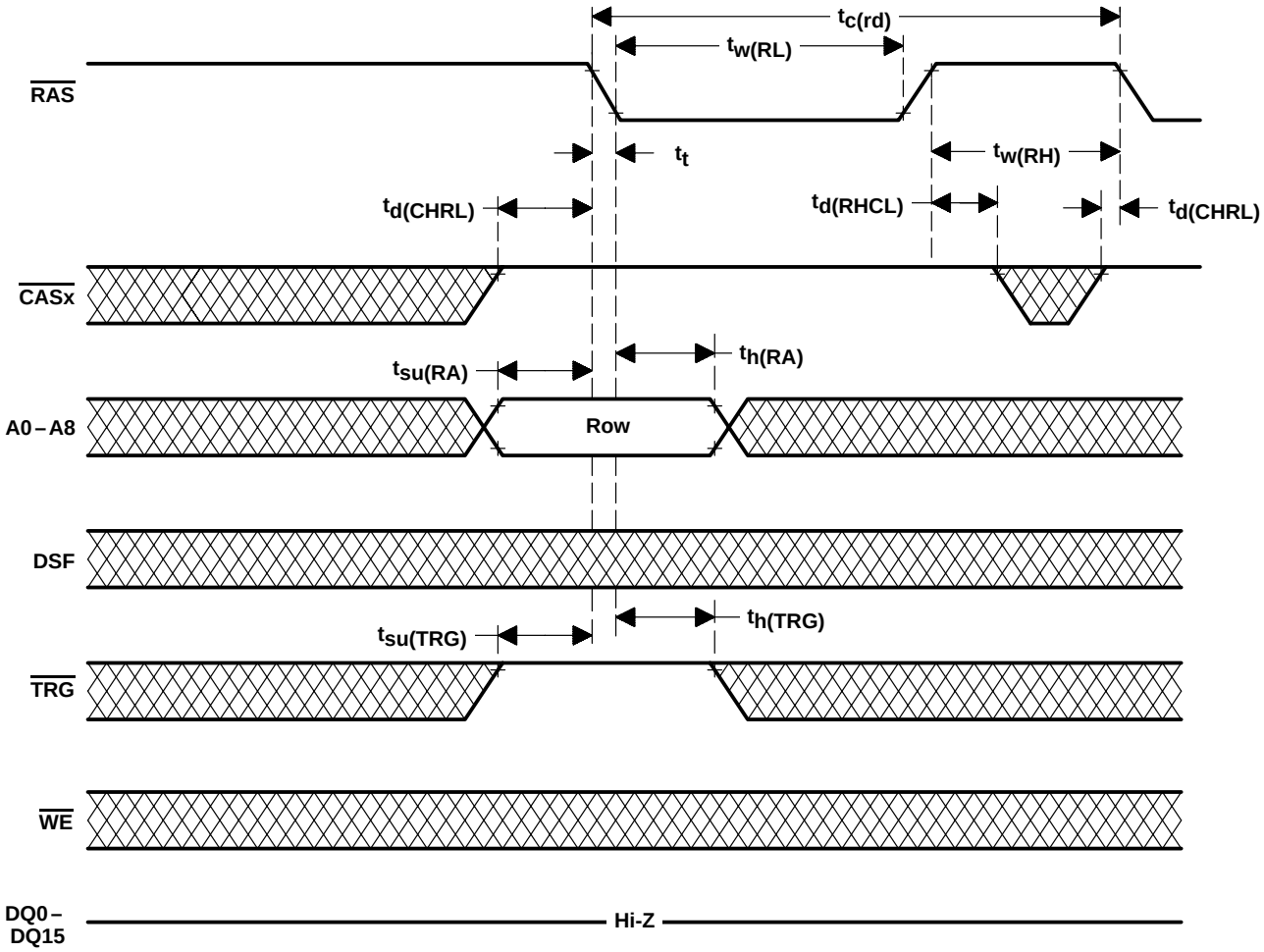


Figure 48. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

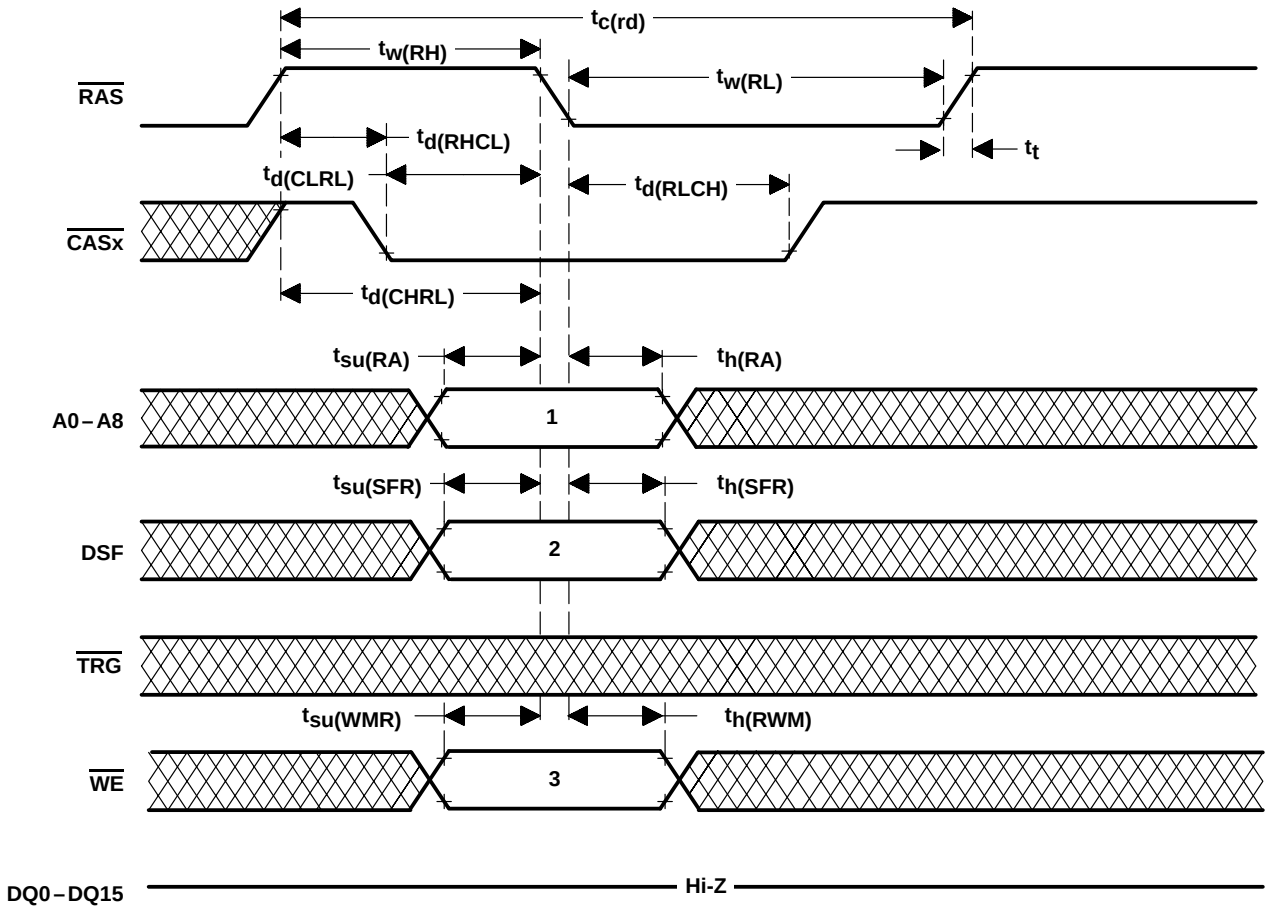


Figure 49. CBR-Refresh-Cycle TIming

Table 15. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset (CBRN)	Don't care	H	H
CBR refresh with stop point set and no reset (CBRS)	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

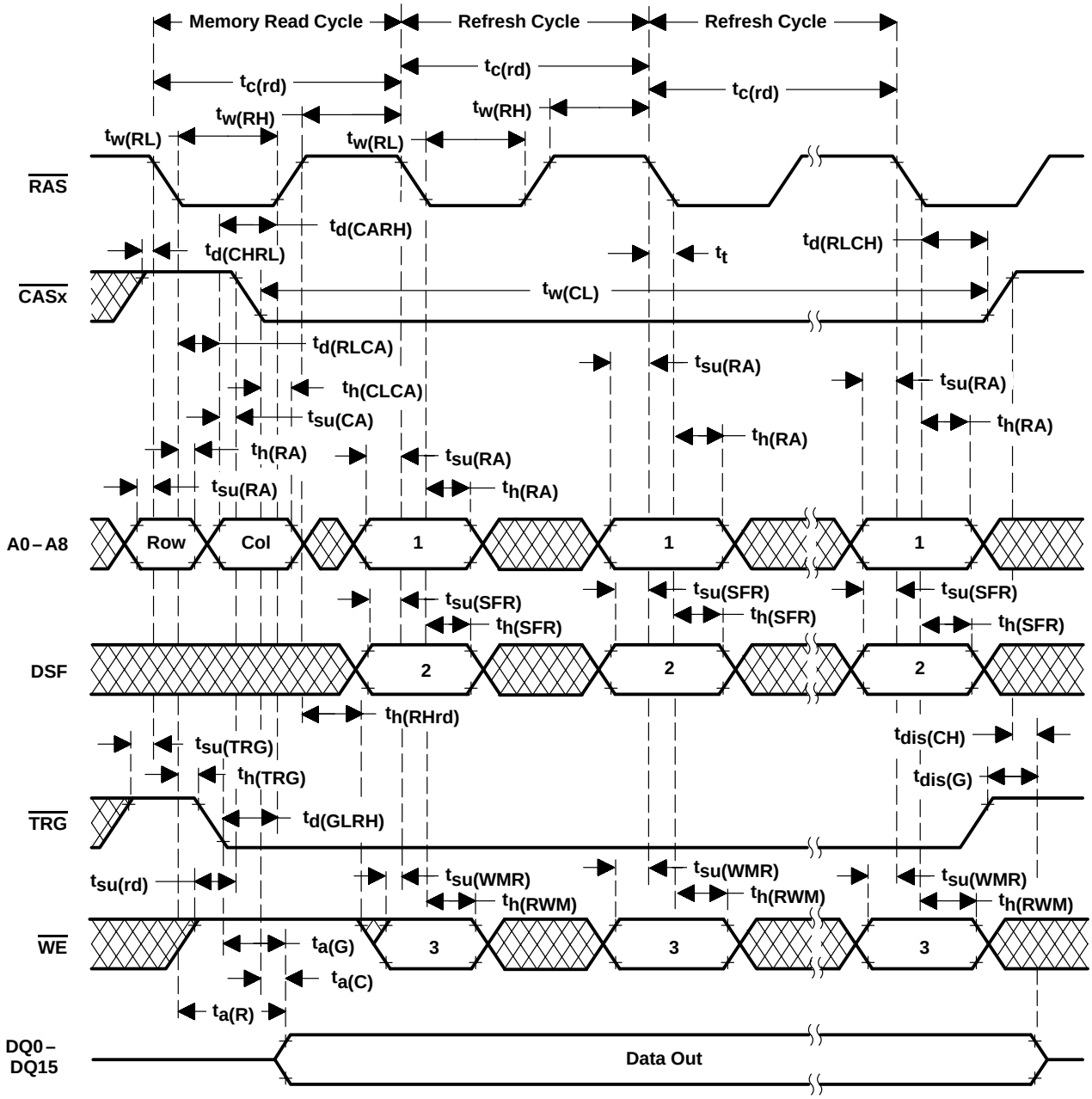
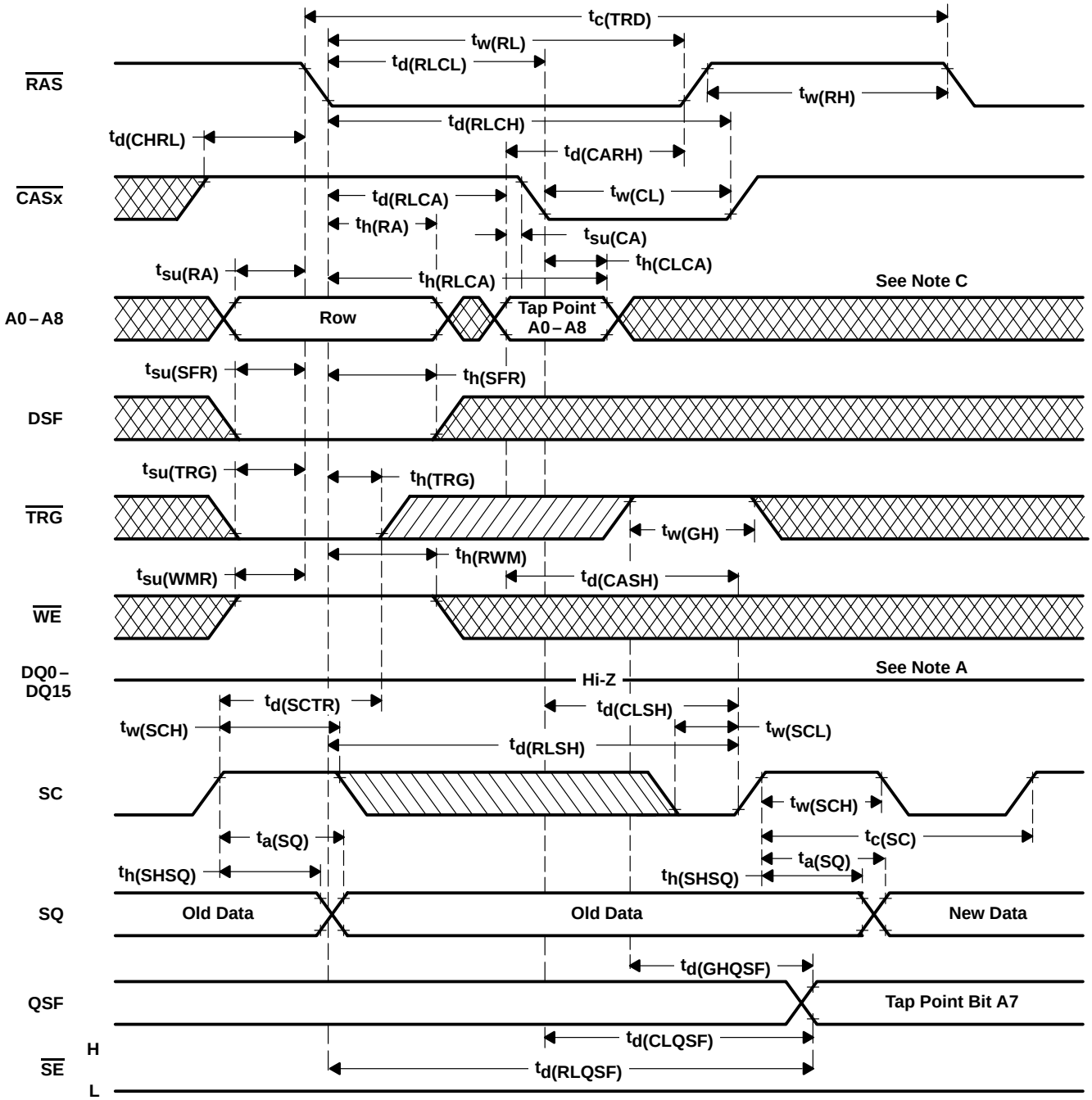


Figure 50. Hidden-Refresh-Cycle Timing

Table 16. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset (CBRN)	Don't care	H	H
CBR refresh with stop point set and no option reset (CBRS)	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory-to-data-register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

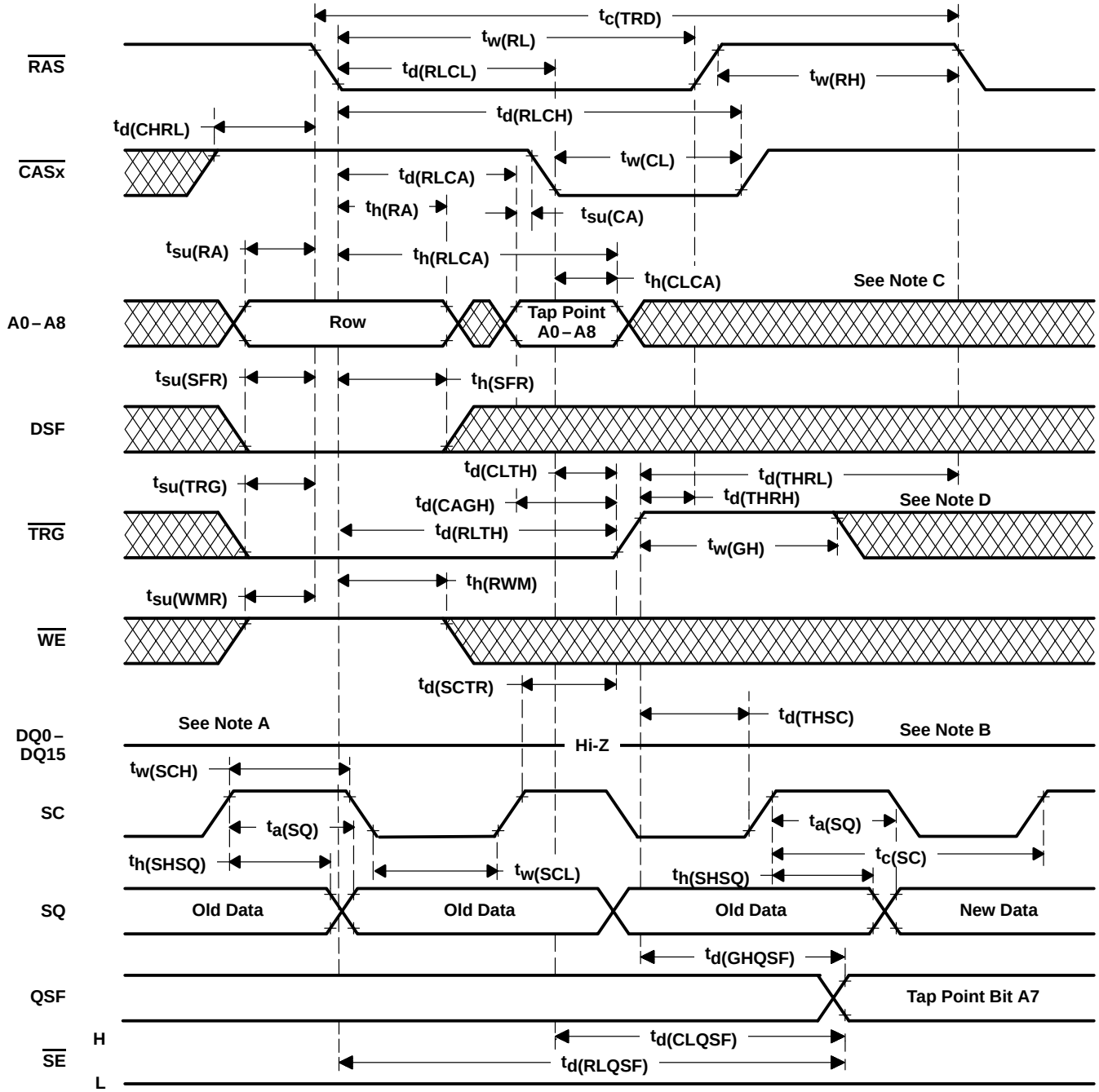
B. Once data is transferred into the data registers, SAM is in the serial-read mode (that is, SQx is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the DRAM half of the row

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 51. Full-Register-Transfer Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register-transfer cycle. The memory to data register-transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

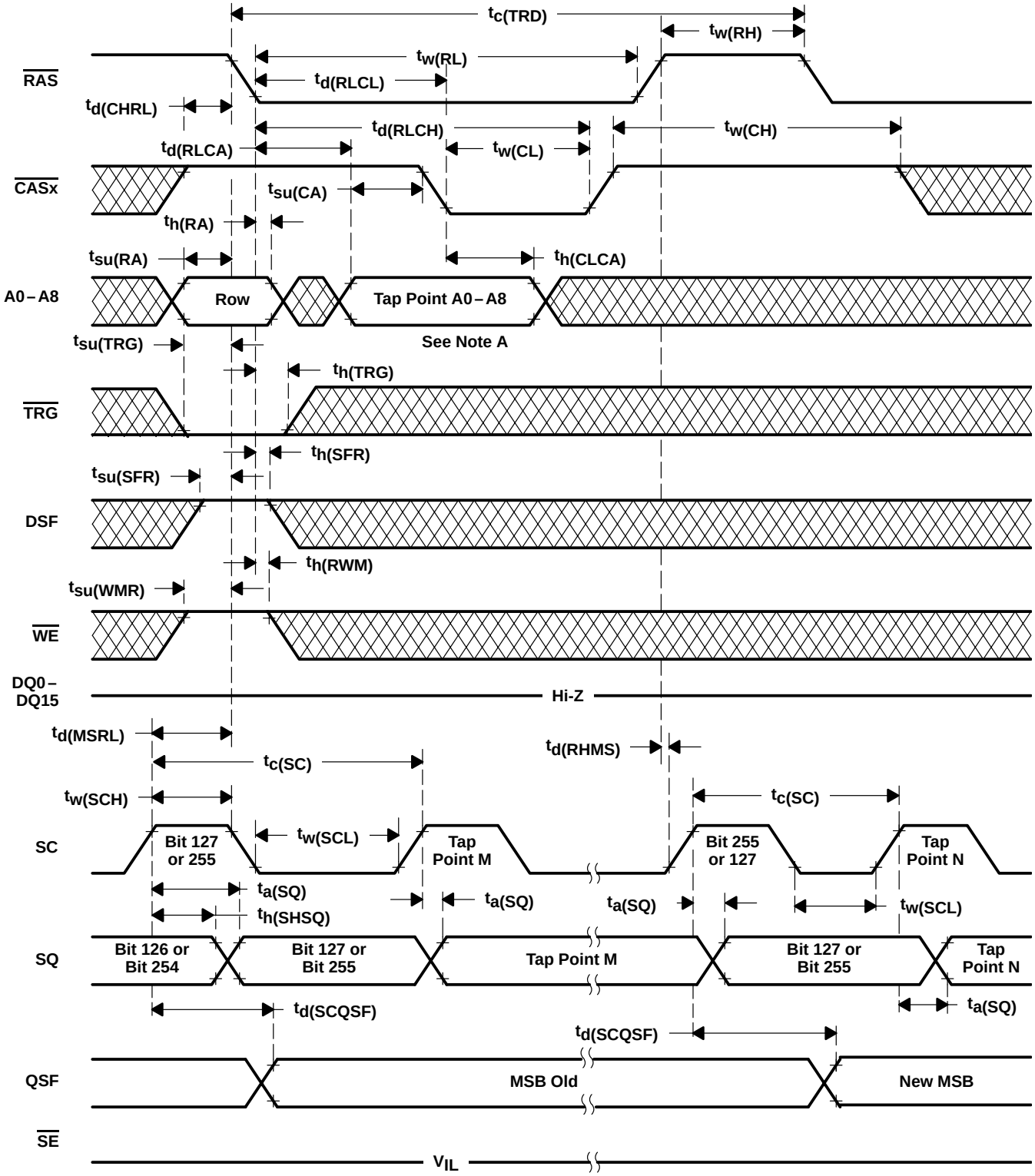
B. Once data is transferred into the data registers, SAM is in the serial-read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after TRG has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the DRAM half of the row

D. Late-load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 52. Full-Register-Transfer Read Timing, Real-Time Load Operation/Late-Load Operation

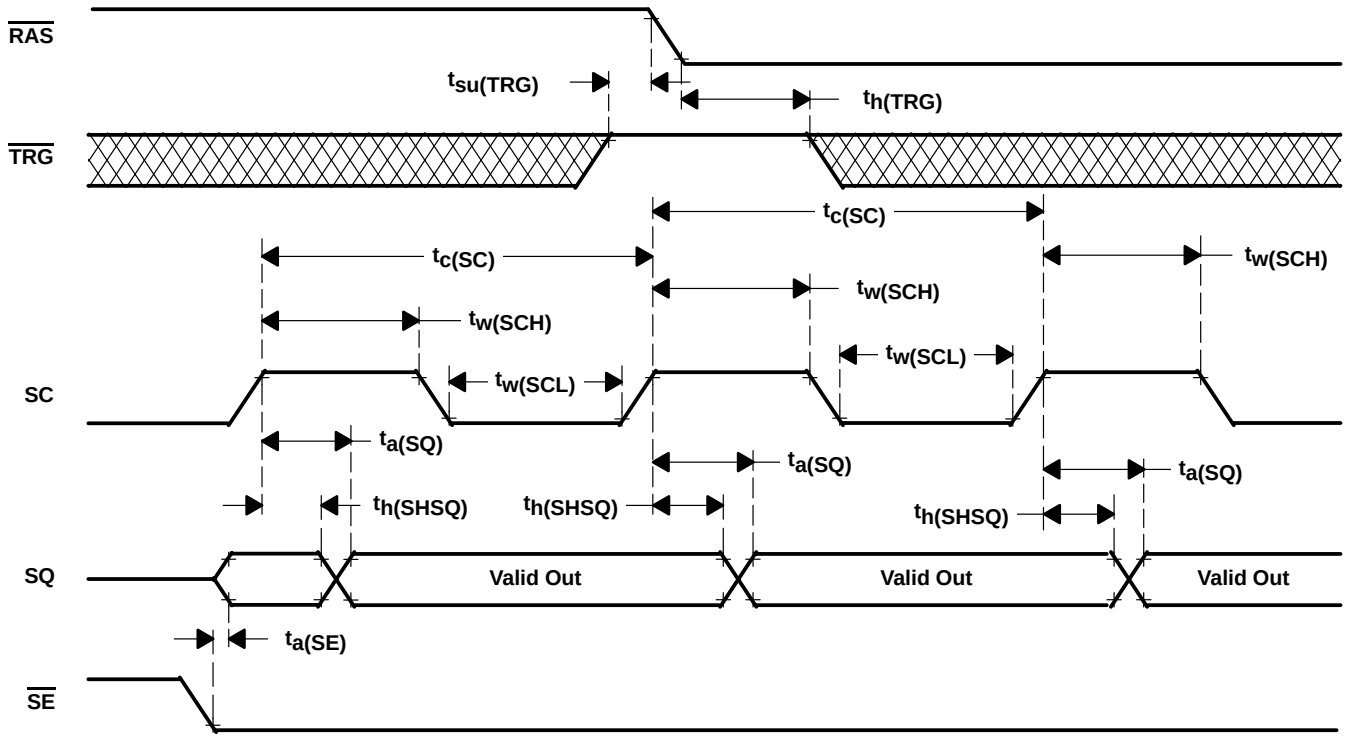
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0 – A6: tap point of the given half; A7: don't care; A8: identifies the DRAM half of the row

Figure 53. Split-Register-Transfer Read Timing

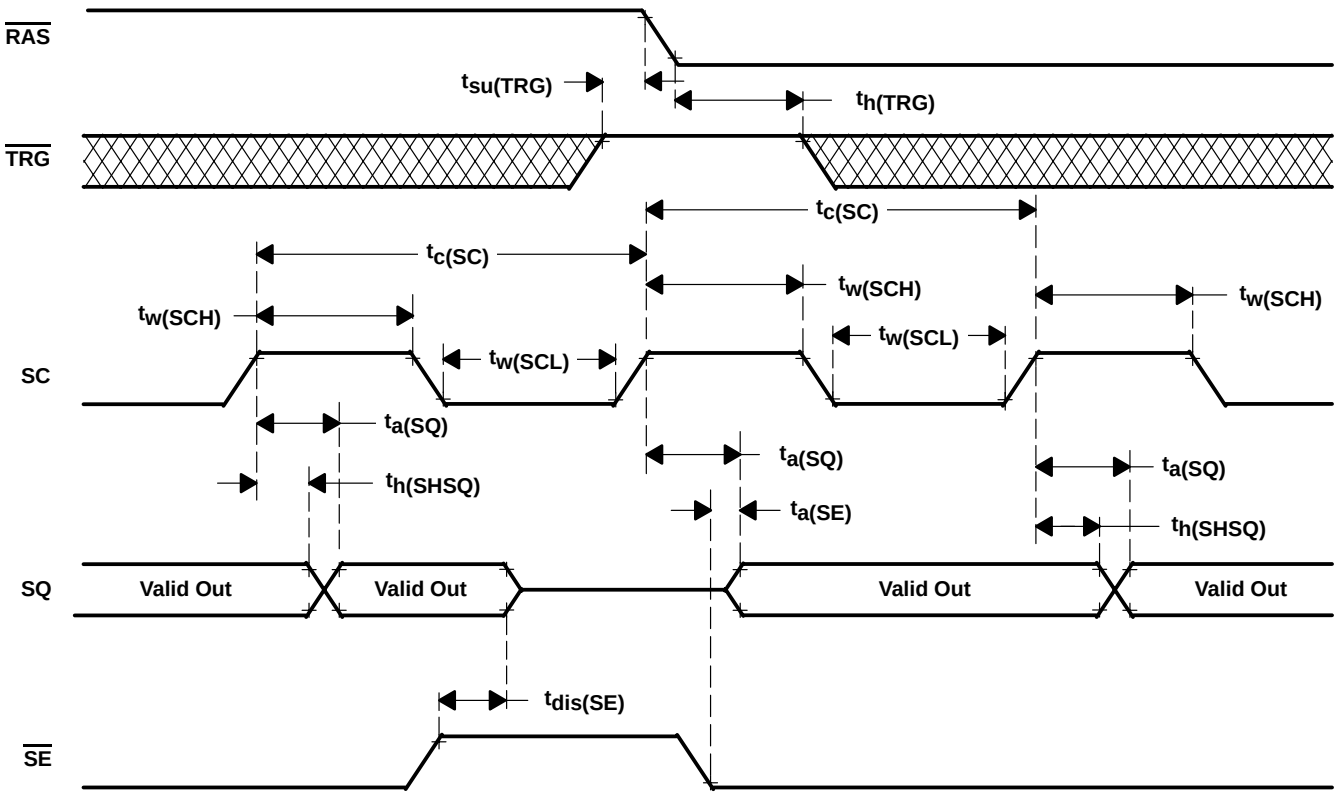
PARAMETER MEASUREMENT INFORMATION



NOTE A: While reading data through the serial-data register, $\overline{TRG}$ is a don't care, except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 54. Serial-Read Timing ($\overline{SE}$ = V_{IL})

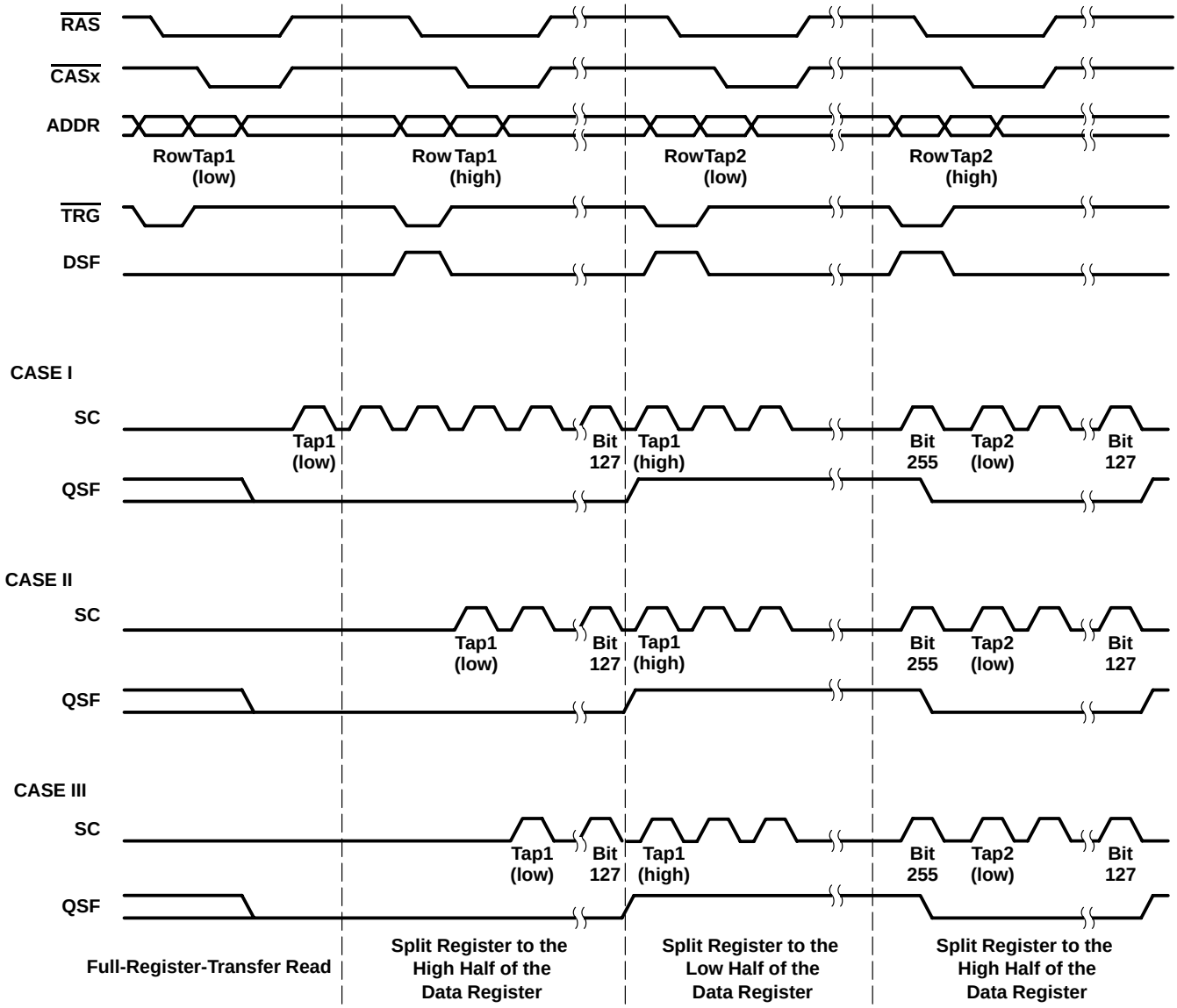
PARAMETER MEASUREMENT INFORMATION



NOTE A: While reading data through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 55. Serial-Read Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION



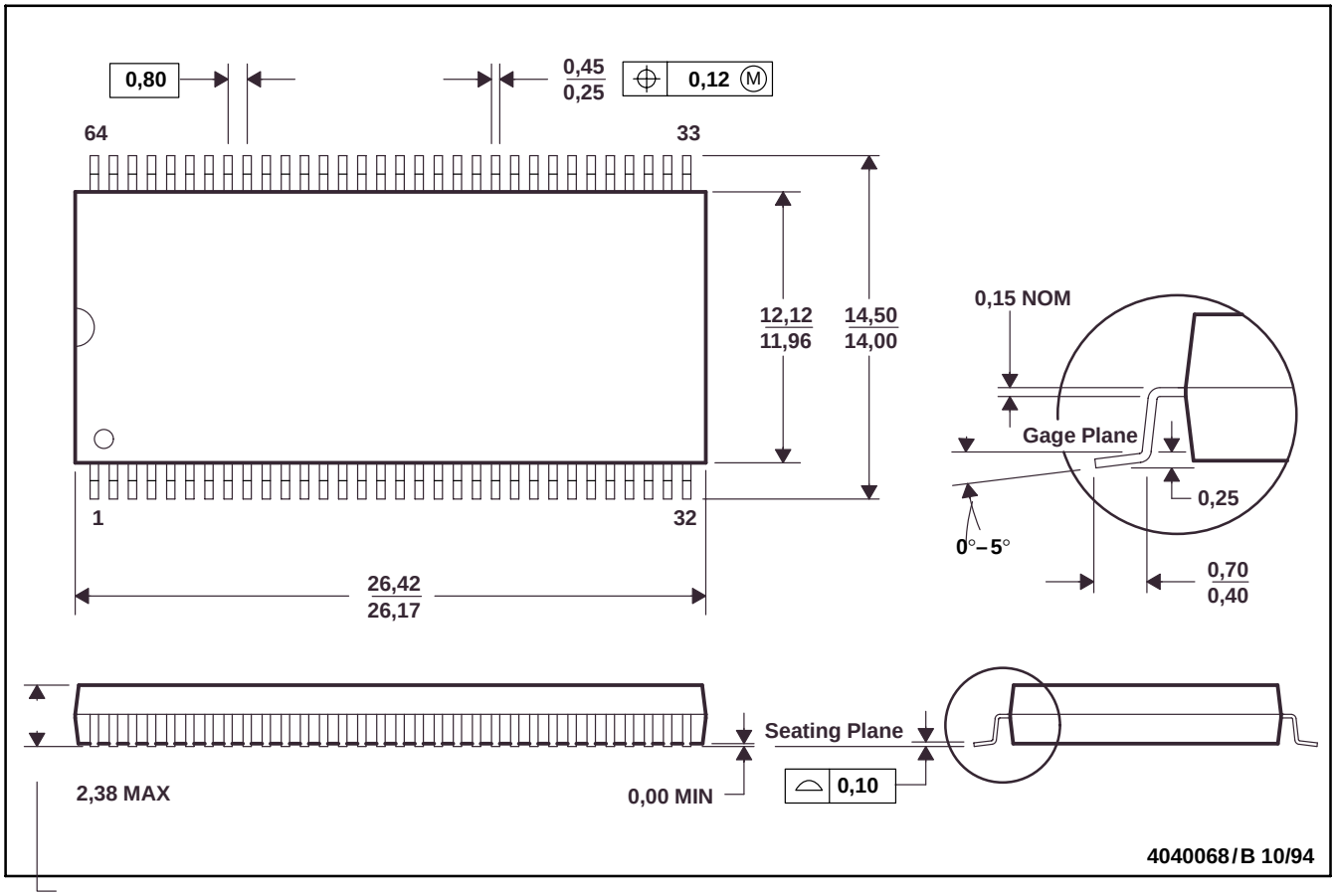
NOTES: A. In order to achieve proper split-register operation, a full-register-transfer read should be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the full-register-transfer read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register-transfer read cycle and the first split-register cycle.

B. A split-register-transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half. After the $t_{d(MSRL)}$ is met, the split-register-transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

Figure 56. Split-Register Operating Sequence

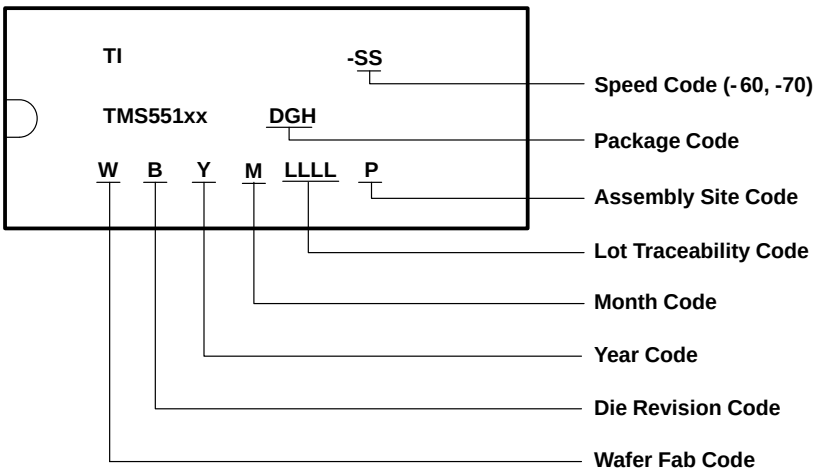
MECHANICAL DATA

DGH (R-PDSO-G64) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold flash or protrusion. Maximum mold protrusion is 0,125.

device symbolization



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265