JW7260

High-side Single ORing Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®7260 is a positive voltage ideal diode-OR controller that drives an external N-channel MOSFET. Forming the diode-OR with N-channel MOSFETs instead of Schottky diodes reduces power consumption, heat dissipation and PC board area.

With the JW7260, power sources can easily be ORed together to increase total system reliability.

In the forward direction the JW7260 controls the voltage drop across the MOSFET to ensure smooth current transfer from one path to the other without oscillation. If a power source fails or is shorted, fast turnoff minimizes reverse current transients.

JW7260 is available in TSOT23-6 Package

FEATURES

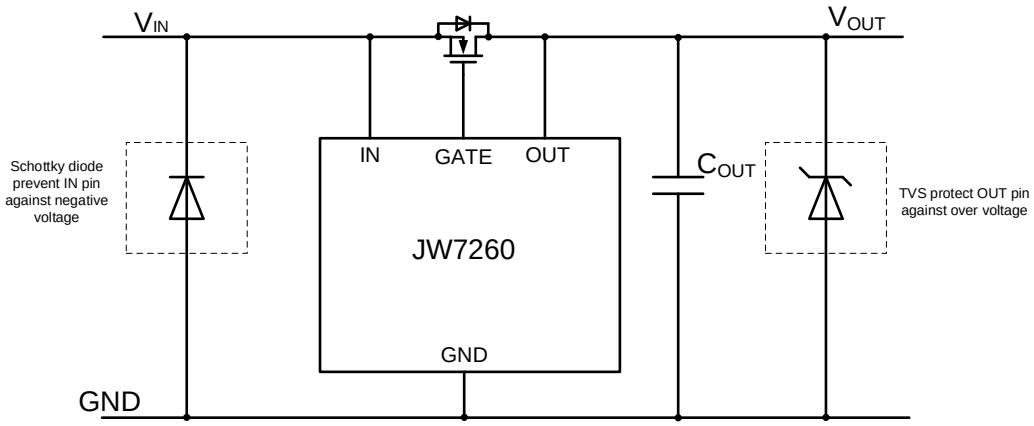
- Replaces power schottky diodes
- Controls external N-Channel MOSFET
- 0.3μs turn-off time limits peak fault current
- Wide operating voltage range: 6V to 80V
- 100-V transient capability
- Smooth switchover without oscillation
- No reverse DC current
- 1-A Peak gate turnoff current
- Available in TSOT23-6 package

APPLICATIONS

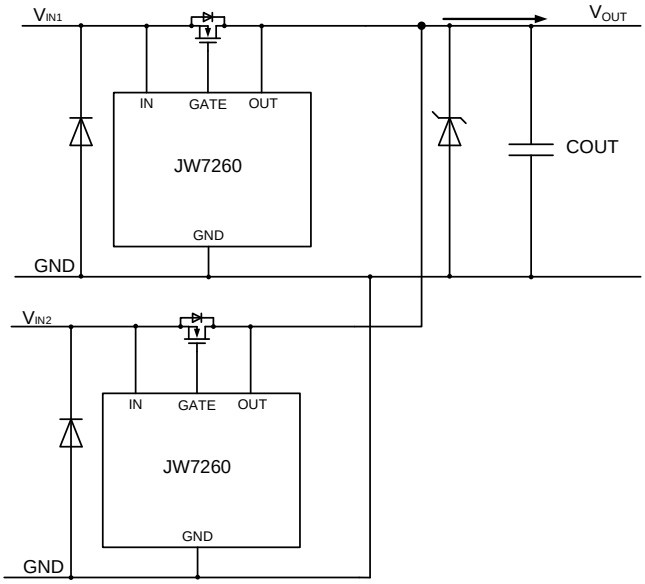
- High Availability Systems
- Advanced TCA® (ATCA) Systems
- +48V and –48V Distributed Power Systems
- Telecom Infrastructure
- Active ORing of Redundant(N+1) Power Supplies

TYPICAL APPLICATION

Typical Application



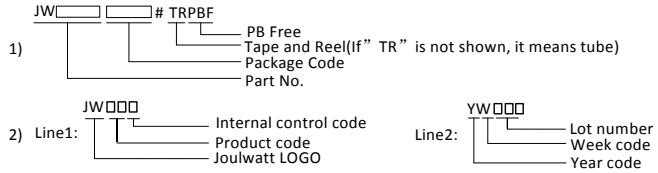
Typical Application



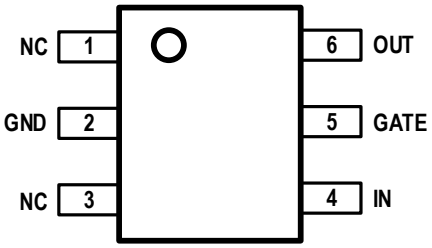
ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW7260TSOTB#TRPBF	TSOT23-6	JWFE□ YW□□□

Note：



PIN CONFIGURATION



TSOT23-6

ABSOLUTE MAXIMUM RATING[1)2)]

IN PIN Voltage ..... -1V to 100V
OUT PIN Voltage.....-0.3V to 100V
GATE Pins Voltage[3)].....IN-1V to IN+13V
Storage Temperature Range .....-65ºC to 150ºC
Lead Temperature(Soldering,10 sec) 300ºC
Junction Temperature[4)]……..150 ºC
ESD Susceptibility (Human Body Model) .....±2kV
ESD Susceptibility (Charged Device Model) .....±750V

RECOMMENDED OPERATING CONDITIONS[5)]

IN PIN Voltage ..... 6V to 80V
OUT PIN Voltage.....6V to 80V
Operation Junction Temperature…….-40~125ºC

THERMAL PERFORMANCE[6)]

	θ_{JA}	θ_{Jc}
TSOT23-6….....	110	55ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDITIONS.
2) All currents into pins are positive, all voltage are referenced to GND unless otherwise specified.
3) The GATE pins are internally limited to a minimum of 13V above IN. Driving these pins beyond the clamp may damage the part.
4) The JW7260 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

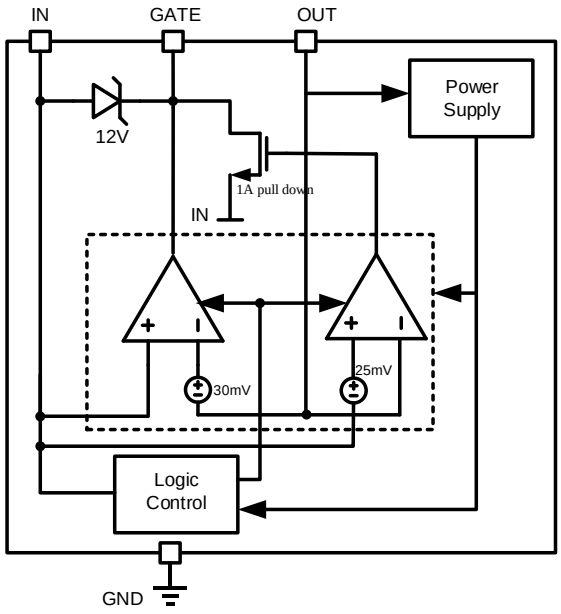
T_J = -40°C~125°C, 6V<V_{OUT}<80V unless otherwise stated.							
Item	**Symbol**	**Condition[5)]**		**Min.**	**Typ.**	**Max.**	**Units**
Operating Supply Range	V_{OUT}			6		80	V
Supply Current	I_{OUT}				540	700	uA
Input Voltage Range	V_{IN}			6		80	V
In Pin Iinput Current	I_{IN}	GATE High			0.6	0.8	mA
External N-Channel Gate Drive(V_{GATE}-V_{IN})	ΔV_{GS}	VOUT=20V to 80V		10	12	16	V
		VOUT=6V to 20V		3.5		15	
External N-Channel Gate Pull-Up Current	$I_{GATEX(UP)}$	V_{GATE}=V_{IN}	V_{IN}=80V	-100	-200	-300	uA
		V_{IN}-V_{OUT}=100mV	V_{IN}=6V	-25	-40	-55	
External N-Channel Gate Pull-Down in Fault Condition	$I_{GATEX(DN)}$	Gate Drive Off, V_{GATE}=V_{IN}+5V		1			A
Gate Turn-Off Time[7)]	t_{OFF}	V_{IN}-V_{OUT}=55mV ⌉-1V, V_{GATE}-V_{IN}<1V			0.3		us
Source-Drain Regulation Voltage(V_{IN}-V_{OUT})	ΔV_{SD}			15	30	50	mV
Reverse V_{SD} Threshold	$V_{SD(REV)}$			-10	-25	-50	mV

7) Guaranteed by design.

PIN DESCRIPTION

Pin TSOT23-6	Name	Description
1	NC	Not connected
2	GND	GND
3	NC	Not connected
4	IN	Input Voltage and GATE Fast Pull-Down Returns. The IN pin is the anode of the ideal diode and connect to the source of the N-channel MOSFET. The voltage sensed at this pin is used to control the source-drain voltage across the MOSFET.
5	GATE	Gate Drive Output. The GATE pin pull high enhancing the N-channel MOSFET when the load current creates more than 30mV.When the load current is small, the gate is actively driven to maintain 30mV. If the reverse current develops more than -25mV of the voltage drop across a MOSFET, a fast pull-down circuit quickly connects the GATE pin to IN pin.
6	OUT	Drain Voltage Sense and Positive Supply Input

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. ORing diodes have been a popular means of connecting these supplies at the point of load. The disadvantage of this approach is the forward voltage drop and resulting efficiency loss. This drop reduces the available supply voltage and dissipates significant power. Using N-channel MOSFETs to replace Schottky diodes reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layouts in high power applications.

The JW7260 is a positive voltage ORing controller that drives an external N-channel MOSFET as pass transistor to replace ORing diode. The IN and OUT pins form the anode and cathode of the ideal diode. The source pin of the external MOSFET is connected to the IN pin. The drain of the MOSFET is connected at the OUT pin, which is the positive supply of the device. The gate of the external MOSFET will be driven by the JW7260 to regulate the voltage drop across the pass transistor.

At power-up, the initial load current flows through the body diode of the MOSFET with the higher IN voltage. The associated GATE pin immediately ramps up and turns on the MOSFET. The amplifier tries to regulate the voltage drop across the source and drain connections to 30mV. If the load current causes more than 30mV of drop, the MOSFET gate is driven fully on and the voltage drop is equal to $R_{DS(ON)} \times I_{LOAD}$.

When the power supply voltages are nearly equal, this regulation technique ensures that the load current is smoothly shared between the MOSFETs without oscillation. The current flowing through each pass transistor depends on the $R_{DS(ON)}$ of each MOSFET and the output impedances of the supplies.

In the event of a supply failure, such as if the supply that is conducting most or all of the current is shorted to GND, reverse current flows temporarily through the MOSFET that is on. This current is sourced from any load capacitance and from the second supply through the body diode of the other MOSFET. The JW7260 quickly responds to this condition, turning off the MOSFET in about 500ns. This fast turn-off prevents the reverse current from ramping up to a damaging level.

APPLICATION IMFORMATION

MOSFET Selection

The JW7260 drives N-channel MOSFET to conduct the load current. The important features of the MOSFETs are on-resistance $R_{DS(ON)}$, the maximum drain-source voltage $V_{DSS,}$ and the threshold voltage.

The gate drive for the MOSFET is guaranteed to be greater than 4.0V when the supply voltage at VOUT is between 6V and 20V. When the supply voltage at VOUT is greater than 20V, the gate drive is guaranteed to be greater than 10V. The gate drive is limited to less than 15V. This allows the use of logic level threshold N-channel MOSFETs and standard N-channel MOSFETs above 20V. An external Zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 18V.

The maximum allowable drain-source voltage, BV_{DSS}, must be higher than the supply voltages. If an input is connected to GND, the full supply voltage will appear across the MOSFET.

System Power Supply Failure

The JW7260 automatically supplies load current from the system input supply with the higher voltage. If this supply shorts to ground, reverse current begins to flow through the pass transistor temporarily and the transistor begins to turn off. When this reverse current creates –25mV of voltage drop across the drain and source pins of the pass transistor, a fast pull-down circuit engages to drive the gate low faster.

The remaining system power supply delivers the load current through the body diode of its pass transistor until the channel turns on.

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/μs or higher.

High slew rates coupled with parasitic inductances in series with the input and output paths may cause potentially destructive transients to appear at the IN and OUT pins of the JW7260 during reverse recovery. A zero impedance short-circuit directly across an input that is supplying current is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the MOSFET finally commutates the reverse current the JW7260 IN pin experiences a negative voltage spike, while the OUT pin spikes in the positive direction

To prevent damage to the JW7260 under conditions of input short-circuit, protect the IN pins and OUT pin as shown in Figure 1. The IN pins are protected by clamping to the GND pin in the negative direction. To protect IN pin from negative voltage, a schottky diode is recommended to be connected from GND to IN. Protect the OUT pin with a clamp, such as with a TVS or TransZorb, or with a local bypass capacitor of at least 10μF or both.

Parasitic inductance between the load bypass or the second supply and the JW7260 allows a zero impedance input short to collapse the voltage at the OUT pin, which increases the total turn-off time (tOFF). For applications up to

30V, bypass the OUT pin with 39μF; above 30V use at least 100μF. One capacitor serves to guard against OUT collapse and also protect OUT from voltage spikes.

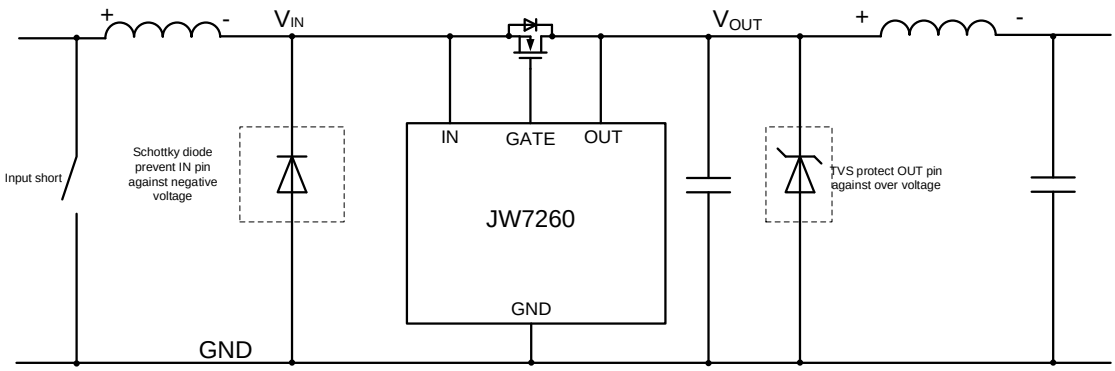


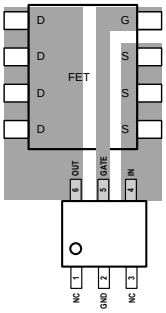
Figure1. Reverse Recovery Produces Inductive Spikes at the IN and OUT Pins. The Polarity of Step Recovery Spikes Is Shown Across Parasitic Inductances

PCB Layout Note

The following advice should be considered when laying out a printed circuit board for the JW7260.

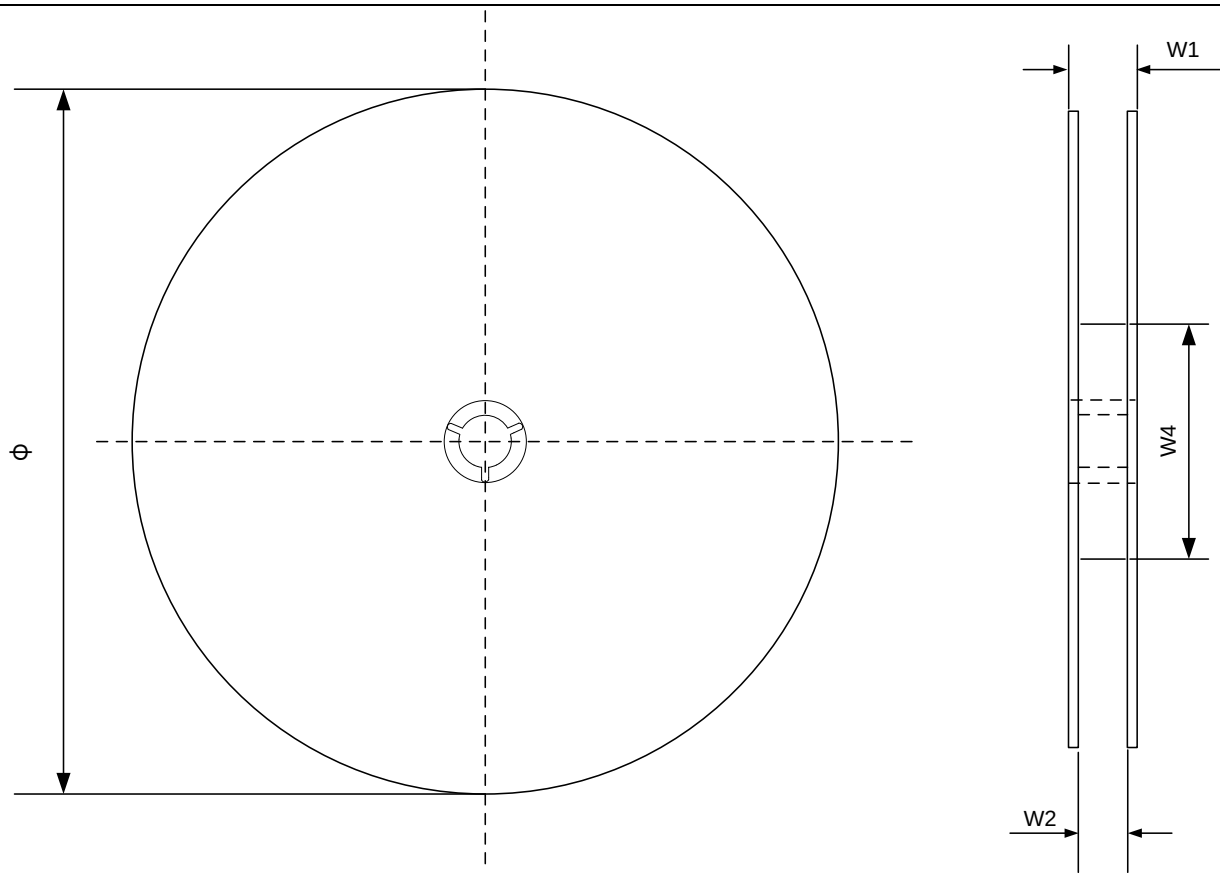
The inputs to the servo amplifiers, IN and OUT should be connected as closely as possible to the MOOSFET's terminals for good accuracy.

Keep the traces to the MOSFETs wide and short. The PCB traces associated with the power path through the MOSFETs should have low resistance



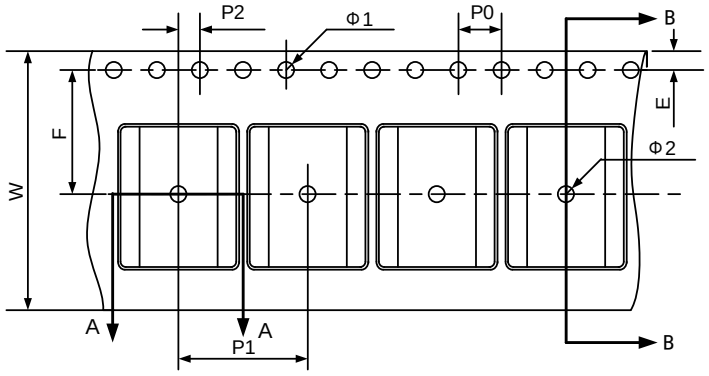
TAPE AND REEL INFORMATION

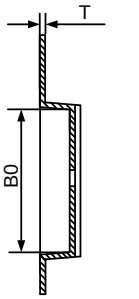
Reel UNIT: mm



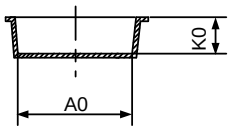
Package	Diameter Φ	Thickness W1	Width W2	W4
TSOT23-6	178±2	12.30±2	9.5±2	58±4

Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

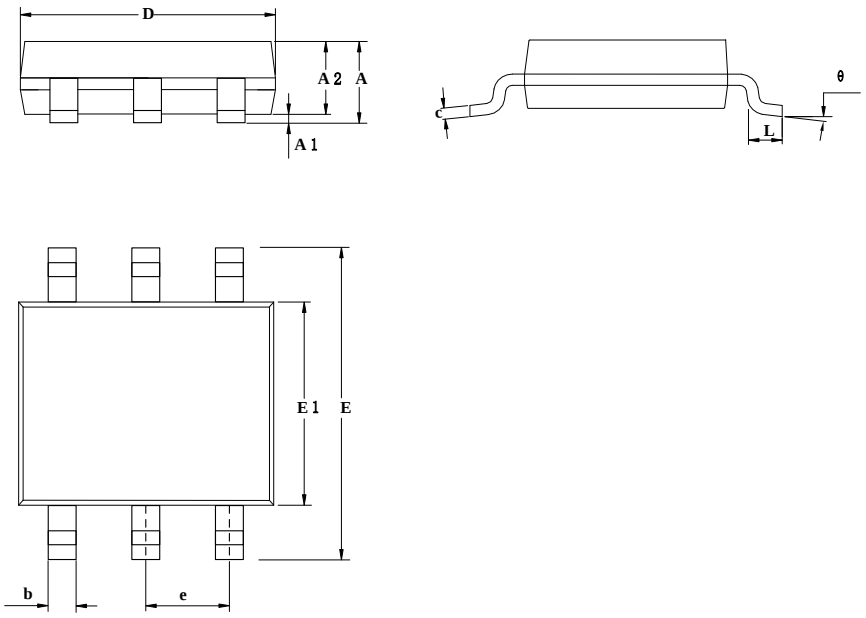
Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions(mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
TSOT23-6	4.0±0.1	2.0±0.1	4.0±0.1	3.17± 0.20	3.10± 0.2	8.0±0.3	0.25±0.2	1.10± 0.20	1.50min	1.00min	1.75± 0.1	3.50± 0.1

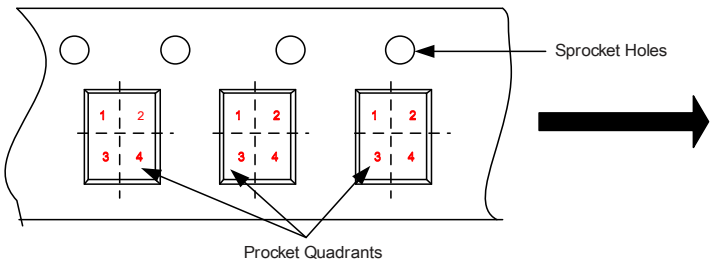
PACKAGE OUTLINE

TSOT23-6 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0	—	0.15
A2	0.55	—	1.00
b	0.30	0.40	0.50
c	0.08	0.15	0.30
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95（BSC）		
L	0.30	0.45	0.60
θ	0°	—	10°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
TSOT23-6	3

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