

## Description

The 9ZXL1550 is a DB1900Z derivative buffer utilizing Low-Power HCSL (LP-HCSL) outputs to increase edge rates on long traces, reduce board space, and reduce power consumption more than 50% from the original 9ZX21501. It is pin-compatible to the 9ZXL1530 and has the output terminations integrated. It is suitable for PCI-Express Gen1/2/3 or QPI/UPI applications, and uses a fixed external feedback to maintain low drift for demanding QPI/UPI applications.

## Recommended Application

Buffer for Romley, Grantley and Purley Servers

## Key Specifications

- Cycle-to-cycle jitter: < 50ps
- Output-to-output skew: <75ps
- Input-to-output delay variation: <50ps
- Phase jitter: PCIe Gen3 < 1ps rms
- Phase jitter: QPI 9.6GB/s < 0.2ps rms

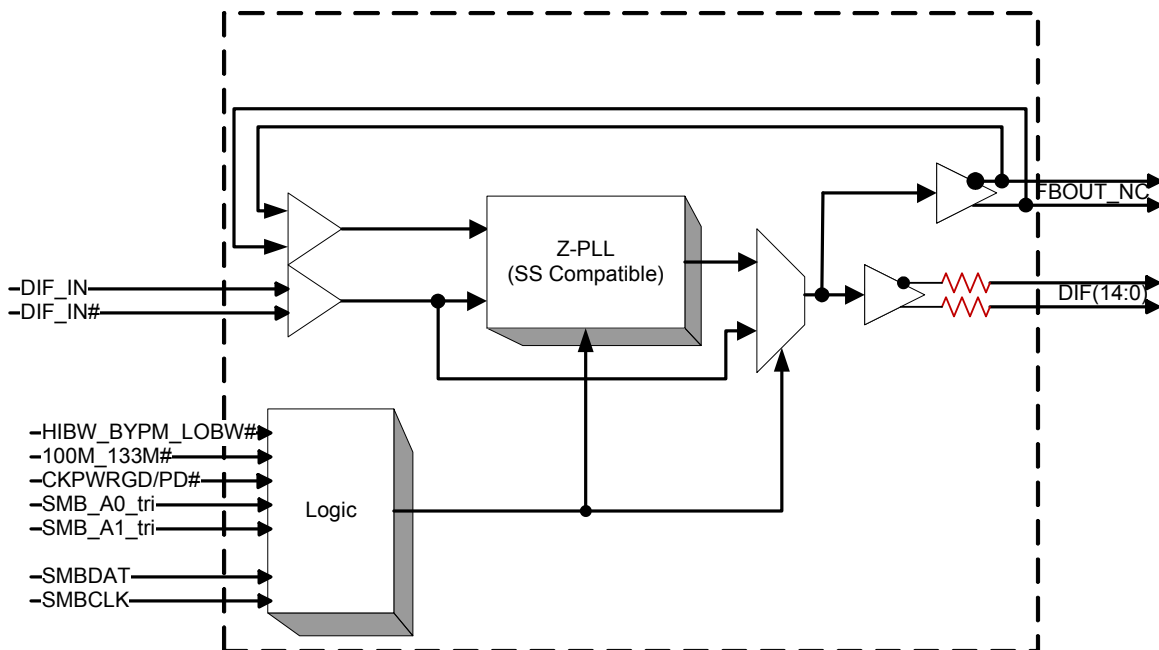
## Features/Benefits

- LP-HCSL outputs; up to 90% IO power reduction, better signal integrity over long traces
- Direct connect to 85Ω transmission lines; eliminates 60 termination resistors, saves 103mm<sup>2</sup> area
- Pin compatible to the 9ZXL1530; easy upgrade to reduced board space
- 64-VFQFPN package; smallest 15 output Z-buffer
- Fixed feedback path: ~ 0ps input-to-output delay
- 9 Selectable SMBus addresses; multiple devices can share same SMBus segment
- Separate VDDIO for outputs; allows maximum power savings
- PLL or bypass mode; PLL can dejitter incoming clock
- 100MHz & 133.33MHz PLL mode; legacy QPI/UPI support
- Selectable PLL BW; minimizes jitter peaking in downstream PLL's
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- SMBus Interface; unused outputs can be disabled

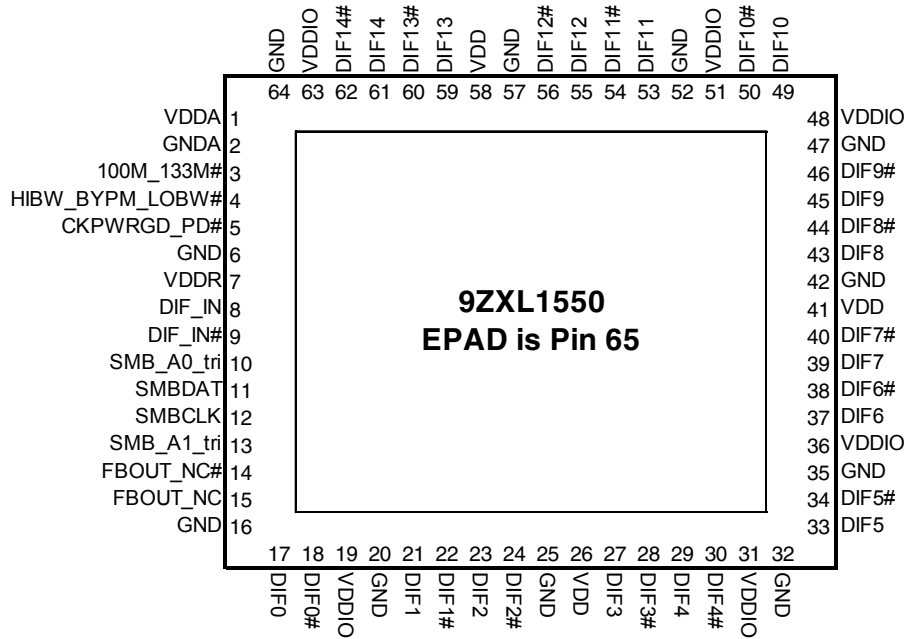
## Output Features

- 15 - LP-HCSL Differential Output Pairs w/integrated terminations ( $Z_o = 85\Omega$ )

## Block Diagram



## Pin Configuration



9x9 mm 64-pin VFQFPN

Note: Pins with ^ prefix have internal 120K pullup  
Pins with v prefix have internal 120K pulldown

## Power Management Table

| Inputs      |                    | Control Bits    | Outputs        |                        | PLL State |
|-------------|--------------------|-----------------|----------------|------------------------|-----------|
| CKPWRGD_PD# | DIF_IN/<br>DIF_IN# | SMBus<br>EN bit | DIFx/<br>DIFx# | FBOUT_NC/<br>FBOUT_NC# |           |
| 0           | X                  | X               | Low/Low        | Low/Low                | OFF       |
| 1           | Running            | 0               | Low/Low        | Running                | ON        |
|             |                    | 1               | Running        | Running                | ON        |

## Power Connections

| Pin Number |                   |                               | Description  |
|------------|-------------------|-------------------------------|--------------|
| VDD        | VDDIO             | GND                           |              |
| 1          |                   | 2                             | Analog PLL   |
| 7          |                   | 6                             | Analog Input |
| 26, 41, 58 | 19,31,36,48,51,63 | 16,20,25,32,35,42,47,52,57,64 | DIF clocks   |

## Functionality at Power-up (PLL mode)

| 100M_133M# | DIF_IN<br>(MHz) | DIFx<br>(MHz) |
|------------|-----------------|---------------|
| 1          | 100.00          | DIF_IN        |
| 0          | 133.33          | DIF_IN        |

## PLL Operating Mode

| HiBW BypM LoBW#    | Byte0, bit (7:6) |
|--------------------|------------------|
| Low ( PLL Low BW)  | 00               |
| Mid (Bypass)       | 01               |
| High (PLL High BW) | 11               |

NOTE: PLL is off in Bypass mode

## Tri-Level Input Thresholds

| Level | Voltage      |
|-------|--------------|
| Low   | <0.8V        |
| Mid   | 1.2<Vin<1.8V |
| High  | Vin > 2.2V   |

## Pin Descriptions

| PIN # | PIN NAME        | TYPE | DESCRIPTION   |
|-------|-----------------|------|---|
| 1     | VDDA            | PWR  | Power for the PLL core.   |
| 2     | GND             | GND  | Ground pin for the PLL core.  |
| 3     | 100M_133M#      | IN   | 3.3V Input to select operating frequency.<br>See Functionality Table for Definition   |
| 4     | HIBW_BYPM_LOBW# | IN   | Trilevel input to select High BW, Bypass or Low BW mode.<br>See PLL Operating Mode Table for Details.   |
| 5     | CKPWRGD_PD#     | IN   | 3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.                 |
| 6     | GND             | GND  | Ground pin.   |
| 7     | VDDR            | PWR  | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.  |
| 8     | DIF_IN          | IN   | HCSL True input   |
| 9     | DIF_IN#         | IN   | HCSL Complementary Input  |
| 10    | SMB_A0_tri      | IN   | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses.  |
| 11    | SMBDAT          | I/O  | Data pin of SMBUS circuitry, 5V tolerant  |
| 12    | SMBCLK          | IN   | Clock pin of SMBUS circuitry, 5V tolerant   |
| 13    | SMB_A1_tri      | IN   | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses.  |
| 14    | FBOUT_NC#       | OUT  | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 15    | FBOUT_NC        | OUT  | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.          |
| 16    | GND             | GND  | Ground pin.   |
| 17    | DIF0            | OUT  | Differential true clock output  |
| 18    | DIF0#           | OUT  | Differential Complementary clock output   |
| 19    | VDDIO           | PWR  | Power supply for differential outputs   |
| 20    | GND             | GND  | Ground pin.   |
| 21    | DIF1            | OUT  | Differential true clock output  |
| 22    | DIF1#           | OUT  | Differential Complementary clock output   |
| 23    | DIF2            | OUT  | Differential true clock output  |
| 24    | DIF2#           | OUT  | Differential Complementary clock output   |
| 25    | GND             | GND  | Ground pin.   |
| 26    | VDD             | PWR  | Power supply, nominal 3.3V  |
| 27    | DIF3            | OUT  | Differential true clock output  |
| 28    | DIF3#           | OUT  | Differential Complementary clock output   |
| 29    | DIF4            | OUT  | Differential true clock output  |
| 30    | DIF4#           | OUT  | Differential Complementary clock output   |
| 31    | VDDIO           | PWR  | Power supply for differential outputs   |
| 32    | GND             | GND  | Ground pin.   |

## Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION                             |
|-------|----------|------|---|
| 33    | DIF5     | OUT  | Differential true clock output          |
| 34    | DIF5#    | OUT  | Differential Complementary clock output |
| 35    | GND      | GND  | Ground pin.                             |
| 36    | VDDIO    | PWR  | Power supply for differential outputs   |
| 37    | DIF6     | OUT  | Differential true clock output          |
| 38    | DIF6#    | OUT  | Differential Complementary clock output |
| 39    | DIF7     | OUT  | Differential true clock output          |
| 40    | DIF7#    | OUT  | Differential Complementary clock output |
| 41    | VDD      | PWR  | Power supply, nominal 3.3V              |
| 42    | GND      | GND  | Ground pin.                             |
| 43    | DIF8     | OUT  | Differential true clock output          |
| 44    | DIF8#    | OUT  | Differential Complementary clock output |
| 45    | DIF9     | OUT  | Differential true clock output          |
| 46    | DIF9#    | OUT  | Differential Complementary clock output |
| 47    | GND      | GND  | Ground pin.                             |
| 48    | VDDIO    | PWR  | Power supply for differential outputs   |
| 49    | DIF10    | OUT  | Differential true clock output          |
| 50    | DIF10#   | OUT  | Differential Complementary clock output |
| 51    | VDDIO    | PWR  | Power supply for differential outputs   |
| 52    | GND      | GND  | Ground pin.                             |
| 53    | DIF11    | OUT  | Differential true clock output          |
| 54    | DIF11#   | OUT  | Differential Complementary clock output |
| 55    | DIF12    | OUT  | Differential true clock output          |
| 56    | DIF12#   | OUT  | Differential Complementary clock output |
| 57    | GND      | GND  | Ground pin.                             |
| 58    | VDD      | PWR  | Power supply, nominal 3.3V              |
| 59    | DIF13    | OUT  | Differential true clock output          |
| 60    | DIF13#   | OUT  | Differential Complementary clock output |
| 61    | DIF14    | OUT  | Differential true clock output          |
| 62    | DIF14#   | OUT  | Differential Complementary clock output |
| 63    | VDDIO    | PWR  | Power supply for differential outputs   |
| 64    | GND      | GND  | Ground pin.                             |
| 65    | EPAD     | GND  | Epad should be connected to GND         |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL1550. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER                 | SYMBOL             | CONDITIONS                 | MIN     | TYP | MAX                   | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage  | VDDA, R            |                            |         |     | 4.6                   | V     | 1,2   |
| 3.3V Logic Supply Voltage | VDD                |                            |         |     | 4.6                   | V     | 1,2   |
| I/O Supply Voltage        | VDDIO              |                            |         |     | 4.6                   | V     | 1,2   |
| Input Low Voltage         | V <sub>IL</sub>    |                            | GND-0.5 |     |                       | V     | 1     |
| Input High Voltage        | V <sub>IH</sub>    | Except for SMBus interface |         |     | V <sub>DD</sub> +0.5V | V     | 1     |
| Input High Voltage        | V <sub>IHSMB</sub> | SMBus clock and data pins  |         |     | 5.5V                  | V     | 1     |
| Storage Temperature       | T <sub>s</sub>     |                            | -65     |     | 150                   | °C    | 1     |
| Junction Temperature      | T <sub>j</sub>     |                            |         |     | 125                   | °C    | 1     |
| Input ESD protection      | ESD prot           | Human Body Model           | 2000    |     |                       | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

## Electrical Characteristics–DIF\_IN Clock Input Parameters

T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER                        | SYMBOL             | CONDITIONS  | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | V <sub>CROSS</sub> | Cross Over Voltage  | 150 |     | 900 | mV    | 1     |
| Input Swing - DIF_IN             | V <sub>SWING</sub> | Differential value  | 300 |     |     | mV    | 1     |
| Input Slew Rate - DIF_IN         | dv/dt              | Measured differentially                                   | 0.4 |     | 8   | V/ns  | 1,2   |
| Input Leakage Current            | I <sub>IN</sub>    | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND | -5  |     | 5   | uA    |       |
| Input Duty Cycle                 | d <sub>tin</sub>   | Measurement from differential waveform                    | 45  |     | 55  | %     | 1     |
| Input Jitter - Cycle to Cycle    | J <sub>DIFIN</sub> | Differential Measurement                                  | 0   |     | 125 | ps    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through +/-75mV window centered around differential zero

## Electrical Characteristics–Input/Supply/Common Parameters

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER                     | SYMBOL                | CONDITIONS  | MIN       | TYP    | MAX                   | UNITS | NOTES |
|-------------------------------|-----------------------|---|-----------|--------|-----------------------|-------|-------|
| Ambient Operating Temperature | T <sub>COM</sub>      | Commercial range  | 0         | 35     | 70                    | °C    |       |
| Input High Voltage            | V <sub>IH</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | 2         |        | V <sub>DD</sub> + 0.3 | V     |       |
| Input Low Voltage             | V <sub>IL</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | GND - 0.3 |        | 0.8                   | V     |       |
| Input Current                 | I <sub>IN</sub>       | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD   | -5        |        | 5                     | uA    |       |
|                               | I <sub>INP</sub>      | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -200      |        | 200                   | uA    |       |
| Input Frequency               | F <sub>ibyp</sub>     | V <sub>DD</sub> = 3.3 V, Bypass mode  | 33        |        | 150                   | MHz   | 2     |
|                               | F <sub>ipll</sub>     | V <sub>DD</sub> = 3.3 V, 100MHz PLL mode  | 90        | 100.00 | 110                   | MHz   | 2     |
|                               | F <sub>ipll</sub>     | V <sub>DD</sub> = 3.3 V, 133.33MHz PLL mode   | 120       | 133.33 | 147                   | MHz   | 2     |
| Pin Inductance                | L <sub>pin</sub>      |   |           |        | 7                     | nH    | 1     |
| Capacitance                   | C <sub>IN</sub>       | Logic Inputs, except DIF_IN   | 1.5       |        | 5                     | pF    | 1     |
|                               | C <sub>INDIF_IN</sub> | DIF_IN differential clock inputs  | 1.5       |        | 2.7                   | pF    | 1,4   |
|                               | C <sub>OUT</sub>      | Output pin capacitance  |           |        | 6                     | pF    | 1     |
| Clk Stabilization             | T <sub>STAB</sub>     | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock   |           | 0.65   | 1                     | ms    | 2     |
| Input SS Modulation Frequency | f <sub>MODIN</sub>    | Allowable Frequency (Triangular Modulation)   | 30        | 31.5   | 33                    | kHz   |       |
| Tdrive_PD#                    | t <sub>DRVPD</sub>    | DIF output enable after PD# de-assertion  |           | 25     | 300                   | us    | 1,3   |
| Tfall                         | t <sub>F</sub>        | Fall time of control inputs   |           |        | 5                     | ns    | 1,2   |
| Trise                         | t <sub>R</sub>        | Rise time of control inputs   |           |        | 5                     | ns    | 1,2   |
| SMBus Input Low Voltage       | V <sub>ILSMB</sub>    |   |           |        | 0.8                   | V     |       |
| SMBus Input High Voltage      | V <sub>IHSMB</sub>    |   | 2.1       |        | V <sub>DD</sub> SMB   | V     |       |
| SMBus Output Low Voltage      | V <sub>OLSMB</sub>    | @ I <sub>PULLUP</sub>   |           |        | 0.4                   | V     |       |
| SMBus Sink Current            | I <sub>PULLUP</sub>   | @ V <sub>OL</sub>   | 4         |        |                       | mA    |       |
| Nominal Bus Voltage           | V <sub>DD</sub> SMB   | 3V to 5V +/- 10%  | 2.7       |        | 5.5                   | V     |       |
| SCLK/SDATA Rise Time          | t <sub>RSMB</sub>     | (Max VIL - 0.15) to (Min VIH + 0.15)  |           |        | 1000                  | ns    | 1     |
| SCLK/SDATA Fall Time          | t <sub>FSMB</sub>     | (Min VIH + 0.15) to (Max VIL - 0.15)  |           |        | 300                   | ns    | 1     |
| SMBus Operating Frequency     | f <sub>MIN</sub> SMB  | Maximum SMBus operating frequency   | 100       |        |                       | kHz   | 5     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

## Electrical Characteristics–DIF LP-HCSL Differential Outputs

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER              | SYMBOL     | CONDITIONS  | MIN  | TYP | MAX  | UNITS | NOTES   |
|------------------------|------------|---|------|-----|------|-------|---------|
| Slew rate              | Trf        | Scope averaging on  | 1.5  | 2.7 | 4    | V/ns  | 1, 2, 3 |
| Slew rate matching     | ΔTrf       | Slew rate matching.   |      | 8.8 | 20   | %     | 1, 2, 4 |
| Voltage High           | VHigh      | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660  | 787 | 850  | mV    |         |
| Voltage Low            | VLow       |   | -150 | 33  | 150  |       |         |
| Max Voltage            | Vmax       | Single ended signal using absolute value. Includes 300mV of over/undershoot. (Scope                   |      | 845 | 1150 | mV    |         |
| Min Voltage            | Vmin       |   | -300 | 9   |      |       |         |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off   | 250  | 471 | 550  | mV    | 1, 5    |
| Crossing Voltage (var) | Δ-Vcross   | Scope averaging off   |      | 14  | 140  | mV    | 1, 6    |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production. C<sub>L</sub> = 2pF with R<sub>S</sub> = 27Ω for Zo = 85Ω differential trace impedance.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup> Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross\_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

## Electrical Characteristics–Current Consumption

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER                | SYMBOL                  | CONDITIONS   | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-------------------------|--|-----|-----|-----|-------|-------|
| Operating Supply Current | I <sub>DDVDD</sub>      | All outputs 100MHz, C <sub>L</sub> = 2pF; Zo = 85Ω |     | 17  | 30  | mA    | 1     |
|                          | I <sub>DDVDDA/R</sub>   | All outputs 100MHz, C <sub>L</sub> = 2pF; Zo = 85Ω |     | 15  | 20  | mA    | 1     |
|                          | I <sub>DDVDDIO</sub>    | All outputs 100MHz, C <sub>L</sub> = 2pF; Zo = 85Ω |     | 112 | 150 | mA    | 1     |
| Powerdown Current        | I <sub>DDVDDPD</sub>    | All differential pairs low-low                     |     | 2.1 | 4   | mA    | 1     |
|                          | I <sub>DDVDDA/RPD</sub> | All differential pairs low-low                     |     | 4.4 | 7   | mA    | 1     |
|                          | I <sub>DDVDDIOPD</sub>  | All differential pairs low-low                     |     | 0.0 | 1.5 | mA    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics—Skew and Differential Jitter Parameters

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER              | SYMBOL                 | CONDITIONS   | MIN  | TYP  | MAX | UNITS    | NOTES     |
|------------------------|------------------------|--|------|------|-----|----------|-----------|
| CLK_IN, DIF[x:0]       | t <sub>SPO_PLL</sub>   | Input-to-Output Skew in PLL mode nominal value @ 35°C, 3.3V, 100MHz                      | -150 | -117 | -50 | ps       | 1,2,4,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>PD_BYP</sub>    | Input-to-Output Skew in Bypass mode nominal value @ 35°C, 3.3V                           | 2.5  | 4    | 4.5 | ns       | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DSPO_PLL</sub>  | Input-to-Output Skew Variation in PLL mode across voltage and temperature                | -50  | 0    | 50  | ps       | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DSPO_BYP</sub>  | Input-to-Output Skew Variation in Bypass mode across temperature for a given voltage     | -250 | 0    | 250 | ps       | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DTE</sub>       | Random Differential Tracking error between two 9ZX devices in Hi BW Mode                 |      | 1    | 5   | ps (rms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DSSTE</sub>     | Random Differential Spread Spectrum Tracking error between two 9ZX devices in Hi BW Mode |      | 5    | 75  | ps       | 1,2,3,5,8 |
| DIF[x:0]               | t <sub>SKEW_ALL</sub>  | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode). 100MHz         |      | 53   | 75  | ps       | 1,2,3,8   |
| PLL Jitter Peaking     | j <sub>peak-hibw</sub> | LOBW#_BYPASS_HIBW = 1  | 0    | 1.8  | 2.5 | dB       | 7,8       |
| PLL Jitter Peaking     | j <sub>peak-lobw</sub> | LOBW#_BYPASS_HIBW = 0  | 0    | 0.7  | 2   | dB       | 7,8       |
| PLL Bandwidth          | pll <sub>HIBW</sub>    | LOBW#_BYPASS_HIBW = 1  | 2    | 3.3  | 4   | MHz      | 8,9       |
| PLL Bandwidth          | pll <sub>LOBW</sub>    | LOBW#_BYPASS_HIBW = 0  | 0.7  | 1.2  | 1.4 | MHz      | 8,9       |
| Duty Cycle             | t <sub>DC</sub>        | Measured differentially, PLL Mode  | 45   | 50   | 55  | %        | 1         |
| Duty Cycle Distortion  | t <sub>DCD</sub>       | Measured differentially, Bypass Mode @100MHz   | 0    | 1    | 2   | %        | 1,10      |
| Jitter, Cycle to cycle | t <sub>jyc-cyc</sub>   | PLL mode   |      | 12   | 50  | ps       | 1,11      |
|                        |                        | Additive Jitter in Bypass Mode   |      | 0    | 50  | ps       | 1,11      |

### Notes for preceding table:

- <sup>1</sup> Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
- <sup>2</sup> Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
- <sup>3</sup> All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
- <sup>4</sup> This parameter is deterministic for a given device
- <sup>5</sup> Measured with scope averaging on to find mean value.
- <sup>6</sup> t is the period of the input clock
- <sup>7</sup> Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- <sup>8</sup> Guaranteed by design and characterization, not 100% tested in production.
- <sup>9</sup> Measured at 3 db down or half power point.
- <sup>10</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
- <sup>11</sup> Measured from differential waveform



## Electrical Characteristics–Phase Jitter Parameters

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER                             | SYMBOL                  | CONDITIONS   | MIN | TYP | MAX      | UNITS    | Notes   |
|---------------------------------------|-------------------------|--|-----|-----|----------|----------|---------|
| Phase Jitter, PLL Mode                | t <sub>jphPCleG1</sub>  | PCle Gen 1   |     | 34  | 86       | ps (p-p) | 1,2,3   |
|                                       | t <sub>jphPCleG2</sub>  | PCle Gen 2 Lo Band<br>10kHz < f < 1.5MHz               |     | 1.2 | 3        | ps (rms) | 1,2     |
|                                       |                         | PCle Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)   |     | 2.1 | 3.1      | ps (rms) | 1,2     |
|                                       | t <sub>jphPCleG3</sub>  | PCle Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)          |     | 0.5 | 1        | ps (rms) | 1,2,4   |
|                                       | t <sub>jphQPI_SMI</sub> | QPI & SMI<br>(100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) |     | 0.2 | 0.5      | ps (rms) | 1,5     |
|                                       |                         | QPI & SMI<br>(100MHz, 8.0Gb/s, 12UI)                   |     | 0.1 | 0.3      | ps (rms) | 1,5     |
| QPI & SMI<br>(100MHz, 9.6Gb/s, 12UI)  |                         |  | 0.1 | 0.2 | ps (rms) | 1,5      |         |
| Additive Phase Jitter,<br>Bypass mode | t <sub>jphPCleG1</sub>  | PCle Gen 1   |     | 0.1 | 10       | ps (p-p) | 1,2,3   |
|                                       | t <sub>jphPCleG2</sub>  | PCle Gen 2 Lo Band<br>10kHz < f < 1.5MHz               |     | 0.1 | 0.3      | ps (rms) | 1,2,6   |
|                                       |                         | PCle Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)   |     | 0.1 | 0.7      | ps (rms) | 1,2,6   |
|                                       | t <sub>jphPCleG3</sub>  | PCle Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)          |     | 0.0 | 0.3      | ps (rms) | 1,2,4,6 |
|                                       | t <sub>jphQPI_SMI</sub> | QPI & SMI<br>(100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) |     | 0.0 | 0.3      | ps (rms) | 1,5,6   |
|                                       |                         | QPI & SMI<br>(100MHz, 8.0Gb/s, 12UI)                   |     | 0.0 | 0.1      | ps (rms) | 1,5,6   |
| QPI & SMI<br>(100MHz, 9.6Gb/s, 12UI)  |                         |  | 0.0 | 0.1 | ps (rms) | 1,5,6    |         |

<sup>1</sup> Applies to all outputs.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> Subject to final ratification by PCI SIG.

<sup>5</sup> Calculated from Intel-supplied Clock Jitter Tool v 1.6.4

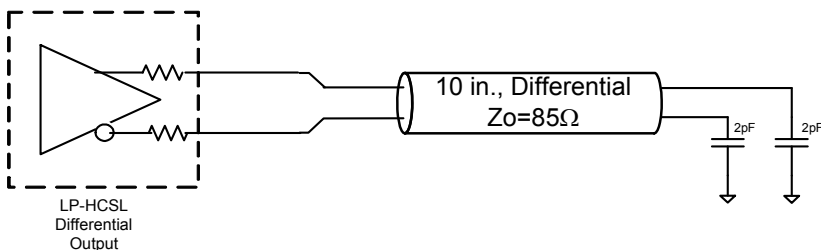
<sup>6</sup> For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)<sup>2</sup> = (total jitter)<sup>2</sup> - (input jitter)<sup>2</sup>

## Test Loads

### Differential Output Terminations

| DIF Zo (Ω) | Rs (Ω)          |
|------------|-----------------|
| 85         | Internal        |
| 100        | 7<br>(External) |

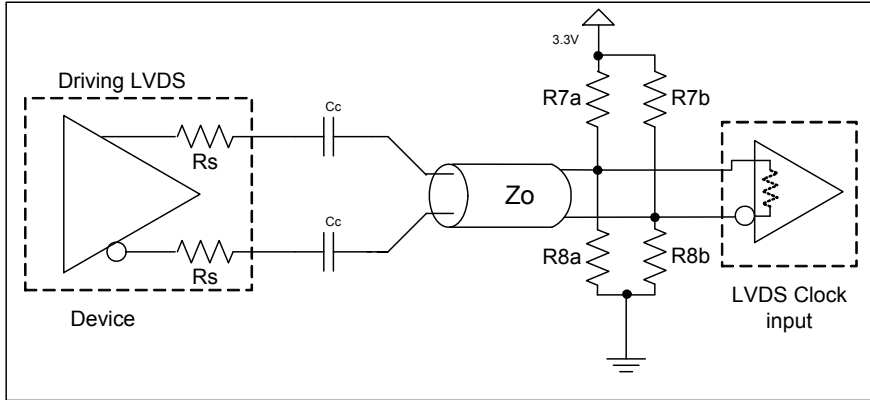
9ZXL1550 Differential Test Loads



## Driving LVDS

### Driving LVDS inputs

| Component | Value                    |                                    | Note |
|-----------|--------------------------|------------------------------------|------|
|           | Receiver has termination | Receiver does not have termination |      |
| R7a, R7b  | 10K ohm                  | 140 ohm                            |      |
| R8a, R8b  | 5.6K ohm                 | 75 ohm                             |      |
| Cc        | 0.1 uF                   | 0.1 uF                             |      |
| Vcm       | 1.2 volts                | 1.2 volts                          |      |



## Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                        | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
|         |                  | 1 Clock                | 1us                         | 0.1s                        | 0.1s                 | 0.1s                        | 1us                         | 1 Clock                |       |       |
|         |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max |       |       |
| DIF     | 100.00           | 9.94900                |                             | 9.99900                     | 10.00000             | 10.00100                    |                             | 10.05100               | ns    | 1,2,3 |
|         | 133.33           | 7.44925                |                             | 7.49925                     | 7.50000              | 7.50075                     |                             | 7.55075                | ns    | 1,2,4 |

## Clock Periods–Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                        | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
|        |                  | 1 Clock                | 1us                         | 0.1s                        | 0.1s                 | 0.1s                        | 1us                         | 1 Clock                |       |       |
|        |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max |       |       |
| DIF    | 99.75            | 9.94906                | 9.99906                     | 10.02406                    | 10.02506             | 10.02607                    | 10.05107                    | 10.10107               | ns    | 1,2,3 |
|        | 133.00           | 7.44930                | 7.49930                     | 7.51805                     | 7.51880              | 7.51955                     | 7.53830                     | 7.58830                | ns    | 1,2,4 |

### Notes:

- <sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.
- <sup>2</sup> All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL1550 itself does not contribute to ppm error.
- <sup>3</sup> Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode
- <sup>4</sup> Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

## General SMBus Serial Interface Information

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation |           |                      |
|-----------------------------|-----------|----------------------|
| Controller (Host)           |           | IDT (Slave/Receiver) |
| T                           | starT bit |                      |
| Slave Address               |           |                      |
| WR                          | WRite     |                      |
| Beginning Byte = N          |           | ACK                  |
|                             |           | ACK                  |
| Data Byte Count = X         |           | ACK                  |
| Beginning Byte N            |           | ACK                  |
|                             | X Byte    | ○                    |
| ○                           |           | ○                    |
| ○                           |           | ○                    |
| Byte N + X - 1              |           | ACK                  |
| P                           | stoP bit  |                      |

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | IDT (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address              |                 |                      |
| WR                         | WRite           |                      |
| Beginning Byte = N         |                 | ACK                  |
|                            |                 | ACK                  |
| RT                         | Repeat starT    |                      |
| Slave Address              |                 |                      |
| RD                         | ReaD            |                      |
|                            |                 | ACK                  |
| ACK                        |                 | Data Byte Count=X    |
| ACK                        |                 | Beginning Byte N     |
|                            | X Byte          | ○                    |
| ○                          |                 | ○                    |
| ○                          |                 | ○                    |
| ○                          |                 | ○                    |
|                            |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

**9ZXL1550 SMBus Addressing**

| SMB_A(1:0)_tri | Address (Rd/Wrt bit = 0) (Hex) |
|----------------|--------------------------------|
| 00             | D8                             |
| 0M             | DA                             |
| 01             | DE                             |
| M0             | C2                             |
| MM             | C4                             |
| M1             | C6                             |
| 10             | CA                             |
| 1M             | CC                             |
| 11             | CE                             |

**SMBusTable: PLL Mode, and Frequency Select Register**

| Byte 0 | Pin # | Name       | Control Function             | Type | 0                                     | 1      | Default |
|--------|-------|------------|------------------------------|------|---------------------------------------|--------|---------|
| Bit 7  | 4     | PLL Mode 1 | PLL Operating Mode Rd back 1 | R    | See PLL Operating Mode Readback Table |        | Latch   |
| Bit 6  | 4     | PLL Mode 0 | PLL Operating Mode Rd back 0 | R    |                                       |        | Latch   |
| Bit 5  |       | Reserved   |                              |      |                                       |        | 1       |
| Bit 4  | 61/62 | DIF_14_En  | Output Enable                | RW   | Low/Low                               | Enable | 1       |
| Bit 3  | 59/60 | DIF_13_En  | Output Enable                | RW   | Low/Low                               | Enable | 1       |
| Bit 2  |       | Reserved   |                              |      |                                       |        | 0       |
| Bit 1  |       | Reserved   |                              |      |                                       |        | 0       |
| Bit 0  | 3     | 100M_133M# | Frequency Select Readback    | R    | 133MHz                                | 100MHz | Latch   |

**SMBusTable: Output Control Register**

| Byte 1 | Pin # | Name     | Control Function | Type | 0       | 1      | Default |
|--------|-------|----------|------------------|------|---------|--------|---------|
| Bit 7  | 39/40 | DIF_5_En | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 6  |       | Reserved |                  |      |         |        | 1       |
| Bit 5  | 29/30 | DIF_4_En | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 4  | 29/30 | DIF_3_En | Output Enable    | RW   |         |        | 1       |
| Bit 3  | 23/24 | DIF_2_En | Output Enable    | RW   |         |        | 1       |
| Bit 2  | 21/22 | DIF_1_En | Output Enable    | RW   |         |        | 1       |
| Bit 1  | 17/18 | DIF_0_En | Output Enable    | RW   |         |        | 1       |
| Bit 0  |       | Reserved |                  |      |         |        | 1       |

**SMBusTable: Output Control Register**

| Byte 2 | Pin # | Name      | Control Function | Type | 0       | 1      | Default |
|--------|-------|-----------|------------------|------|---------|--------|---------|
| Bit 7  | 55/56 | DIF_12_En | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 6  | 53/54 | DIF_11_En | Output Enable    | RW   |         |        | 1       |
| Bit 5  | 49/50 | DIF_10_En | Output Enable    | RW   |         |        | 1       |
| Bit 4  |       | Reserved  |                  |      |         |        | 1       |
| Bit 3  | 45/46 | DIF_9_En  | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 2  | 43/44 | DIF_8_En  | Output Enable    | RW   |         |        | 1       |
| Bit 1  | 39/40 | DIF_7_En  | Output Enable    | RW   |         |        | 1       |
| Bit 0  | 37/38 | DIF_6_En  | Output Enable    | RW   |         |        | 1       |

**SMBusTable: Reserved Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

**SMBusTable: Reserved Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

**SMBusTable: Vendor & Revision ID Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0            | 1 | Default |
|--------|-------|------|------------------|------|--------------|---|---------|
| Bit 7  | -     | RID3 | REVISION ID      | R    | B Rev = 0000 |   | 0       |
| Bit 6  | -     | RID2 |                  | R    |              |   | 0       |
| Bit 5  | -     | RID1 |                  | R    |              |   | 0       |
| Bit 4  | -     | RID0 |                  | R    |              |   | 1       |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | -            | - | 0       |
| Bit 2  | -     | VID2 |                  | R    | -            | - | 0       |
| Bit 1  | -     | VID1 |                  | R    | -            | - | 0       |
| Bit 0  | -     | VID0 |                  | R    | -            | - | 1       |

**SMBusTable: DEVICE ID**

| Byte 6 | Pin # | Name | Control Function  | Type | 0                             | 1 | Default |
|--------|-------|------|-------------------|------|-------------------------------|---|---------|
| Bit 7  | -     |      | Device ID 7 (MSB) | R    | 1550 is 155 decimal or 9B Hex |   | 1       |
| Bit 6  | -     |      | Device ID 6       | R    |                               |   | 0       |
| Bit 5  | -     |      | Device ID 5       | R    |                               |   | 0       |
| Bit 4  | -     |      | Device ID 4       | R    |                               |   | 1       |
| Bit 3  | -     |      | Device ID 3       | R    |                               |   | 1       |
| Bit 2  | -     |      | Device ID 2       | R    |                               |   | 0       |
| Bit 1  | -     |      | Device ID 1       | R    |                               |   | 1       |
| Bit 0  | -     |      | Device ID 0       | R    |                               |   | 1       |

**SMBusTable: Byte Count Register**

| Byte 7 | Pin # | Name | Control Function  | Type | 0   | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7  |       |      | Reserved  |      |   |   | 0       |
| Bit 6  |       |      | Reserved  |      |   |   | 0       |
| Bit 5  |       |      | Reserved  |      |   |   | 0       |
| Bit 4  | -     | BC4  | Writing to this register configures how many bytes will be read back. | RW   | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. |   | 0       |
| Bit 3  | -     | BC3  |   | RW   |   |   | 1       |
| Bit 2  | -     | BC2  |   | RW   |   |   | 0       |
| Bit 1  | -     | BC1  |   | RW   |   |   | 0       |
| Bit 0  | -     | BC0  |   | RW   |   |   | 0       |

**SMBusTable: Reserved Register**

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

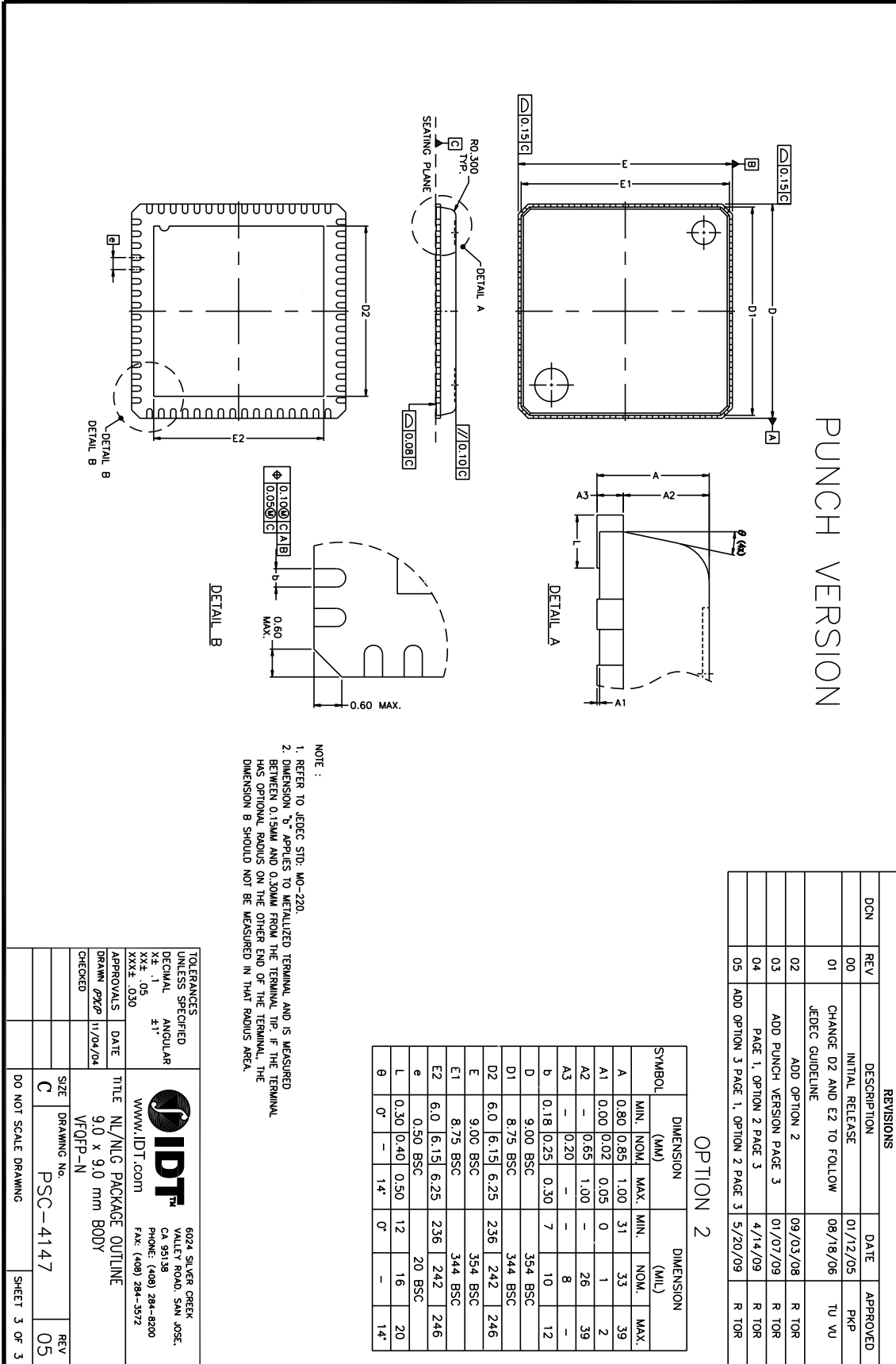
## Marking Diagram



Notes:

1. "L" denotes RoHS compliant package.
2. "LOT" denotes the lot number.
2. "COO" denotes country of origin.
3. "YYWW" is the last two digits of the year and week that the part was assembled.

Package Outline and Package Dimensions (NLG64)



| REVISIONS |     |  |          |
|-----------|-----|--|----------|
| DCN       | REV | DESCRIPTION                                | DATE     |
|           | 00  | INITIAL RELEASE                            | 01/12/05 |
|           | 01  | CHANGE D2 AND E2 TO FOLLOW JEDEC GUIDELINE | 08/18/06 |
|           | 02  | ADD OPTION 2                               | 09/03/08 |
|           | 03  | ADD PUNCH VERSION PAGE 3                   | 01/07/09 |
|           | 04  | PAGE 1, OPTION 2 PAGE 3                    | 4/14/09  |
|           | 05  | ADD OPTION 3 PAGE 1, OPTION 2 PAGE 3       | 5/20/09  |

**TOLERANCES UNLESS SPECIFIED**

DECIMAL ±0.10

ANGULAR ±1°

XXX±.030

DATE 11/20/15

DRAWN PXP

CHECKED

APPROVALS

SIZE C

DRAWING No. PSC-4147

DO NOT SCALE DRAWING

REV 05

SHEET 3 OF 3

**IDT**

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6024 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138

PHONE: (408) 284-8200

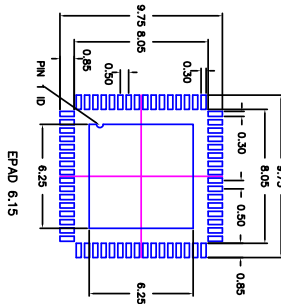
FAX: (408) 284-3572

TITLE NL/NLG PACKAGE OUTLINE

9.0 x 9.0 mm BODY

VFOFP-N

Package Outline and Package Dimensions (NLG64), cont.



- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
  2. TOP DOWN VIEW. AS VIEWED ON PCB.
  3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  4. LAND PATTERN RECOMMENDATION PER IPC-7351B LP CALCULATOR.

| REVISIONS |  |          |          |
|-----------|--|----------|----------|
| REV       | DESCRIPTION  | DATE     | APPROVED |
| 00        | INITIAL RELEASE  | 01/12/05 | PKP      |
| 01        | CHANGE D2 AND E2 TO FOLLOW JEDEC GUIDELINE                         | 08/18/06 | TU VU    |
| 02        | ADD OPTION 2   | 09/03/08 | R. TOR   |
| 03        | ADD PUNCH VERSION PAGE 3   | 01/07/09 | R. TOR   |
| 04        | PAGE 1, OPTION 2 PAGE 3  | 4/14/09  | R. TOR   |
| 05        | ADD OPTION3 PAGE 1, OPTION 2 PAGE 3                                | 5/20/09  | R. TOR   |
| 06        | COOR DIM L OPTION 4 EPAD MORE DIMENSION OPTION 2, ADD LAND PATTERN | 7/11/13  | KS       |
| 07        | ADD OPTION 5 IN PAGE 2   | 05/20/14 | CK LEE   |

|                             |             |                                 |  |
|-----------------------------|-------------|---------------------------------|--|
| TOLERANCES UNLESS SPECIFIED |             | 6024 SILVER CREEK               |  |
| DECIMAL                     | ANGULAR     | VALLEY ROAD, SAN JOSE, CA 95138 |  |
| XX. .1                      | ±1°         | PHONE: (408) 284-8200           |  |
| XXX. .05                    |             | FAX: (408) 284-3572             |  |
| XXXX. .030                  |             | www.IDT.com                     |  |
| APPROVALS                   | DATE        | TITLE                           |  |
| DRAWN: <i>gwp</i>           | 11/04/04    | NL/NLG PACKAGE OUTLINE          |  |
| CHECKED                     |             | VFQFP-N                         |  |
| SIZE                        | DRAWING No. | REV                             |  |
| C                           | PSC-4147    | 07                              |  |
| DO NOT SCALE DRAWING        |             | SHEET 4 OF 4                    |  |



## Ordering Information

| Part / Order Number | Shipping Package | Package       | Temperature |
|---------------------|------------------|---------------|-------------|
| 9ZXL1550BKLF        | Trays            | 64-pin VFQFPN | 0 to +70°C  |
| 9ZXL1550BKLFT       | Tape and Reel    | 64-pin VFQFPN | 0 to +70°C  |

“LF” suffix denotes Pb-Free configuration, RoHS compliant.

“B” is the device revision designator (will not correlate with the datasheet revision).

## Revision History

| Rev. | Issuer | Issue Date | Description  | Page #  |
|------|--------|------------|--|---------|
| A    | RDW    | 2/27/2015  | <ol style="list-style-type: none"> <li>1. Cleaned up output pin names to be DIFxx instead of DIF_xx</li> <li>2. Updated electrical tables with characterized data</li> <li>3. Updated ordering info to B rev along with Rev ID.</li> <li>4. Updated termination schemes for driving LVDS.</li> <li>5. Minor cleanup and move to final</li> </ol> | Various |
| B    | RDW    | 3/6/2015   | <ol style="list-style-type: none"> <li>1. Updated Data sheet Title, General Description and Recommended Application text.</li> <li>2. Corrected tSPO_PLL parameter in Skew and Differential Jitter Parameters table.</li> </ol>  | 1,8     |
| C    | RDW    | 3/16/2015  | 1.Changed max IDDVDDIOPD limit from 0.5mA to 1.5mA.  | 7       |
| D    | RDW    | 6/16/2015  | Added landing pattern from POD drawing.  | 16      |
| E    | RDW    | 11/20/2015 | <ol style="list-style-type: none"> <li>1. Updated QPI references to QPI/UPI</li> <li>2. Updated DIF_IN table to match PCI SIG specification, no silicon change</li> </ol>  | 1,5     |



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