FAIRCHILD SEMICONDUCTOR®

February 2008

FMS6346
Six Channel, 6th-Order SD/HD Video Filter Driver

Features

- Three selectable sixth-order 8/32MHz (SD/HD) filters
- Three fixed sixth-order 8MHz (SD) filters
- Transparent input clamping
- Single video load drive ($2V_{pp}$, 150Ω, A_V = 6dB)
- AC- or DC-coupled inputs
- AC- or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- Low power
- 5V only
- Robust (12kV HBM) output ESD protection
- Lead-free package - TSSOP-20

Applications

- Cable and satellite set-top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6346 Low Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Six sixth-order Butterworth filters provide improved image quality compared to typical passive solutions. The combination of low-power Standard-Definition (SD) and High-Definition (HD) filters greatly simplify DVD video output circuitry. Three channels offer fixed SD filters, while the other three are selectable between SD and HD filters.

The FMS6346 offers a fixed gain of 6dB. The FMS6346 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (*see Applications section for details*).

The outputs can drive AC- or DC-coupled single (150Ω) video loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output.

Ordering Information

Part Number	Gain Option	Temperature	Package	Container	Quantity
FMS6346MTC20	6dB	0°C to 70°C	TSSOP-20	Rail	94
FMS6346MTC20X	6dB	0°C to 70°C	TSSOP-20	Reel	2500

All packages are lead free per JEDEC: J-STD-020B standard.

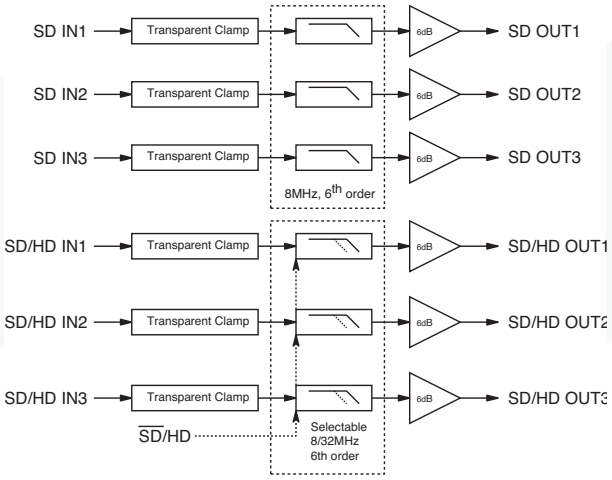


Figure 1. Block Diagram

Pin Configuration

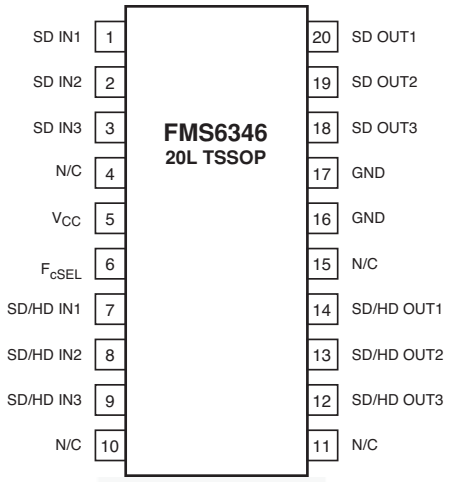


Figure 2. Pin Configuration

Pin Assignments

Pin#	Pin	Type	Description
1	SD IN1	Input	SD video input, channel 1
2	SD IN2	Input	SD video input, channel 2
3	SD IN3	Input	SD video input, channel 3
4	N/C	Input	No Connection
5	VCC	Input	+5V supply
6	FcSEL	Input	Selects filter corner frequency for pins 7, 8, and 9: “0” = SD, “1” = PS
7	SD/HD IN1	Input	Selectable SD or PS video input, channel 1
8	SD/HD IN2	Input	Selectable SD or PS video input, channel 2
9	SD/HD IN3	Input	Selectable SD or PS video input, channel 3
10	N/C	Input	No Connection
11	N/C	Input	No Connection
12	SD/HD	Out-	Filtered SD or PS video output, channel 3
13	SD/HD	Out-	Filtered SD or PS video output, channel 2
14	SD/HD	Out-	Filtered SD or PS video output, channel 1
15	N/C	Input	No Connection
16	GND	Input	Must be tied to ground
17	GND	Input	Must be tied to ground
18	SD OUT3	Out-	Filtered SD video output, channel 3
19	SD OUT2	Out-	Filtered SD video output, channel 2
20	SD OUT1	Out-	Filtered SD video output, channel 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
I_{OUT}	Output Current, Any One Channel (Do Not Exceed)		50	mA

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature Range	-65		150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			300	°C
θ_{JA}	Thermal Resistance, JEDEC Standard Multi-Layer Test Boards, Still Air		74		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	0		70	°C
V_{CC}	Supply Voltage Range	4.75	5.00	5.25	V

DC Electrical Characteristics

T_A = 25°C, V_{cc} = 5V, R_{source} = 37.5Ω, inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current(1)	No Load		60	80	mA
V_{IN}	Video Input Voltage Range	Referenced to GND, if DC-coupled		1.4		V_{pp}
V_{IL}	Digital Input Low(1)	f_{cSEL}	0		0.8	V
V_{IH}	Digital Input High(1)	f_{cSEL}	2.4		V_{CC}	V

Standard-Definition Electrical Characteristics

T_A = 25°C, V_{in} = 1V_{pp}, V_{cc} = 5V, R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{SD}	Channel Gain(1)	All SD Channels	5.8	6.0	6.2	dB
f_{1dBSD}	-1dB Bandwidth(1)	All SD Channels	5.50	7.15		MHz
f_{cSD}	-3dB Bandwidth(1)	All SD Channels	6.5	8.0		MHz
f_{SBSD}	Attenuation (Stopband Reject)(1)	All SD Channels at f = 27MHz	43	50		dB
DG	Differential Gain	All SD Channels		0.7		%
DP	Differential Phase	All SD Channels		1.0		°
THD	Output Distortion	V_{OUT} = 1.4V_{pp}, 3.58MHz		0.35		%
X_{TALKSD}	Crosstalk (ch-to-ch)	at 1MHz		-54		dB
SNR	Signal-to-Noise Ratio(2)	NTC-7 weighting, 100kHz to 4.2MHz		72		dB
t_{pdSD}	Propagation Delay	Delay from input to output, 4.5MHz		90		ns

High-Definition Electrical Characteristics

T_A = 25°C, V_{IN} = 1V_{pp}, V_{cc} = 5V, R_{source} = 37.5Ω, F_{cSEL} = 1, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{HD}	Channel Gain(1)	All HD Channels	5.8	6.0	6.2	dB
f_{1dBSHD}	-1dB Bandwidth(1)	All HD Channels	28	31		MHz
f_{cHD}	-3dB Bandwidth(1)	All HD Channels	30	34		MHz
f_{SBHD}	Attenuation (Stopband Reject)(1)	All HD Channels at f = 74.25MHz	30	41		dB
THD	Output Distortion (All HD Channels)	V_{OUT} = 1.4V_{pp}, 22MHz		0.9		%
X_{TALKHD}	Crosstalk (ch-to-ch)	at 1MHz		-54		dB
SNR	Signal-to-Noise Ratio(2)	Unweighted; 100kHz to 30MHz		60		dB
t_{pdHD}	Propagation Delay	Delay from input to output		25		ns

Notes:

1. 100% tested at 25°C.
2. SNR = 20 * log (714mV/rms noise).

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 1V_{pp}, V_{CC} = 5V, R_{source} = 37.5Ω, inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads; unless otherwise noted.

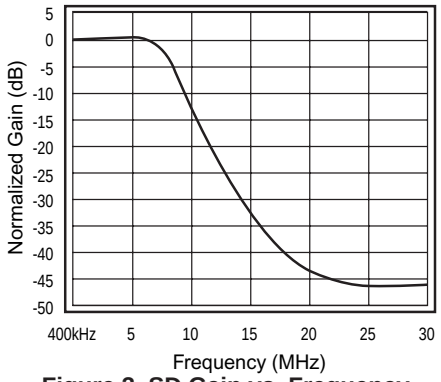


Figure 3. SD Gain vs. Frequency

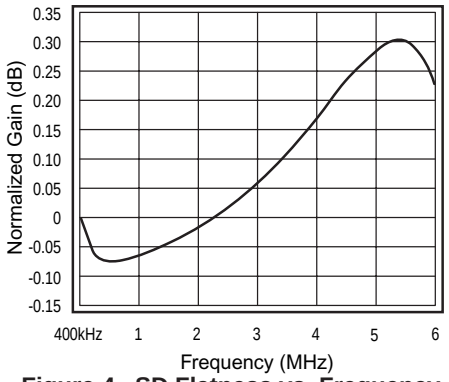


Figure 4. SD Flatness vs. Frequency

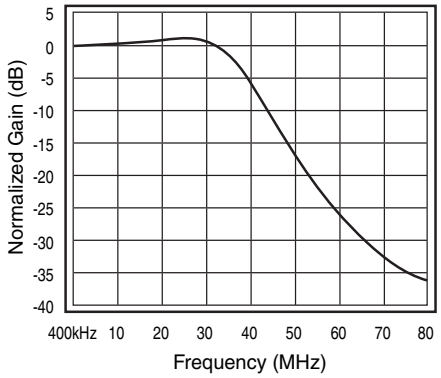


Figure 5. HD Gain vs. Frequency

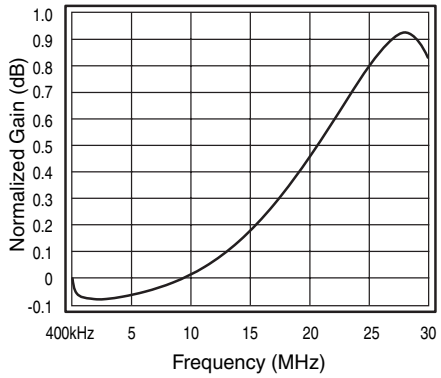


Figure 6. HD Flatness vs. Frequency

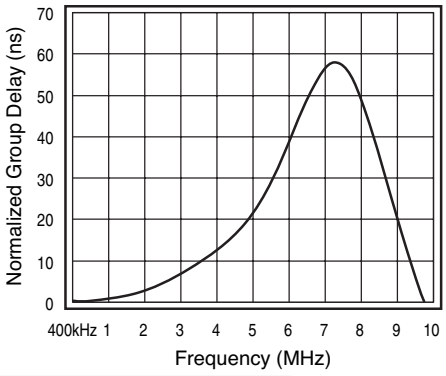


Figure 7. SD Group Delay vs. Frequency

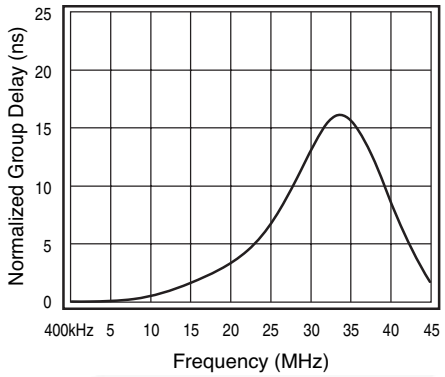


Figure 8. HD Group Delay vs. Frequency

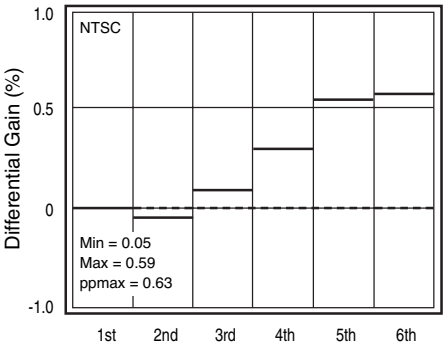


Figure 9. SD Differential Gain

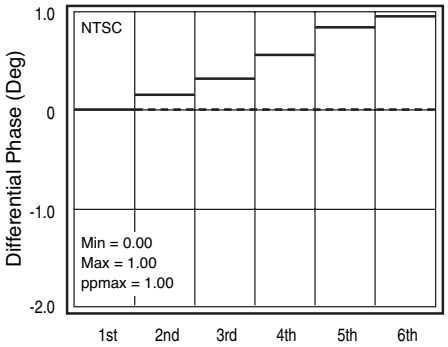


Figure 10. HD Differential Phase

Applications Information

Functional Description

The FMS6346 Low-Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 11.

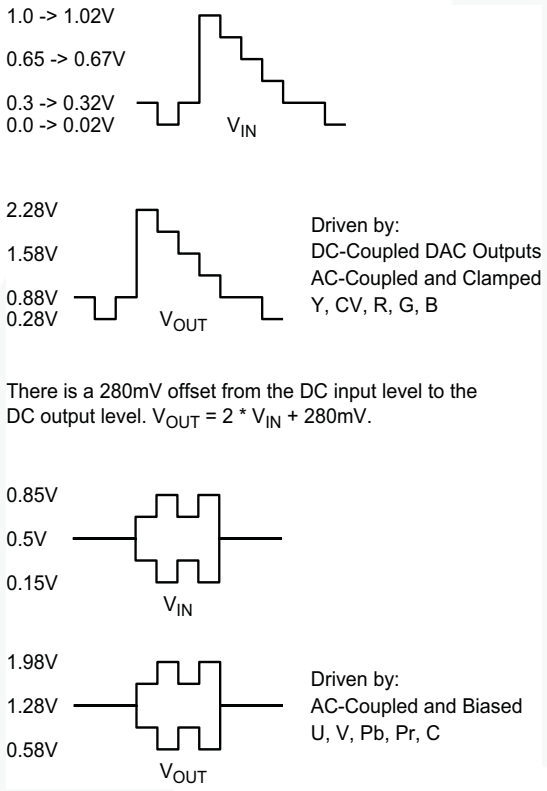


Figure 11. Typical Voltage Levels

The FMS6346 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6346 without an AC coupling capacitor. The worst-case sync tip compression due to the clamp does not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range. When the input is AC-coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground.

For symmetric signals like C, U, V, Cb, Cr, Pb, and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 12.

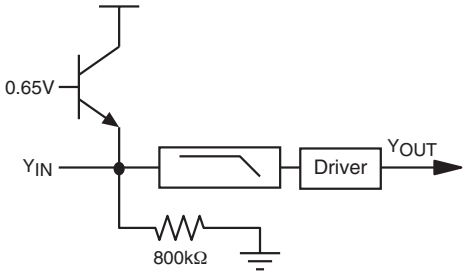


Figure 12. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use the configuration shown in Figure 13.

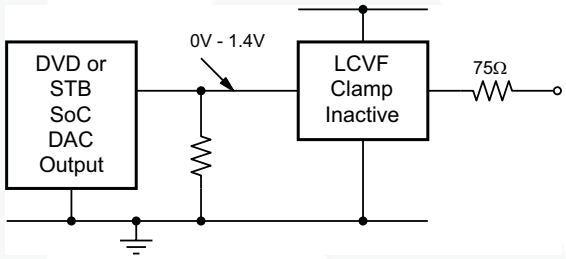


Figure 13. DC-Coupled Inputs and Outputs

If the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled as shown in Figure 14.

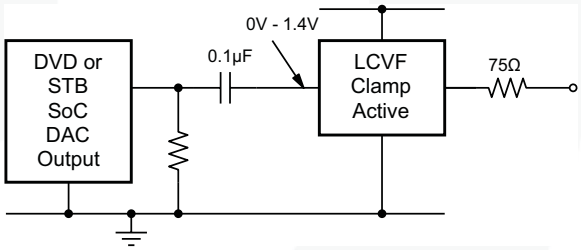


Figure 14. AC-Coupled Inputs, DC-Coupled Outputs

When the is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC-coupled as shown in Figure 15.

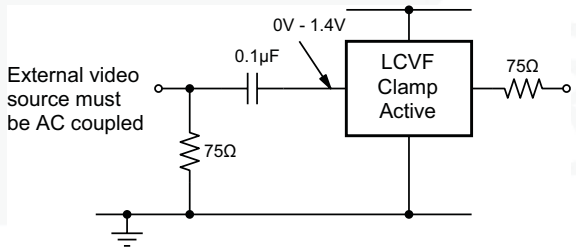


Figure 15. SCART Configuration with DC-Coupled Outputs

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20%, so the external resistance should be 7.5MΩ to set the DC level to 500mV. If a pull-up resistance less than 7.5MΩ is desired, an external pull-down can be added such that the DC input level is set to 500mV.

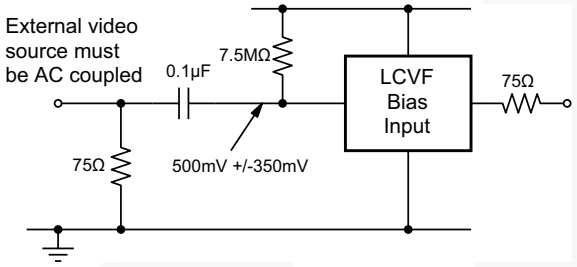


Figure 16. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired, as shown in Figure 17.

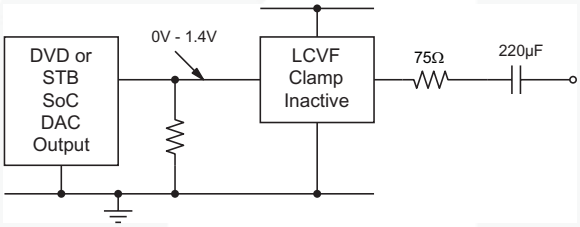


Figure 17 DC-Coupled Inputs, AC-Coupled Outputs

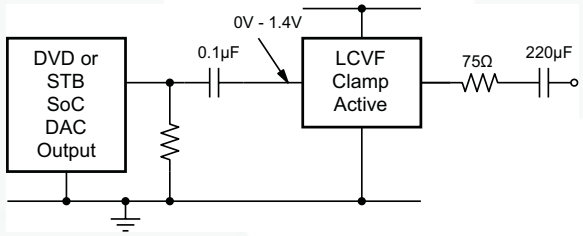


Figure 18. AC-Coupled Inputs, AC-Coupled Outputs

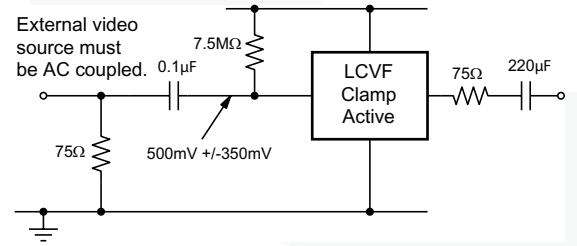


Figure 19. Biased SCART with AC-Coupled Outputs

NOTE: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6346 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6346's power dissipation and internal temperature rise:

$T_J = T_A + P_d \bullet \theta_{JA}$

where $P_d = P_{CH1} + P_{CH2} + P_{CHx}$

and $P_{CHx} = V_s \bullet I_{CH} - (V_O^2/R_L)$

where

$V_O = 2V_{in} + 0.280V$

$I_{CH} = (I_{CC} / 6) + (V_O/R_L)$

V_{IN} = RMS value of input signal

I_{CC} = 60mA

V_s = 5V

R_L = channel load resistance

Board layout can affect thermal characteristics. Refer to the *Layout Considerations* section for more information.

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6346DEMO, to guide layout and aid device testing and characterization. The FMS6346DEMO is a four-layer board with a full power and ground plane. Following this layout configuration provides the optimum performance and thermal characteristics. For best results, follow the steps below as a basis for high-frequency layout:

- Include 10µF and 0.1µF ceramic bypass capacitors
- Place the 10µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat
- For two-layer boards, use a ground plane that extends beyond the device by at least 0.5 inches
- Minimize all trace lengths to reduce series inductances

Typical Application Diagram

The following circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to 1.4V. AC-coupled or DC-coupled outputs may be used with AC-coupled outputs offering slightly lower power dissipation.

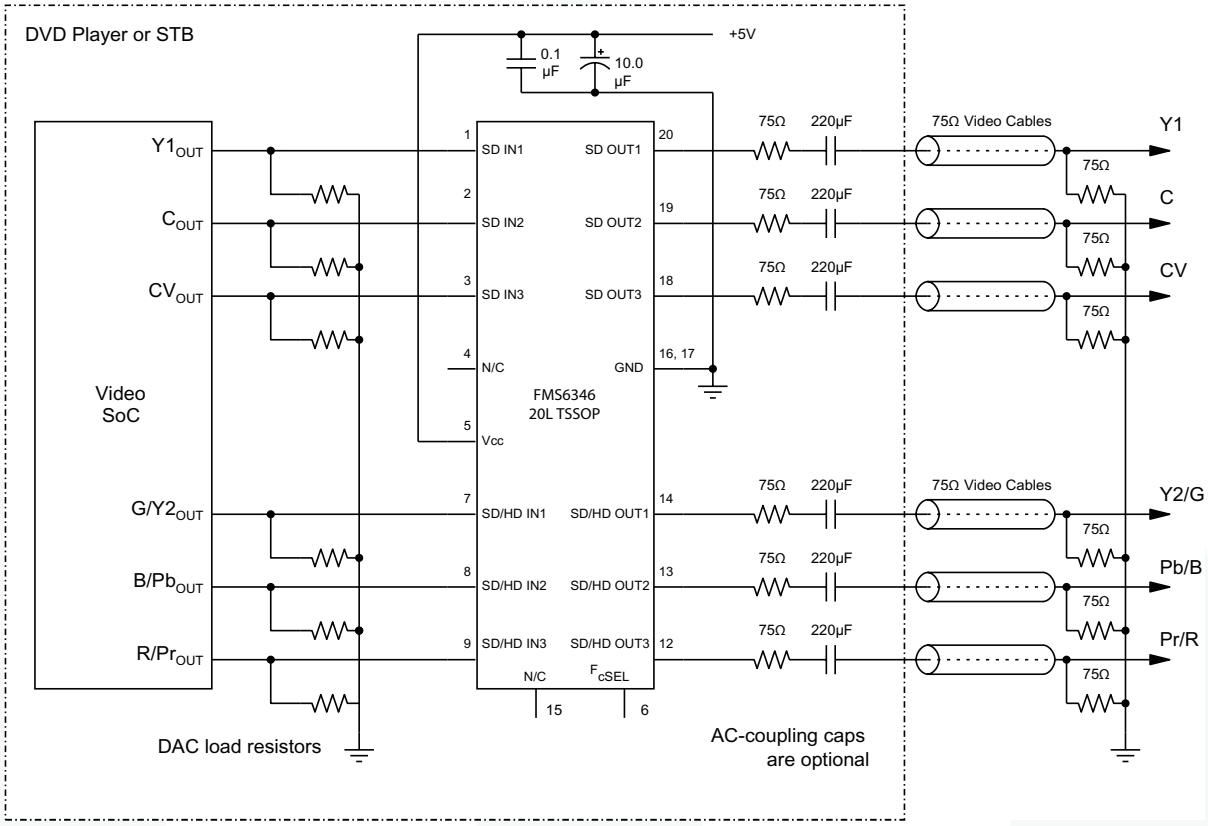
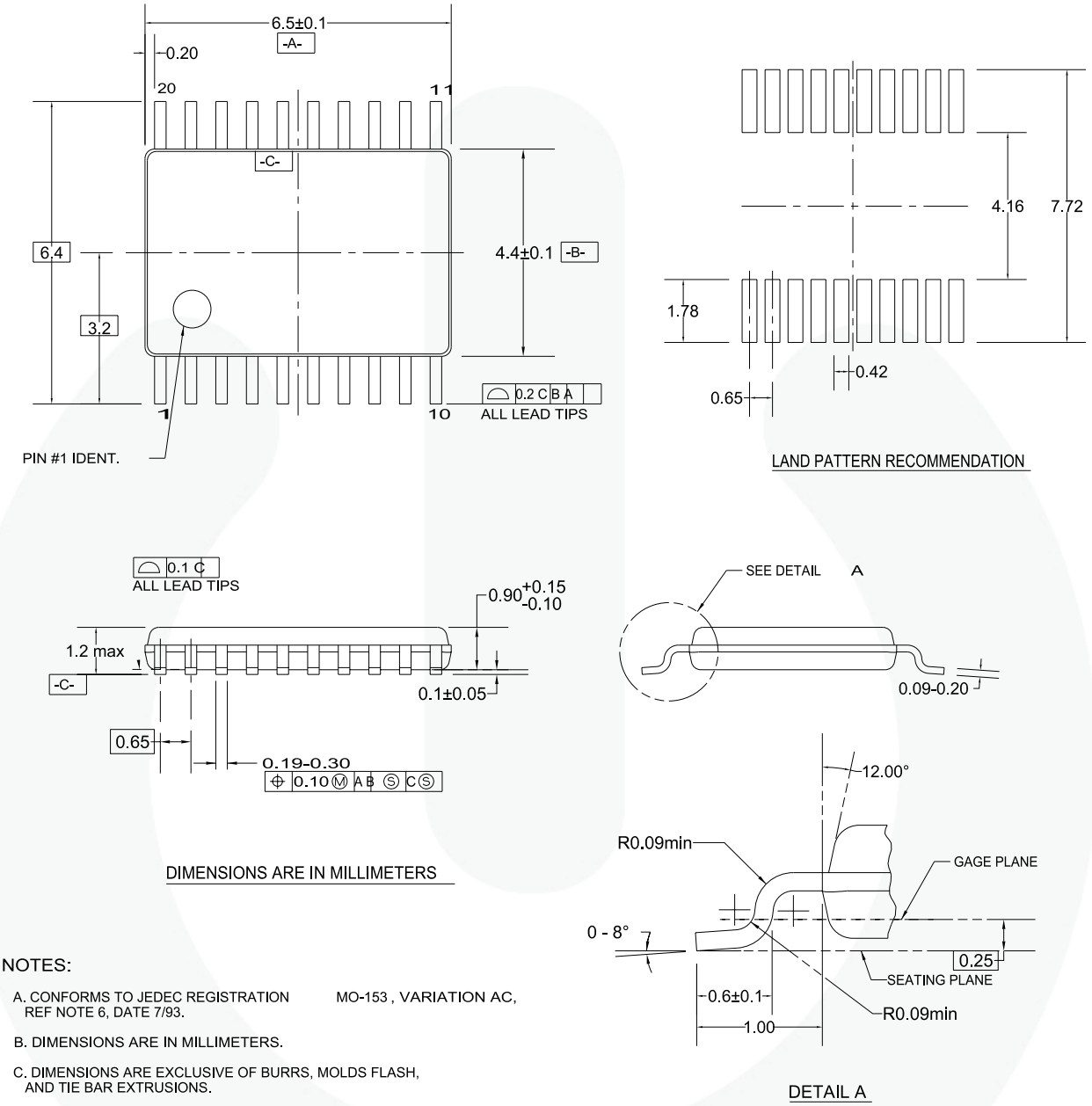


Figure 20. Typical Application Diagram

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153 , VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 21. 20-Lead, Thin-Shrink Outline Package (TSSOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EZSWITCH™ *
™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter®*
FPS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power220®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33