

MC74HCT138A

1-of-8 Decoder/ Demultiplexer with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT138A is identical in pinout to the LS138. The HCT138A may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The HCT138A decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

Features

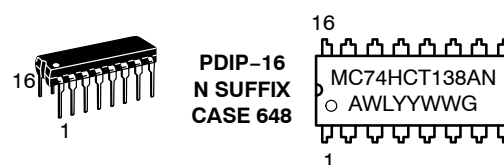
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates
- Pb-Free Packages are Available*



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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

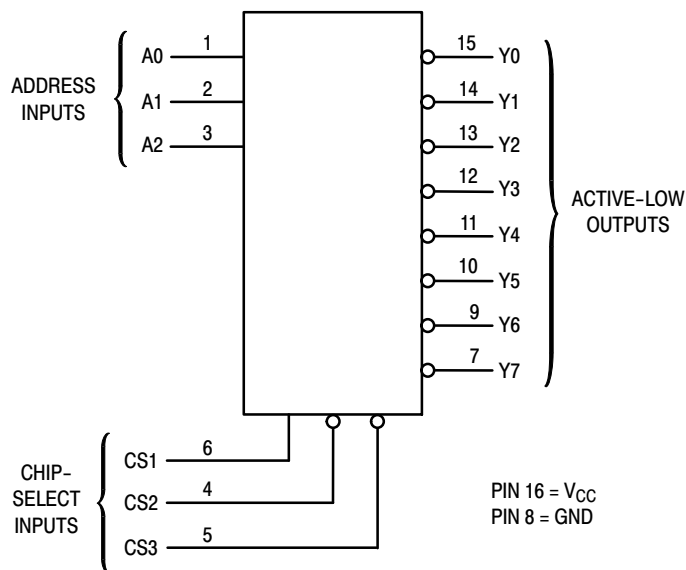
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

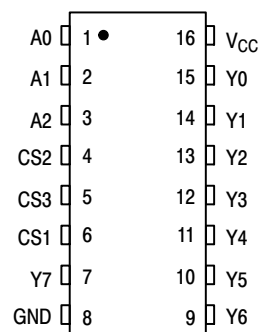
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	L

H = high level (steady state)

L = low level (steady state)

X = don't care

Design Criteria	Value	Units
Internal Gate Count*	30.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two-input NAND gate.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HCT138ANG	PDIP-16 (Pb-Free)	500 Units / Box
MC74HCT138ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HCT138ADR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC74HCT138ADTR2	TSSOP-16*	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V	
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V	
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V	
I_{in}	DC Input Current, per Pin	± 20	mA	
I_{out}	DC Output Current, per Pin	± 25	mA	
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA	
P_D	Power Dissipation in Still Air	Plastic DIP†	750	mW
		SOIC Package†	500	
		TSSOP Package†	450	
T_{stg}	Storage Temperature	- 65 to + 150	$^{\circ}C$	
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package)	260	$^{\circ}C$	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: - 10 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$
 SOIC Package: - 7 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$
 TSSOP Package: - 6.1 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				- 55 to 25 $^{\circ}C$	$\leq 85^{\circ}C$	$\leq 125^{\circ}C$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 V$ or $V_{CC} - 0.1 V$ $ I_{out} \leq 20 \mu A$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 V$ or $V_{CC} - 0.1 V$ $ I_{out} \leq 20 \mu A$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 mA$	4.5	3.98	3.84	3.7	V
			5.5	0.1	0.1	0.1	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 mA$	4.5	0.26	0.33	0.4	V
			5.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	5.5	4.0	40	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 V$, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	$\geq - 55^{\circ}C$	25 $^{\circ}C$ to 125 $^{\circ}C$		mA
				2.9	2.4		

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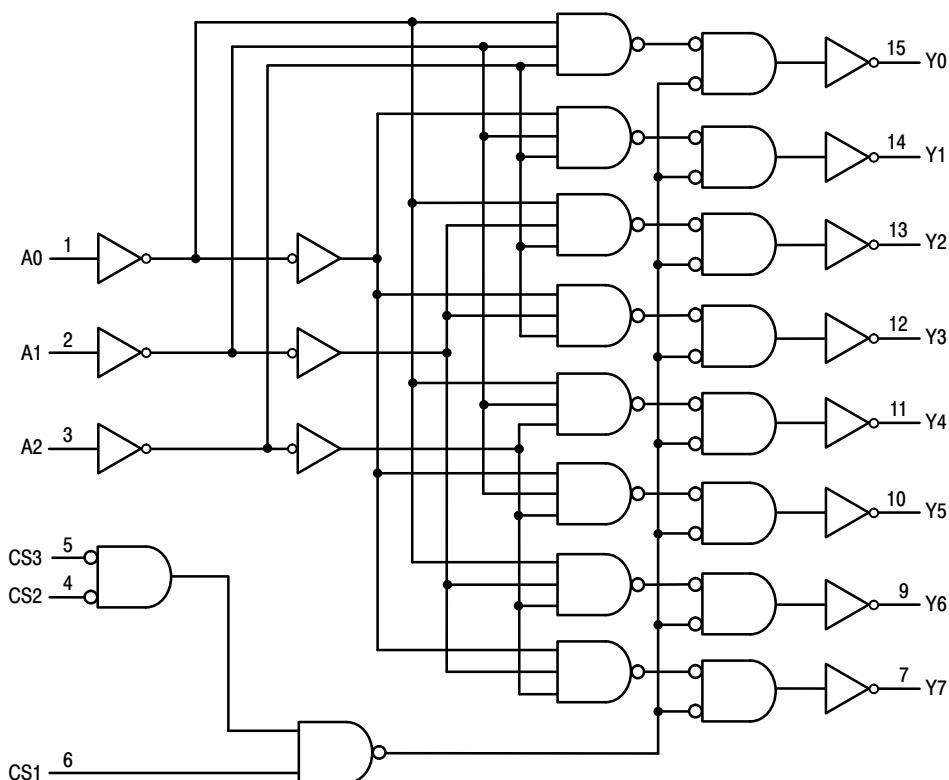
AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		- 55 to 25° C	≤ 85° C	≤ 125° C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	30	38	45	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	27	34	41	ns
t_{PLH} , t_{PHL}	Maximum Output Transition Time, CS2 or CS3 to Output Y (Figures 3 and 4)	30	38	45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	15	19	22	ns
t_r , t_f	Maximum Input Rise and Fall Time	500	500	500	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25° C, $V_{CC} = 5.0 \text{ V}$		pF
		51		

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

EXPANDED LOGIC DIAGRAM



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SWITCHING WAVEFORMS

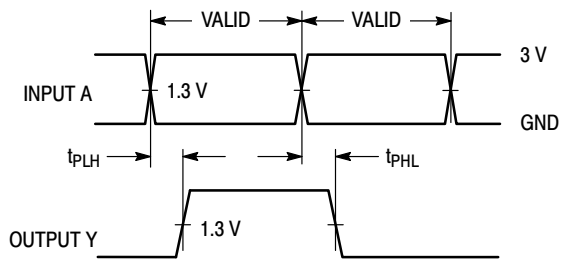


Figure 1.

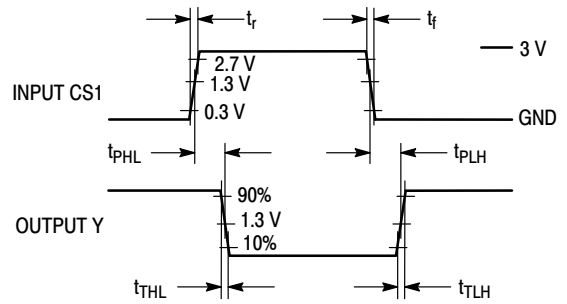


Figure 2.

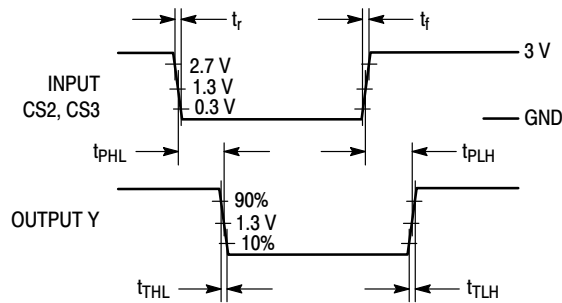
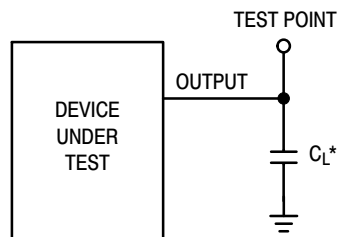


Figure 3.

TEST CIRCUIT



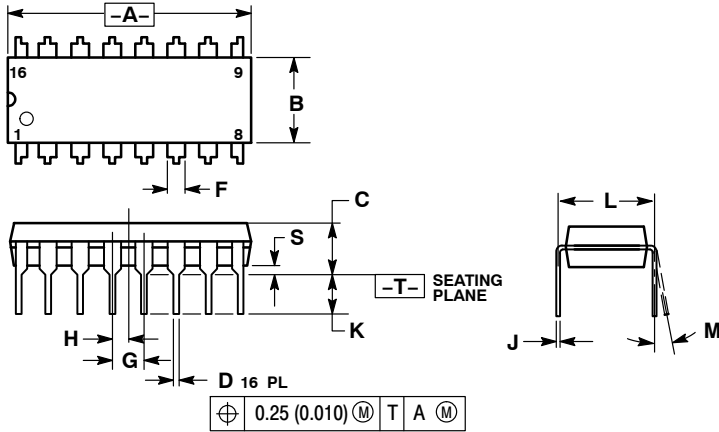
*Includes all probe and jig capacitance

Figure 4.

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PACKAGE DIMENSIONS

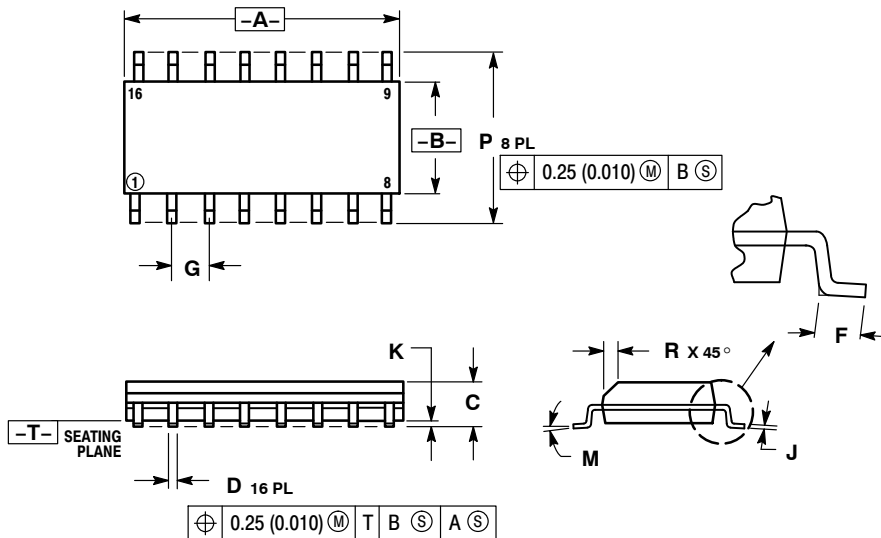
PDIP-16
N SUFFIX
CASE 648-08
ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



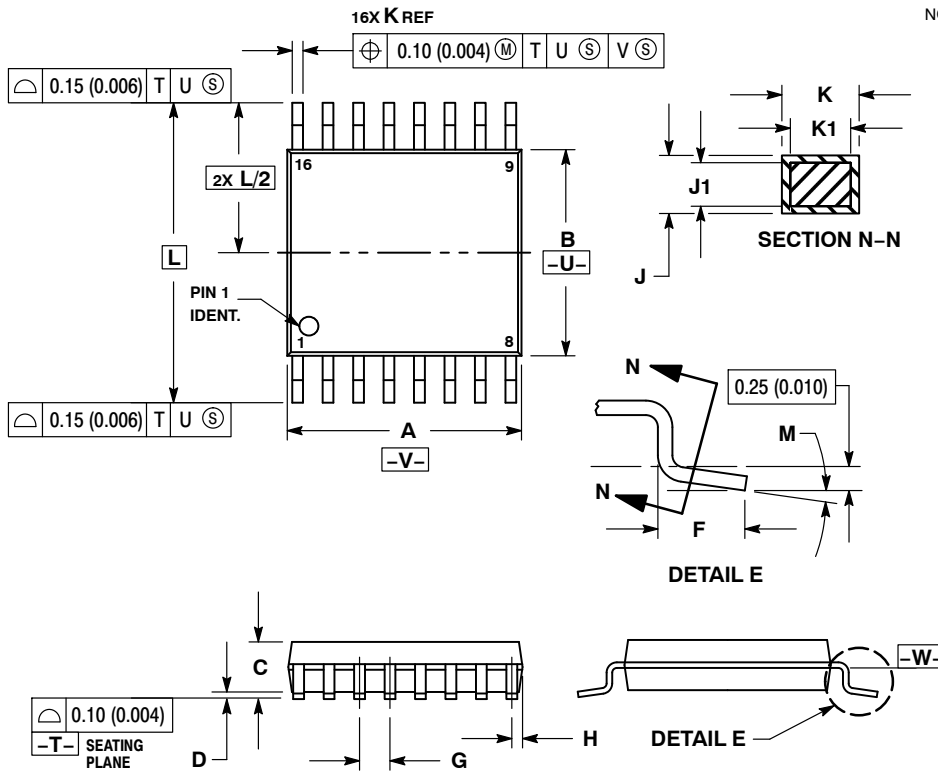
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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