Half-bridge evaluation board with TDI EiceDRIVER™ 1EDN7116G gate driver and OptiMOS™ 6 100 V MOSFET

About this document

Scope and purpose

This user guide provides an overview and detailed feature description of the EVAL_7116G_100V_SSO8 general-purpose half-bridge evaluation board with OptiMOS™ 6 ISC022N10NM6 MOSFET and TDI EiceDRIVER™ 1EDN7116G gate driver.

The EVAL_7116G_100V_SSO8 is designed to showcase the performance of the ISC022N10NM6 when used with the TDI EiceDRIVER™ 1EDN7116G in a half-bridge configuration. For this purpose, it provides optimized waveform measurement points and other features enabling easy lab bench usage.

Intended audience

The intended audience for this document is power electronic engineers, technicians, and developers of power electronic systems which are interested in evaluating the performance of OptiMOS™ 6 MOSFET and the TDI EiceDRIVER™ 1EDN7116G gate driver.

Evaluation Board

This board is to be used during the design-in process for evaluating and measuring characteristic curves, and for checking datasheet specifications.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 The board at a glance

The EVAL_7116G_100V_SSO8 shown in the following figure is a board for general-purpose evaluation of OptiMOS™ 6 100V MOSFET in SSO8 package together with TDI EiceDRIVER™ 1EDN7116G gate driver. This board includes an optimized layout for a hard-switching half-bridge, as well as waveform measurement points and other useful features to enable easy lab bench characterization of the switch and the driver. It is pre-configured to run as a buck or boost converter, but you can easily reconfigure the board for a double pulse test or any half-bridge topology with external connections.

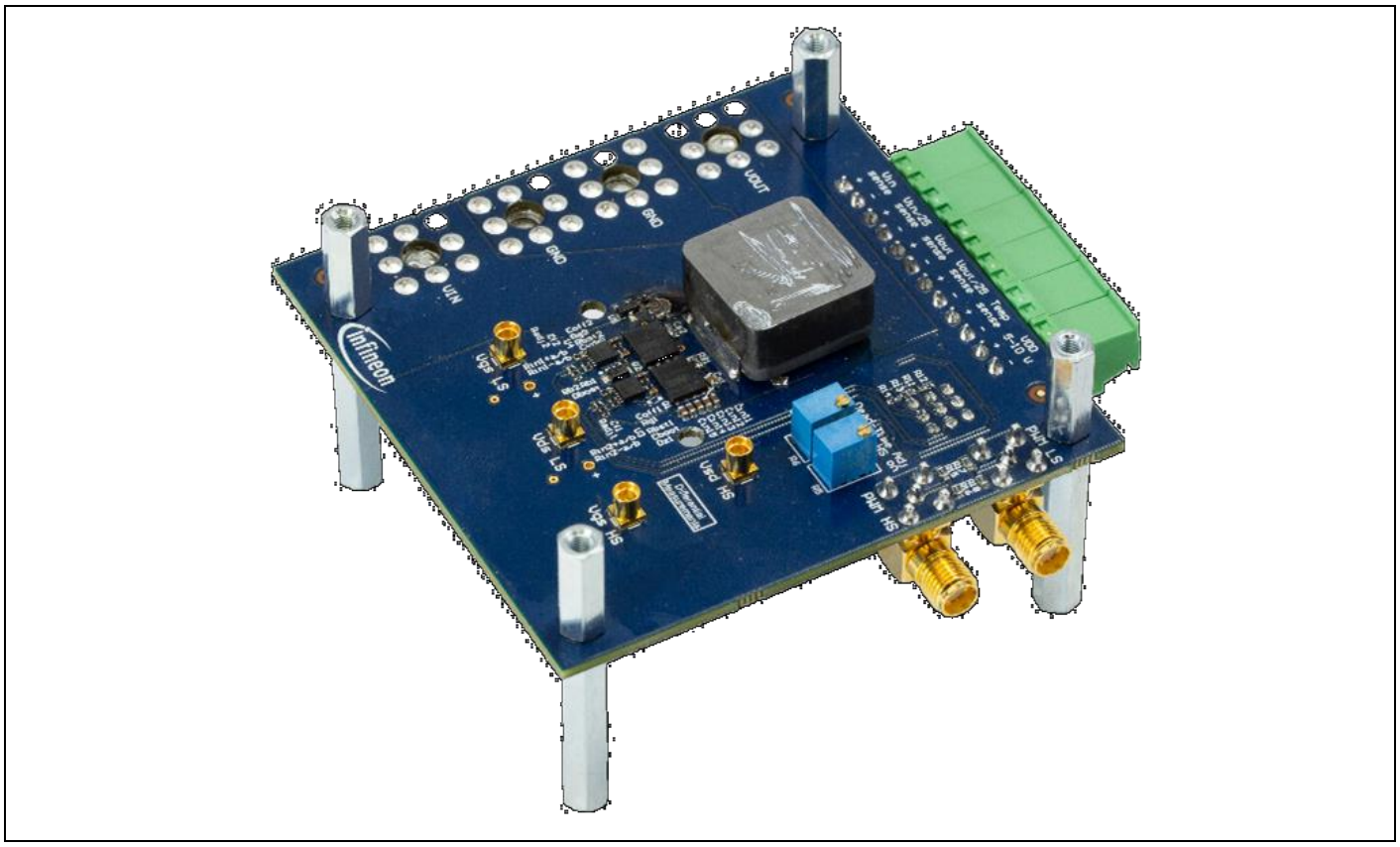


Figure 1 EVAL_7116G_100V_SSO8

1.1 Scope of supply

The main part of the board consists of high-side and low-side FETs in half-bridge topology driven by two TDI EiceDRIVER™ 1EDN7116G gate driver. It can be controlled either directly by two PWM input signals or if only one PWM is available, the second PWM signal can be generated by making use of the onboard dead-time generation circuit. With this dead-time circuitry, both dead-times can be set using an onboard trimmer freely. The board comes without power inductor assembled but two large pads are available to solder any kind of power inductor. Additionally, input and output capacitors are assembled onboard which provide enough capacitance for most of the operating conditions when the board can be operated. A DC power supply and load can be connected to the four power connectors labeled as “V_{IN}”, “V_{OUT}” and “GND”.

1.2 Block diagram

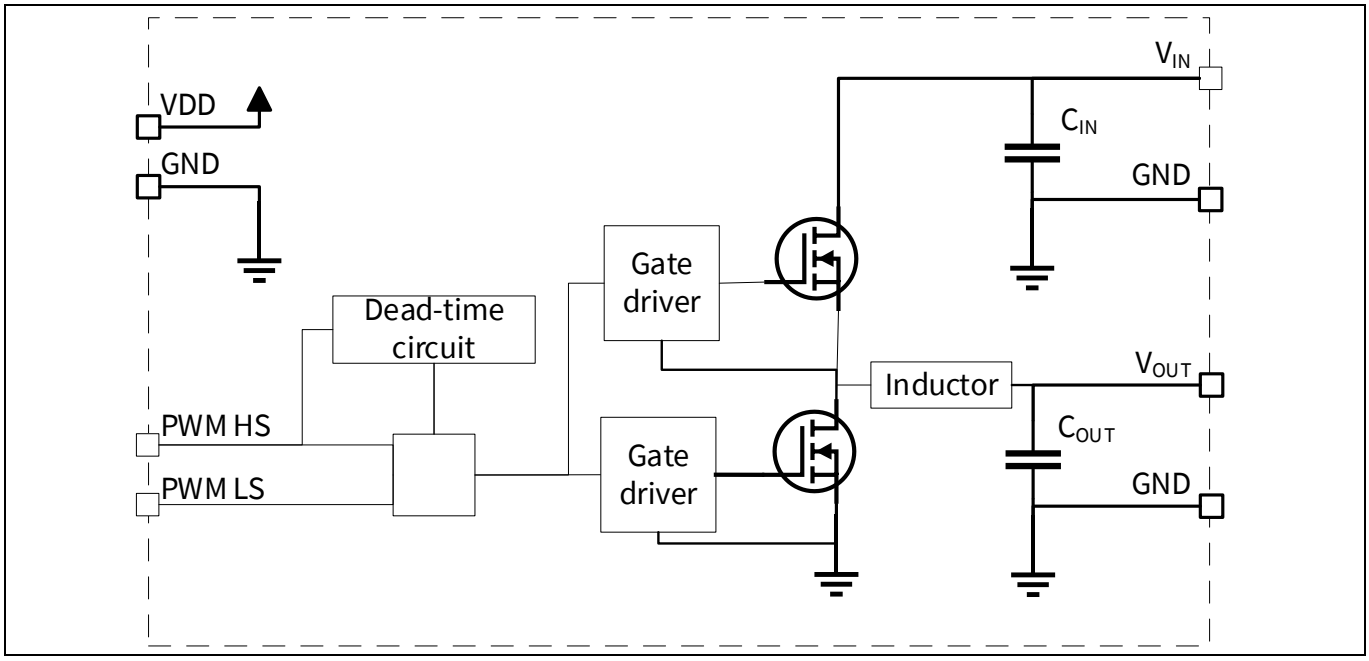


Figure 2 EVAL_7116G_100V_SSO8 block diagram

1.3 Main features

The EVAL_7116G_100V_SSO8 board comes with several key features including:

- Optimized layout
- Different PWM inputs options (see Section 2.1.1)
- Onboard dead-time generation (see Section 2.1.1)
- Onboard temperature sensing (see Section 2.4.4)
- Different heatsink assembly options (see Section 2.1.2)
- Optimized measurement points (see Section 2.4)

1.4 Board parameters and technical data

Table 1 Board characteristics

Parameter	Values			Unit	Note
	Min	Typ	Max		
V_{DD} supply current	–	60	–	mA	With charge pump set to -1 V. At 600 kHz
V_{IN} to GND	–	–	100	V	Limited by capacitor voltage ratings
V_{OUT} to GND	–	–	100	V	Limited by capacitor voltage ratings
On-board deadtime adjustment range	10	–	100	ns	Limits depend on accuracy of trimmers

Table 2 Recommended operating conditions

Parameters	Values			Unit	Note
	Min	Typ	Max		
VDD Supply voltage	–	10	11	V	–
V_{IN} to GND	–	–	80	V	–
V_{OUT} to GND	–	–	80	V	–
PWM voltage level	–	5	–	V	Rework needed for 3.3 V signals, see 2.5.1
DC input/output current	–	–	25	A	At 400 kHz – 48 V input – bottom heatsink

2 System and functional description

2.1 Description of the functional blocks

2.1.1 PWM options

There are different options for the PWM signals to control the half-bridge and as follows:

- Dual 5 V logic inputs with 50 Ω terminated SMA
- Dual 3.3 V logic inputs with 50 Ω terminated SMA (rework needed, see 2.5.1)
- Dual 5 V logic inputs with High-Z terminated 3-pin header
- Single high-side 5 V logic input with onboard dead-time generator

Option 1: When using a two-channel benchtop function/waveform generator to supply both high-side and low-side PWM signals, the most convenient option is to connect them via the PWM HS and PWM LS SMA connectors. Each SMA input is terminated with 50 Ω and configures the function generator to drive a 50 Ω load. In the default configuration of the board, all logic signals must be based on 5 V, not 3.3 V. To configure the board for 3.3 V logic, see the rework for further instructions in 2.5.1.

Option 2: Connect a single high-side PWM signal from a waveform generator with 5 V logic and 50 Ω termination. The second PWM can then be generated using the onboard dead-time generation circuit with dead-time determined by the R5 and R6 trimmer resistors. The maximum dead-time achievable with this circuit is about 100 ns per edge, but it is recommended to start with a value close to 10 ns per edge.

Option 3: The dual PWM signals can also be supplied directly at the header J1, but with a High-Z termination rather than 50 Ω. Configure the function generator or other signal source to drive a High-Z load, rather than 50 Ω. How to set the jumpers or connect to a High-Z source as shown in the following figure.

Figure 3 Jumper J1 settings for dual 50 Ω logic inputs (1), single high-side 5V logic input (2), and dual 5 V High-Z terminated logic inputs (3)

2.1.2 Heatsink attachment options

The provided heatsink comes with a pre-installed pad of t-Global TG-A1780, which is an ultra-soft galvanically isolated TIM pad with a thermal conductivity of 17.8 W/mK and a thickness of 0.5 mm.

Other recommended TIM pads are: TG-A1780, TG-A1660, TG-A1450, or TG-A1250.

The heatsink can be installed on the underside of the PCB for bottom-side cooling or on top of the transistors for dual-sided cooling. To install the heatsink on either side, first remove the plastic protective tape, then place the heatsink in the desired location. Next, evenly compress both spring pins at the same time. It is recommended to use two flat-head (slotted) screwdriver or similar tool to avoid finger injury on the pin fins.

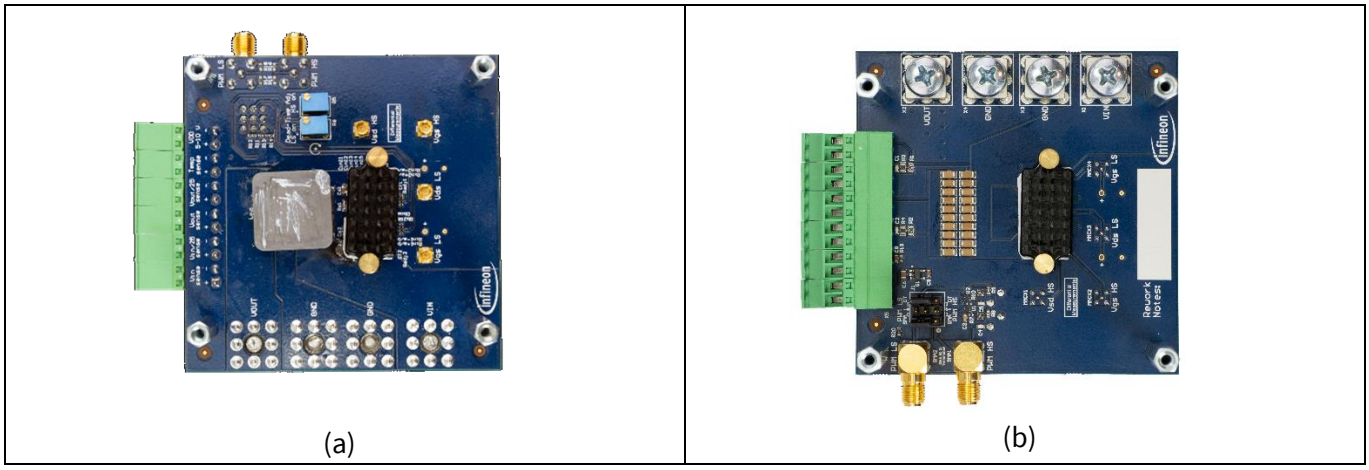


Figure 4 Heatsink attachment options (a) top and (b) bottom

2.1.3 Inductor mounting

The board comes without a power inductor assembled but two large pads that gives the flexibility to solder any kind of power inductor. The following are two options of power inductors which have been considered to take some measurements.

- SER2918H from Coilcraft
- IHLP8787 from Vishay

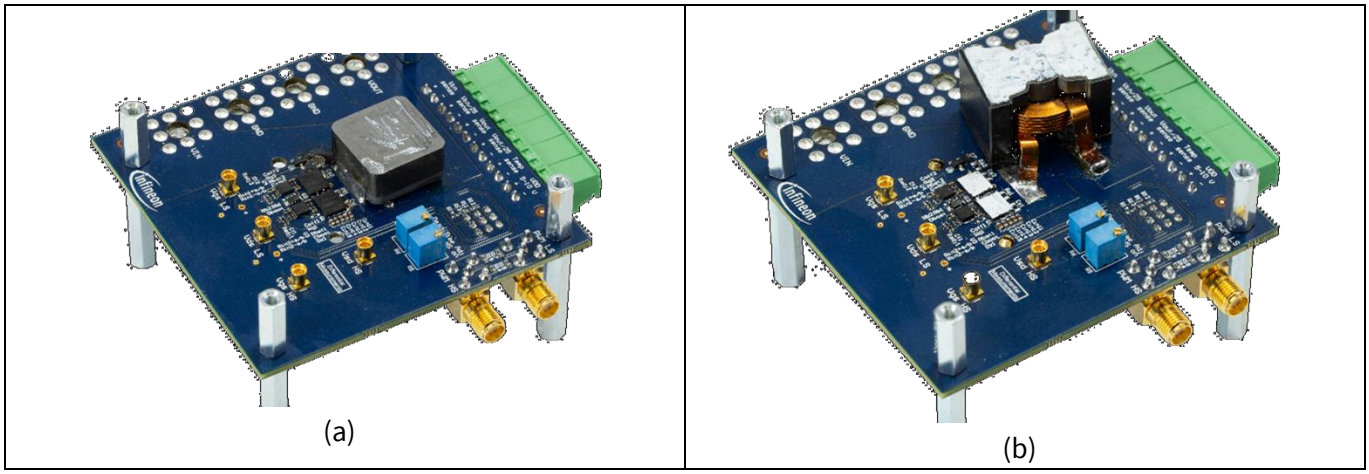


Figure 5 Mounted power inductors (a) IHLP8787 from Vishay and (b) SER2918H from Coilcraft

2.1.4 TDI EiceDRIVER™ 1EDN7116G

The EiceDRIVER™ 1EDN71x6G is a single-channel high-side and low-side gate-driver IC compatible with GaN SG HEMTs and silicon MOSFETs. Its key features enable a high-performance system design with fast-switching transistors, including truly differential input (TDI), four driving strength options, active Miller clamp, bootstrap voltage clamp, and adjustable charge pump to provide negative off-state voltage in PG-SON-10 package [1].

The active bootstrap voltage clamp of the driver enables supplying the high-side switch via the BST pin of the low-side driver which prevents overcharging of the decoupling capacitor next to the high-side gate driver during dead-time.

However, in the EVAL_7116G_100V_SSO8 board where overcharging will not be an issue, a conventional bootstrapping method is used by supplying the high-side switch via the VDD pin of the low-side driver; allow increasing the driving strength by connecting the BST pin together with the output source and sink pins.

Another feature of the driver is the adjustable negative charge pump that can be set by the external resistors to supply a desirable negative off-state driving voltage, which provides additional induced turn-on immunity when the active Miller clamp is not sufficient. Voltage is set before power-up of IC, so the voltage cannot be adjusted during operation. The different setup options for the charge pump are shown in Table 3. In the EVAL_7116G_100V_SSO8 board, the CP is set to provide a V_{OFF} of -1 V by mounting adjust resistor of 3.3 KΩ.

Table 3 Adjustable charge pump settings

V_{OFF} voltage	**Adjust resistor**
Disabled (floating)	< 0.75 kΩ
–0.5 V	1.5 kΩ
–1 V	**3.3 kΩ**
–1.5 V	6.8 kΩ
–2 V	15 kΩ

For more details about the EiceDRIVER™ 1EDN7116G gate driver, visit the 1EDN7116G webpage.

2.1.5 OptiMOS™ 6 100 V ISC022N10NM6 MOSFET

ISC022N10NM6 OptiMOS™ 6 100 V MOSFET in normal level is setting the new technology standard in the field of discrete power MOSFETs. The latest OptiMOS™ 6 MOSFET technology at 100 V from Infineon utilizes a proprietary novel needle trench technology that enables higher power density, efficiency, and ruggedness. Compared to alternative products, Infineon's leading thin wafer technology is enabling significant performance benefits. In the SuperSO8 package, it achieves ~20% improvements in on-state resistance (RDS(on)) and 30% better figure of merits (FOM - RDS(on) x Qg and Qgd) compared to the previous technology OptiMOS™ 5 MOSFETs. This enables designers to increase efficiency, allowing easier thermal design and less paralleling, leading to system cost reduction [2].

2.1.6 RC snubber circuit

The snubber circuit consists of a resistor and capacitor that are connected in series and parallel to the FETs. The snubber circuit is used to damp the oscillations generated by the parasitic inductances and capacitances during the switching transitions. The EVAL_7116G_100V_SSO8 board comes with footprint for optional RC snubber across the high-side and low-side FETs. Placing a snubber helps to eliminate the excessive switching spikes and ringing that can develop across the FETs when switching fast. However, the power dissipated by these extra components reduces the overall system efficiency.

The RC snubber must be sized properly to get an optimized performance. Select the size of the capacitor based on how much energy need to be absorbed, then depending on the capacitor, estimate the resistor needed for dissipating the power [3]. For more details about sizing the snubber, see [3].

2.2 Basic operation: Buck converter test setup

The board can be run in a buck mode using the test setup shown in Figure 6. This test mode is useful for performance characterization as well as waveform measurements, especially when the motivation is to measure the gate and drain voltage waveforms of the low-side switch Q2 when soft-switching.

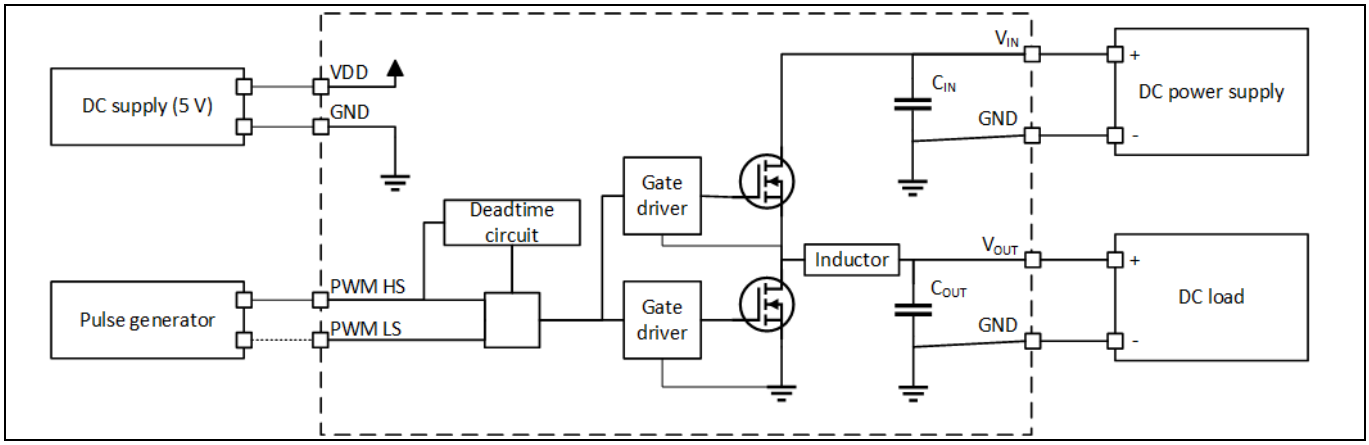


Figure 6 Buck converter test setup

2.3 Other operation modes

The design and connections of the EVAL_7116G_100 V_SSO8 board enable to use it in different test setups. It can be operated in the following setups:

- Boost-converter test setup
- Buck-converter double pulse test setup
- Boost-converter double pulse test setup

2.3.1 Boost-converter test setup

The board can be configured to run as a boost converter using a power inductor and a bank of 100 V bulk capacitance on the bottom side of the board for V_{IN} and V_{OUT}. In contrast to buck mode, reverse the connections for V_{IN} and V_{OUT} with a voltage supply on V_{OUT} and a DC load on V_{IN}.

This test mode is useful for performance characterization as well as waveform measurements, especially when the motivation is to measure the gate and drain voltage waveforms of the low-side switch when hard-switching.

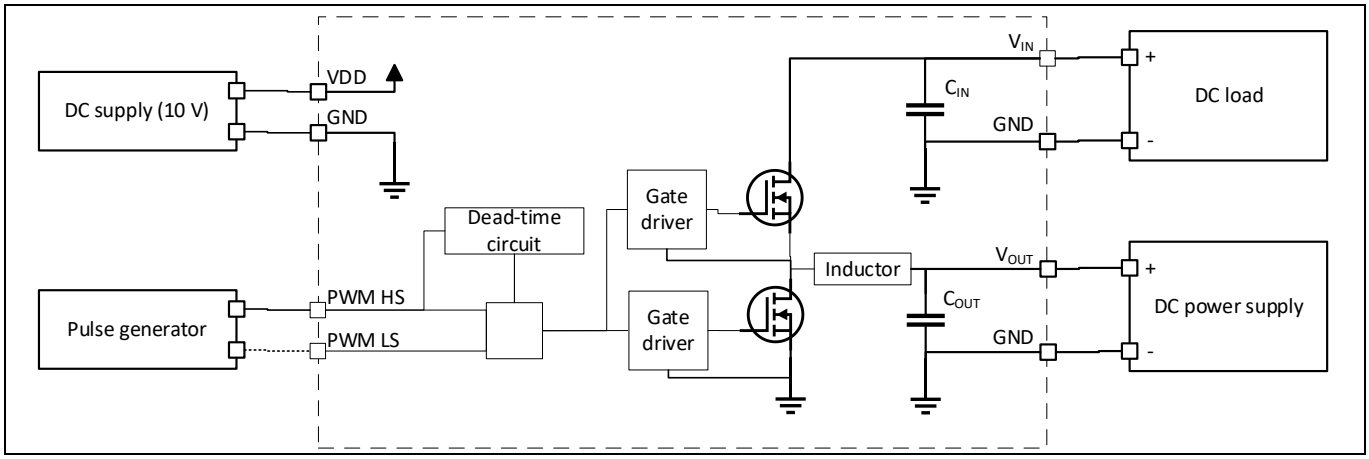


Figure 7 Boost converter test setup

2.3.2 Double pulse test setup

Two different types of double pulse tests can be performed: buck- and boost-modes. For both modes, the inductor must have a high inductance value, typically in the range of 10 to 100 µH, often routed off-board with cables to allow inductor current measurement using a split-core current probe.

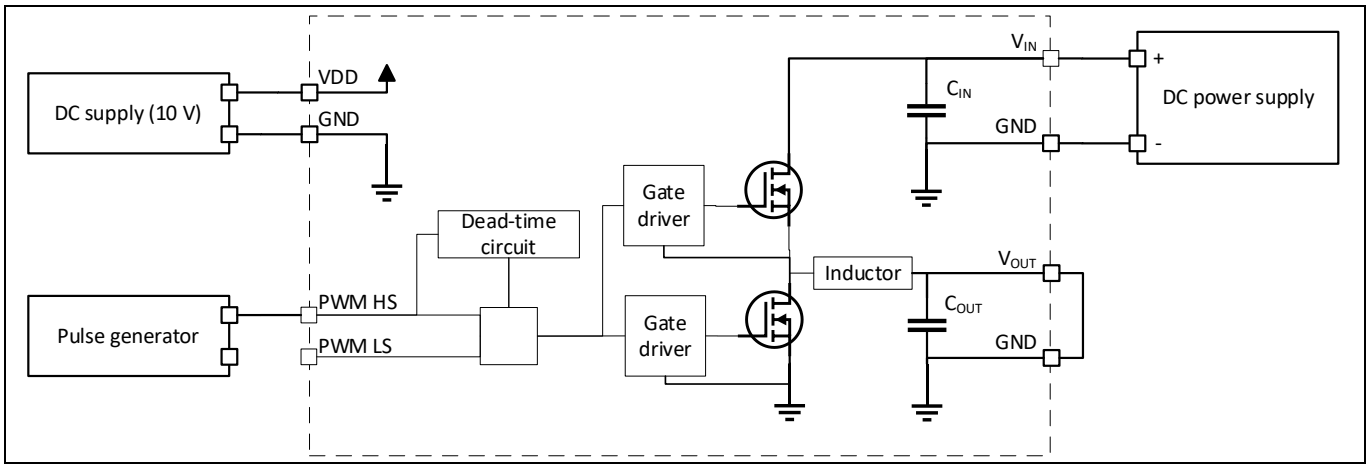


Figure 8 Buck-mode double pulse test setup

Buck-mode double pulse testing enables capturing soft-switching voltage waveforms without self-heating effects. Connect V_{OUT} to the GND and a DC power supply to V_{IN}. The high-side PWM is sent two pulses: one long pulse to raise the inductor current to the desired level, and one short pulse to view the turn-on and turn-off transitions [4], [5]. Typically, set the low-side PWM input manually to 0 V for safety during this test. Implement this on jumper J3 as shown in Figure 10.

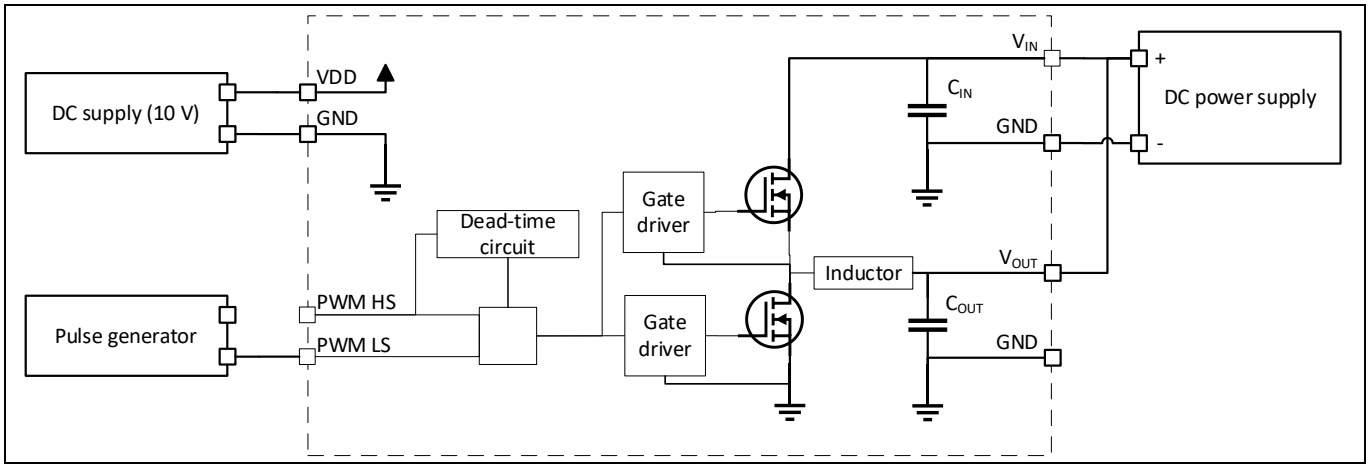


Figure 9 Boost converter double pulse test setup

The second option is the boost-mode double pulse testing which enables capturing hard-switching voltage waveforms without self-heating effects. Connect V_{IN} to V_{OUT} with a DC voltage supply provided to both. For boost-mode double pulse testing, the low-side PWM is sent two pulses: one long pulse to raise the inductor current to the desired level, and one short pulse to view the turn-on and turn-off transitions. Typically, set the high-side PWM input manually to 0 V for safety during this test. Implement this on jumper J3 as shown in Figure 10.

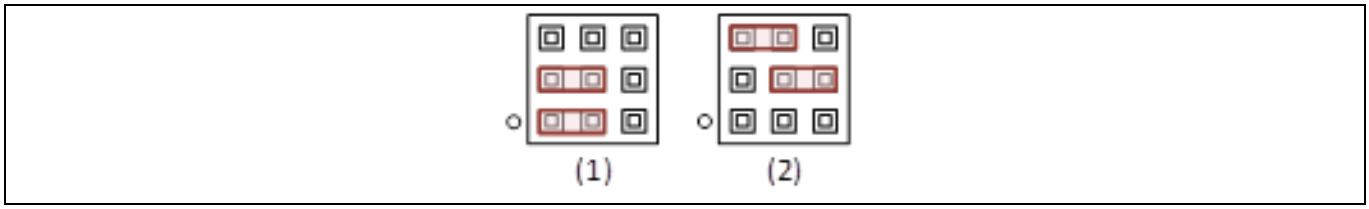


Figure 10 Double pulse test jumper settings for buck-mode (1) and boost-mode (2)

2.4 Measurement options

2.4.1 DC voltage measurements

The board is equipped with convenient screw terminal plugs for the DC measurements.

Input and output voltage can be measured with or without 25x attenuation, making it compatible with a digital multimeter or datalogger for efficiency measurements, or alternatively for inputs to an external controller.

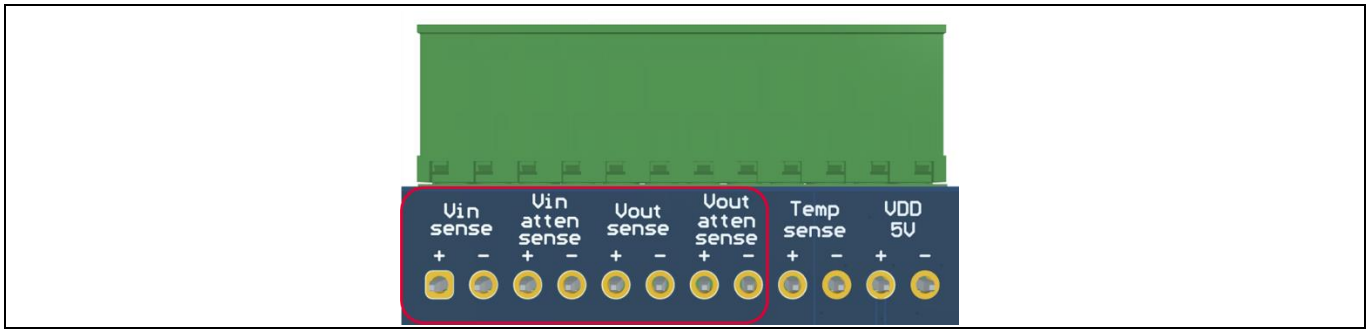


Figure 11 Screw terminal plugs for DC voltage measurement

2.4.2 Low-side single-ended voltage measurements

Any passive probe can be used to measure the low-side voltage waveforms of OptiMOS™ 6 MOSFET, but they should have suitable bandwidth and connectivity. The recommended bandwidth for all voltage probes and oscilloscopes is minimum 1 GHz.

The loop between the probe tip and the measurement points (both + and – sides) should be within 10 mm, preferably shorter. One example of a recommended probing solution is TPP1000 from Tektronix [6] with MMCX tip adapter 206-0663-xx, as shown Figure 12, which guarantees the tightest possible probing loop for this tip. An alternative recommended passive MMCX probe is the MMCX-A1025 probe from PMK. As a second option, a “spring clip” probe tip solution can be used at the provided vias, but this does degrade the measurement fidelity to some degree.

V_{DS_LS} can be measured in three locations: MMCX, two vias beside the MMCX, or two vias located very close to the low-side switch. V_{GS_LS} can be measured at the MMCX or at the vias beside it.

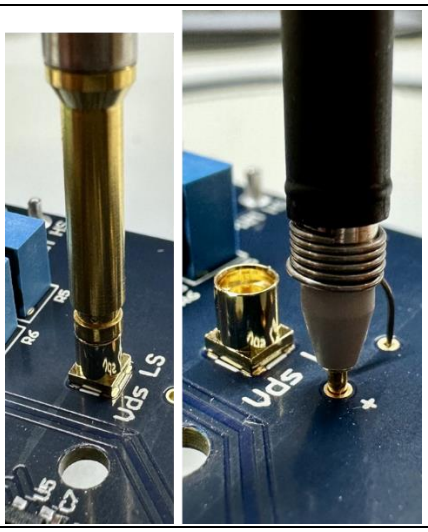


Figure 12 Low-side single-ended voltage measurements

2.4.3 High-side differential voltage measurements

In general, high-side voltage waveforms measurements are challenging due to the extremely high dV/dt and dI/dt involved. The most accurate measurement scheme comes from an extremely high-bandwidth optically isolated probing system, for example, the isoVu system from Tektronix [8] or the FireFly series from PMK [9].

In addition to the bandwidth of the probing system, the probing loop connectivity is critical. An MMCX tip adapter for high-side differential measurements is very important for an accurate measurement with the highest fidelity and the lowest signal degradation.

Figure 13 High-side differential voltage measurements with high-bandwidth differential probes

2.4.4 Temperature measurements

The board is equipped with an onboard PCB temperature sensor, but it is recommended to use a contacting thermocouple solution or an infrared thermal camera to capture the temperature of the OptiMOS™ 6 MOSFET, as well as the power inductor. When using a thermal camera, it is highly recommended to paint all target surfaces with a matte-finish paint (white or black is commonly used) to ensure that the emissivity is consistent for all temperature measurements [10].

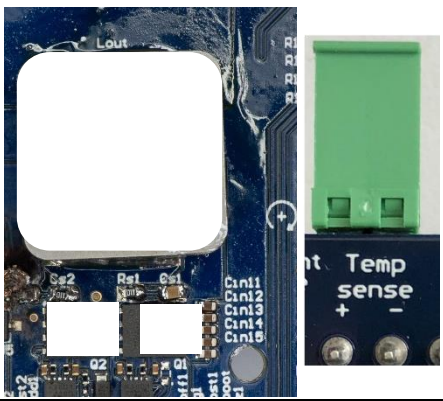


Figure 14 Exemplary white painted surfaces for temperature measurement with a thermal infrared camera (left) and screw terminal plug connection to sense the output of the onboard temperature sensor (right)

2.5 Rework options

2.5.1 TDI resistor adjustment for 3.3 V PWM input

TDI EiceDRIVER™ 1EDN7116G gate driver utilizes a truly differential input (TDI) circuit for common-mode voltage rejection, as an alternative to level-shifting or galvanic isolation. Select the input resistor values based on the logic voltage level of the PWM inputs, e.g., 5 V or 3.3 V. The default configuration of the board has a TDI resistance of 28 kΩ + 47 kΩ = 75 kΩ, required for a 5 V logic input.

To use dual 3.3 V logic inputs, e.g., from an external control board, reduce the input resistance from 75 kΩ to 47 kΩ. To enable 3.3 V logic inputs, you can solder 0 Ω resistors or solder bridge the four positions ending in byp to bypass the 28 kΩ resistors, leaving only 47 kΩ un-bypassed.

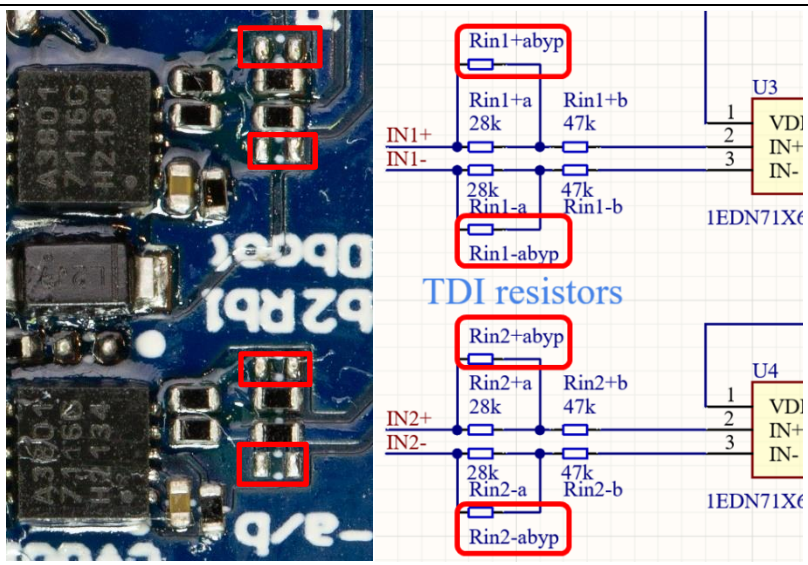


Figure 15 Rework option for 3.3 V input PWM signal

2.5.2 Cross-connect PWM inputs for overlap protection

By default, the input PWM signals can be overlapped to achieve short dead-times. Enable overlap protection by cross-connecting the IN+ and IN- signals between the gate drivers. Therefore, remove 0 Ω resistors R11 and R13, and place them on positions R12 and R14 as shown in the following figure. With this rework, the shortest achievable effective dead-time can be slightly higher.

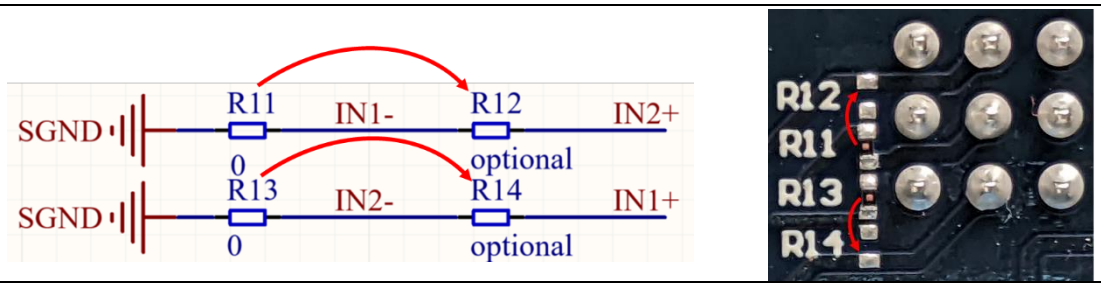


Figure 16 Rework option for overlap protection of the PWM input signals

3 System design

3.1 Schematics

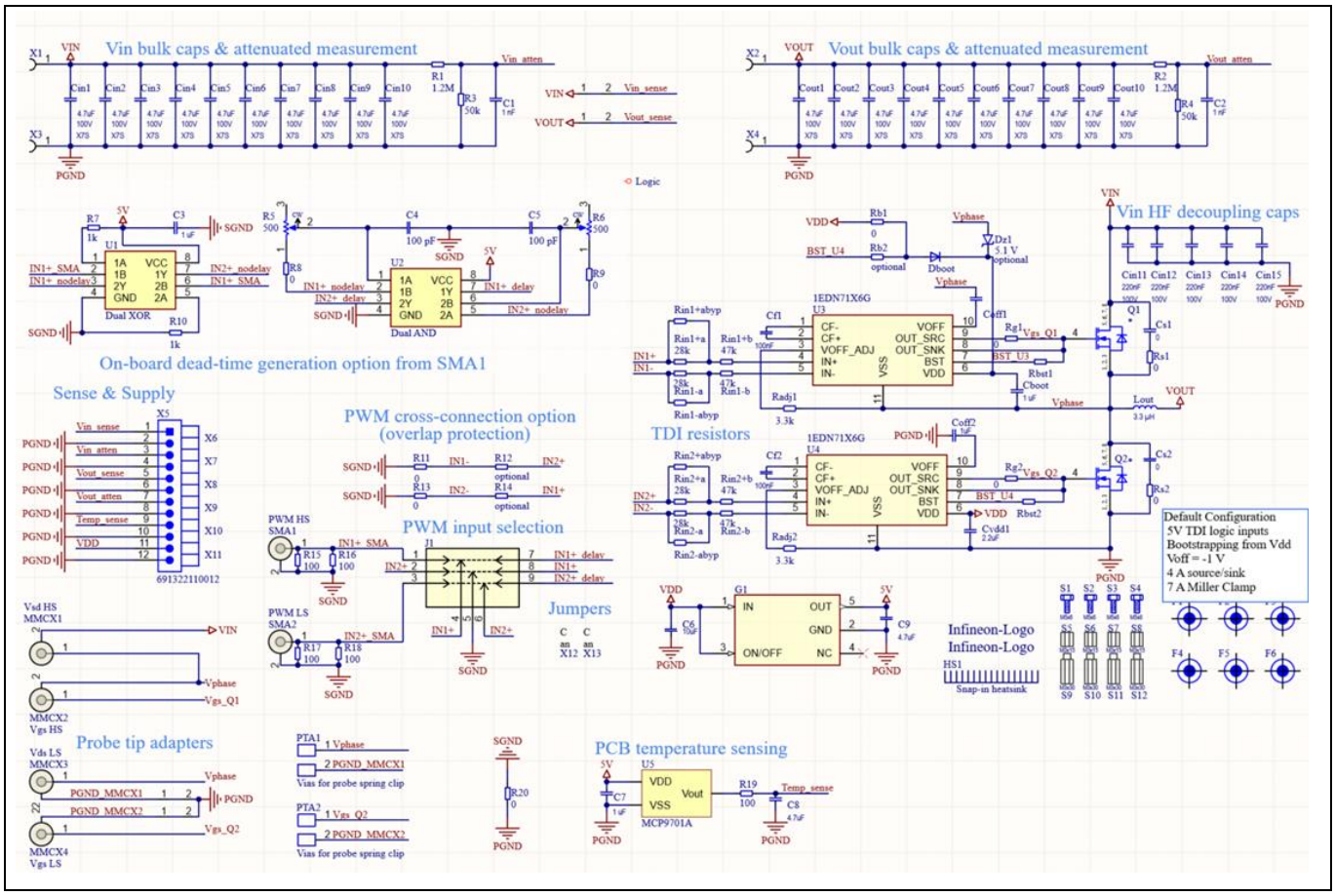
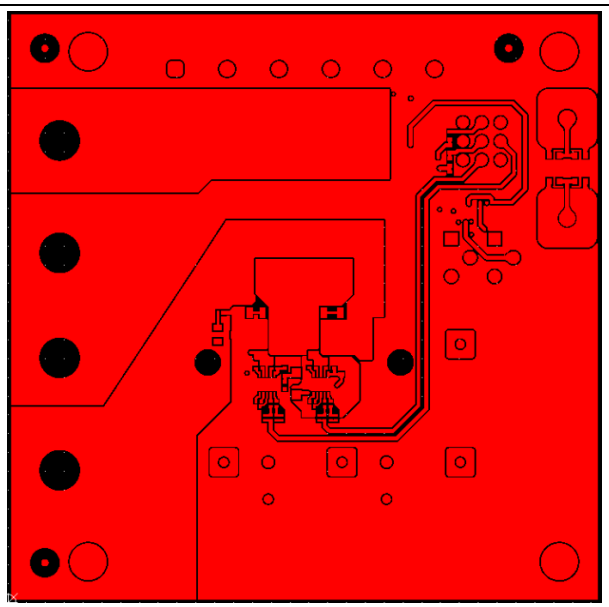
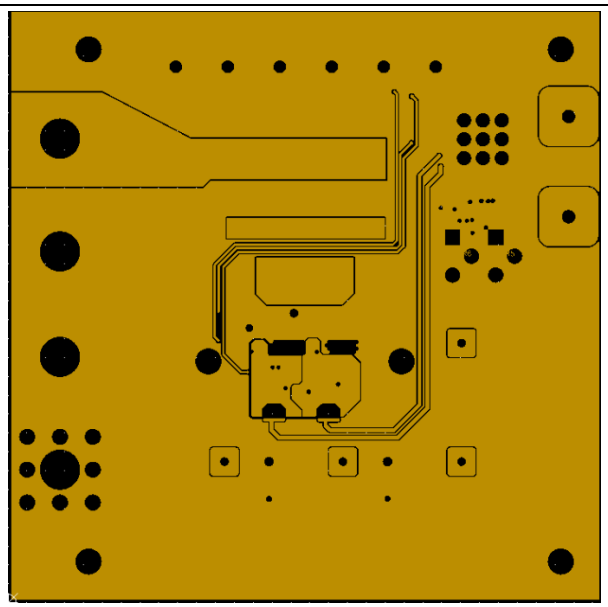


Figure 17 Schematics of the EVAL_7116G_100V_SSO8 board

3.2 Layout

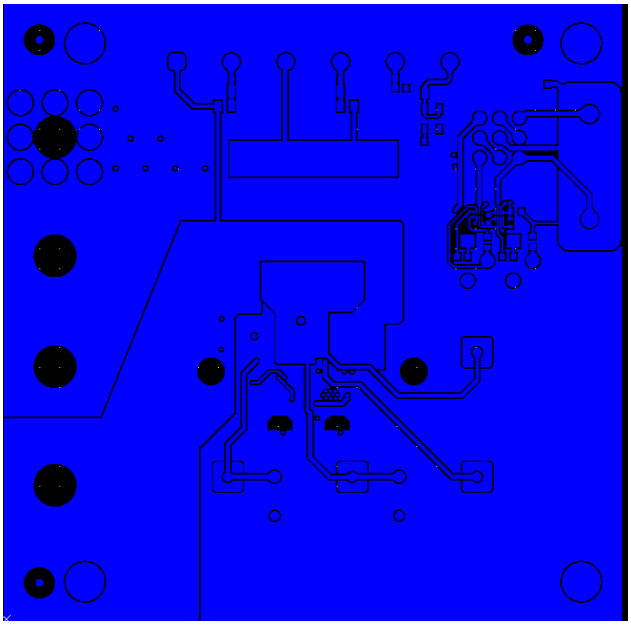


(a)

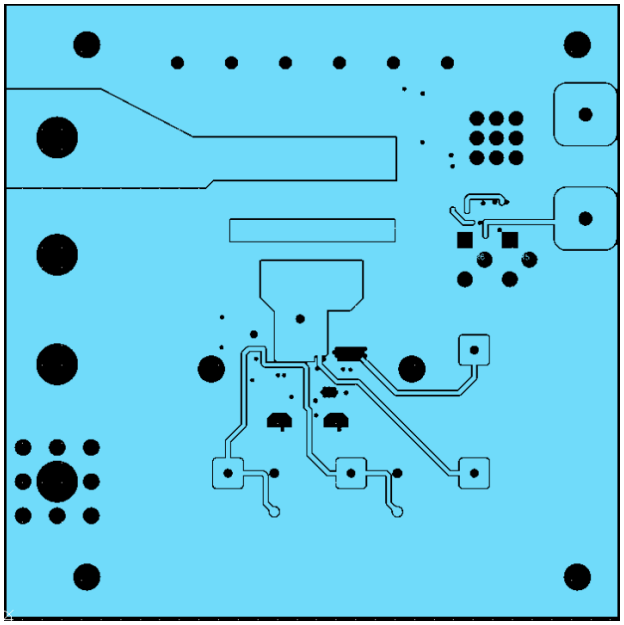


(b)

Figure 18 Gerber files of the EVAL_7116G_100V_SSO8 (a) top layer (b) mid layer 1



(a)



(b)

Figure 19 Gerber files of the EVAL_7116G_100V_SSO8 (a) bottom layer (b) mid layer 2

3.3 Bill of materials

Table 4 BOM of the EVAL_7116G_100V_SSO8

S. No.	Ref designator	Description	Manufacturer	Manufacturer P/N	Populated
1	C1, C2	1 nF	Kemet	C0603C102K3GACTU	Fitted
2	C3	1 uF	Murata	GCM188R71E105KA64D	Fitted
3	C4, C5	100 pF	Würth Elektronik	885012006023	Fitted
4	C6	10uF	Murata	GRM21BC71E106ME11L	Fitted
5	C7, Cboot	1 uF	Murata	GRT155C81E105KE13D	Fitted
6	C8, C9	4.7uF	Murata	GRM188C81E475KE11D	Fitted
7	Cf1, Cf2	100nF	Taiyo Yuden	TMK105B7104KVHF	Fitted
8	Cin1 ~ Cin10, Cout1 ~ Cout10	4.7uF	Murata	GRM31CC72A475ME11L	Fitted
9	Cin11, Cin12, Cin13, Cin14, Cin15	220nF	Taiyo Yuden	HMK107C7224KAHTE	Fitted
10	Coff1, Coff2	1uF	Murata	GRT155C81E105KE13D	Fitted
11	Cs1, Cs2	0	Murata	GRT155C81E105KE13D	Not fitted
12	Cvdd1	2.2uF	Murata	GRM155C81E225ME11D	Fitted
13	Dboot	Schottky diode	ON semi	MBR2H200SFT1G	Fitted
14	Dz1	Optional	Diodes Inc	BZT585B5V1T-7	Not fitted
15	G1	–	Texas Instruments	LP2980IM5-5.0/NOPB	Fitted
16	HS1	Heatsink	–	–	Not Fitted
17	J1	–	Samtec	TSW-103-07-G-T	Fitted
18	Lout	3.3 µH	Vishay	IHLP7575JZER3R3M5A	Not fitted
19	MMCX1, MMCX2, MMCX3, MMCX4	MMCX vertical jack	Würth Elektronik	66012002111503	Fitted
20	Q1, Q2	–	Infineon	ISC030N10NM6	Fitted
21	R1, R2	1.2M	Susumu	RG2012P-125-B-T5	Fitted
22	R3, R4	50k	Vishay	PTN0805E5002BST1	Fitted
23	R5, R6	500	Vishay	T63YB501KT20	Fitted
24	R7, R10	1k	Stackpole	RMCF0402FT1K00	Fitted
25	R8, R9, R20	0	YAEGO	RC0603JR-070RL	Fitted
26	R11, R13, Rb1	0	Stackpole	RMCF0402ZT0R00	Fitted
27	R12, R14	Optional	–	–	Not fitted
28	R15, R16, R17, R18, R19	100	Stackpole	RMCF0603FG100R	Fitted
29	Radj1, Radj2	3.3k	Stackpole	RMCF0402JT3K30	Fitted
30	Rb2	Optional	Stackpole	RMCF0402ZT0R00	Not fitted
31	Rbst1, Rbst2, Rg1, Rg2	0	Stackpole	RMCF0402ZT0R00	Fitted
32	Rin1+a, Rin1-a, Rin2+a, Rin2-a	28k	Panasonic	ERA-2APB2802X	Fitted

S. No.	Ref designator	Description	Manufacturer	Manufacturer P/N	Populated
33	Rin1+abyp, Rin1-abyp, Rin2+abyp, Rin2-abyp	Optional	–	–	Not fitted
34	Rin1+b, Rin1-b, Rin2+b, Rin2-b	47k	Panasonic	ERA-2APB473X	Fitted
35	Rs1, Rs2	0	YAEGO	RC0603JR-070RL	Not fitted
36	S1, S2, S3, S4	M5x6	RS PRO	(1/100) x 908-7693	Fitted
37	S5, S6, S7, S8	–	Wuerth Elektronik	970150321	Fitted
38	S9, S10, S11, S12	–	Wuerth Elektronik	971300321	Fitted
39	SMA1, SMA2	SMA jack	Würth Elektronik	60311002111526	Fitted
40	U1	Dual XOR	Diodes Inc	74LVC2G86HK3-7	Fitted
41	U2	Dual AND	Nexperia	74LVC2G08GS-Q100X	Fitted
42	U3, U4	TDI EiceDRIVER™ for GaN	Infineon Technologies	1EDN7116G	Fitted
43	U5	MCP9701AT-E/TT	Microchip Technology	MCP9701AT-E/TT	Fitted
44	X1, X2, X3, X4	–	Würth Elektronik	74655095R	Fitted
45	X5	–	Würth Elektronik	691322110012	Fitted
46	X6, X7, X8, X9, X10, X11	–	Würth Elektronik	691363110002	Fitted
47	X12, X13	–	Würth Elektronik	609002115121	Fitted

3.4 Connector details

Table 5 Connectors

No.	Label	Function
1	V_{DD} supply	Gate driver supply
2	V_{IN} Sense	Input voltage DC measurement
3	V_{OUT} Sense	Output voltage DC measurement
4	Temp Sense	Temperature DC measurement
5	V_{IN} Attenu Sense	Attenuated Input voltage DC measurement
6	V_{OUT} Attenu Sense	Attenuated output voltage DC measurement
7	PWM_HS	PWM input for the High side
8	PWM_LS	PWM input for the low side
9	V_{IN} Supply	DC Voltage supply
10	V_{OUT} load	Electronic load
11	GND	Ground

4 System performance

4.1 Test points

The board comes with the following test points which allows easy lab measurement and characterizations.

- Low-side drain to source voltage V_{DS_LS}
- High-side drain to source voltage V_{DS_HS}
- low-side gate to source voltage V_{GS_LS}
- High-side gate to source voltage V_{GS_HS}

4.2 Test results

In this section some lab measurement examples are shown at different test setup modes and several options.

The main tests that have been performed for evaluations are:

- Switching waveforms
- Efficiency measurement
- Thermal images

Testing conditions:

- Input V_{in} = 48 V / output V_{out} = 12 V (Buck) Input V_{in} = 12 V / output V_{out} = 48 V (Boost)
- Switching frequency: (a) 200 kHz and (b) 400 kHz
- Power Inductor: (a) SER2918H 10 µH from Coilcraft (b) IHLP8787 3.3 µH from Vishay
- RC snubber chosen: (a) without snubber (b) snubber 1 ohm – 1 nF
- Heat sink attachment: Bottom
- Still airflow

4.2.1 Switching waveforms

The switching waveforms of the EVAL_7116G_100V_SSO8 board that are shown in the following figure are taken at 200 kHz switching frequency, 20 A load, without RC snubber and using the SER2918H 10 µH power inductor.

When the EVAL_7116G_100V_SSO8 board works in buck configuration, the high-side FET is hard-switching that cause ringing and overshoot at the switch node as shown in V_{DS_LS} waveform in Figure 20. Likewise, the EVAL_7116G_100V_SSO8 board can work as a boost configuration simply by swapping the connection of V_{IN} and $V_{OUT.}$ When working as boost the low-side FET is hard-switching and the switch node ringing effect on the high-side FET in V_{DS_HS} is shown in Figure 21.

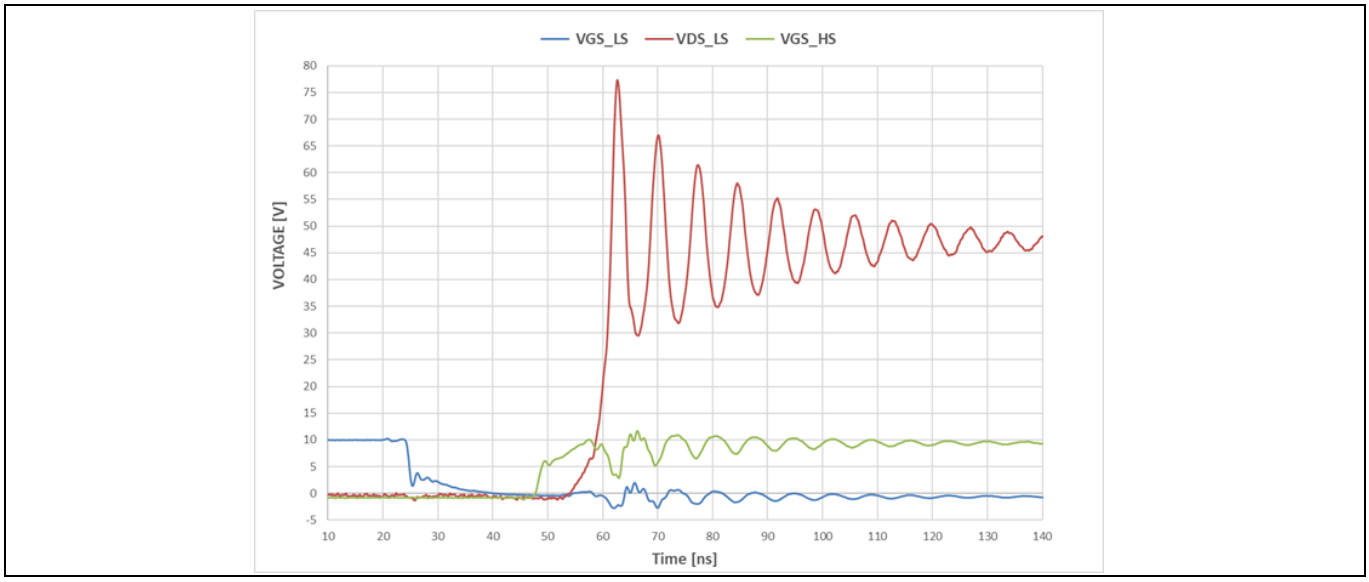


Figure 20 V_{DS_LS} overshoot and ringing during turn-on of high-side FET in buck mode – waveform at 20 A load

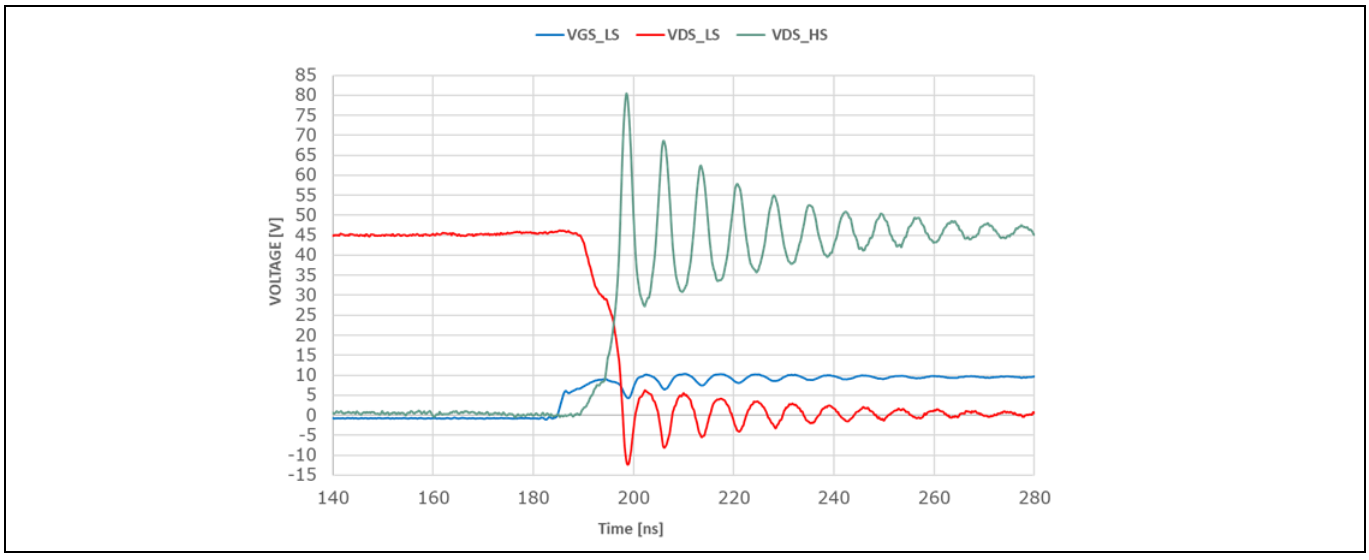


Figure 21 V_{SD_HS} overshoot and ringing during turn-on of low-side FET in boost mode – waveform at 20 A load

4.2.2 Efficiency measurement and thermal images

The EVAL_7116G_100V_SSO8 board efficiency has been measured at different conditions. Figure 22 shows a measurement example that compares the efficiency of the board using a 10 µH SER2918H inductor vs. 3.3 µH IHLP878 inductor. Relatively higher efficiency can be measured with the bigger inductor at lower switching frequency as shown for the 200 kHz example due to lower inductor ripple and lower switching losses. However, at higher switching frequency, the 400 kHz example current ripple and losses are almost similar for both inductors.

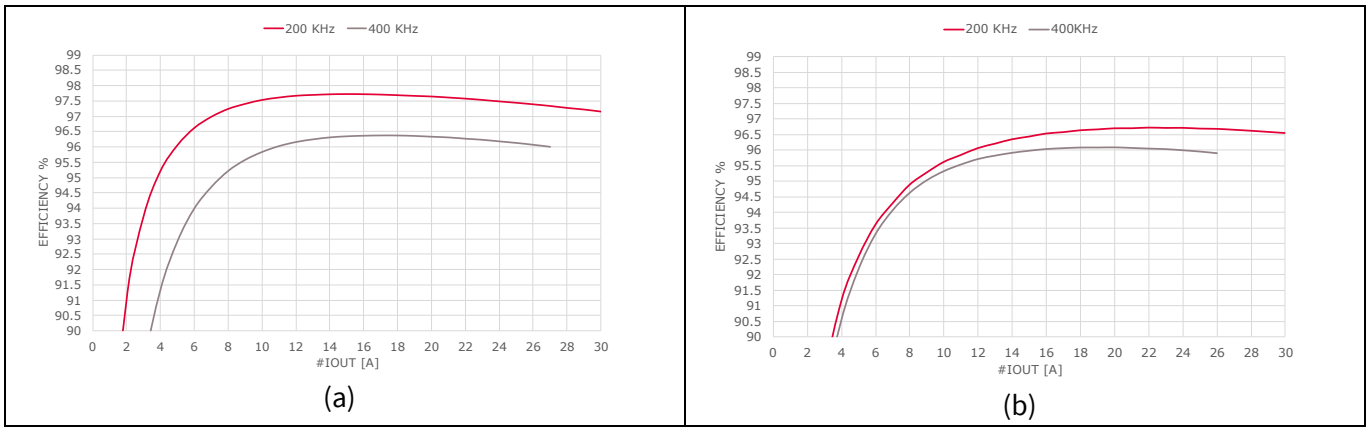


Figure 22 Efficiency at 48 V input line without using snubber (a) 10 µH SER2918H inductor (b) 3.3 µH IHLP878

Figure 23 and Figure 24 show the corresponding thermal performance of the EVAL_7116G_100V_SSO8 board at the end of the efficiency sweep where HS MOSFETs are hotter when the switching frequency is 400 kHz due to higher switching losses caused by the increase in switching frequency. At 200 kHz, the higher temperature is captured with the smaller inductor due to higher losses as explained earlier.

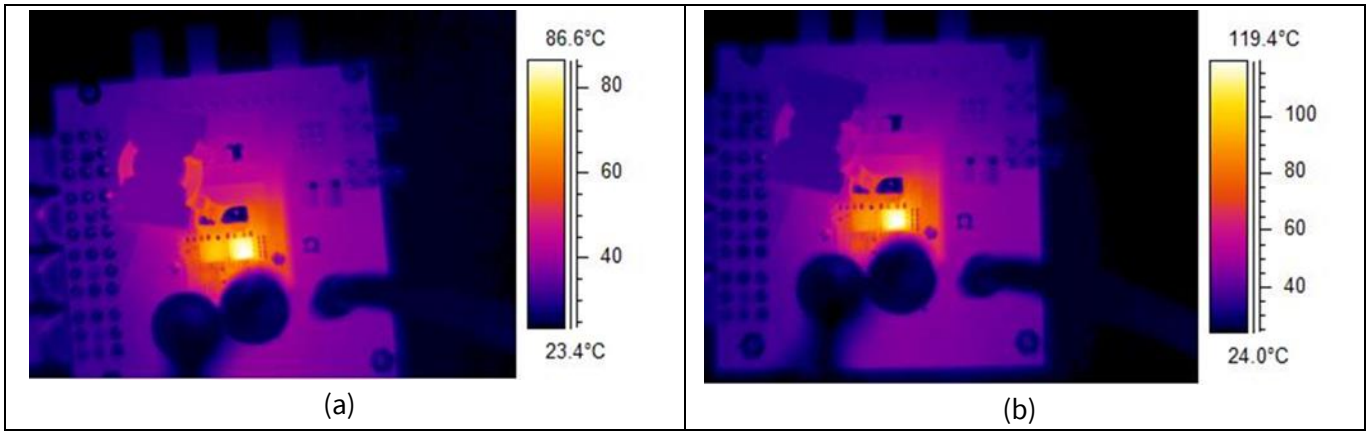


Figure 23 Thermal image at full load using the SER2918H (a) 200 kHz (b) 400 kHz

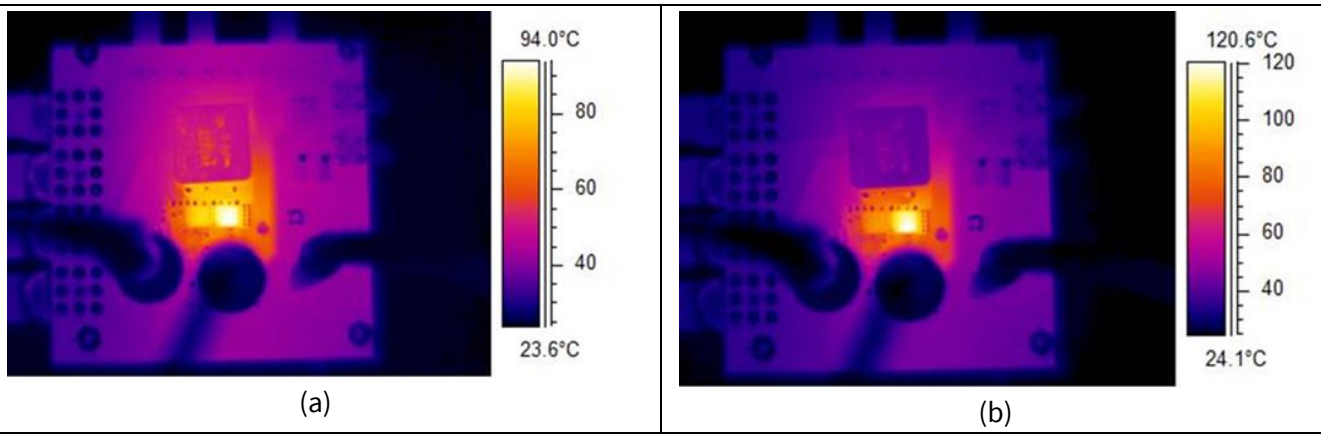


Figure 24 Thermal images at full load using 3.3µH IHLP8787 inductor (a) 200 kHz (b) 400 kHz

4.2.3 Measurement with the RC snubber

The RC snubber can be used for damping the ringing and voltage spikes across the FET that happen during switching transition due to the parasitics. These voltage spikes can be destructive to the FET if exceeded its absolute maximum rating. In addition, high dV/dt cannot be desirable as it can cause EMI issues.

A measurement example with the snubber is shown in this section using 1ohm _1nF snubber. Figure 25 shows reduced ringing and lower overshoot of the V_{DS_LS} waveform. However, this comes with tradeoff for the efficiency as shown in Figure 26. The more damping of the switching ringing and overshoot is needed bigger size of snubber will be required to absorb more energy which means higher losses and lower efficiency.

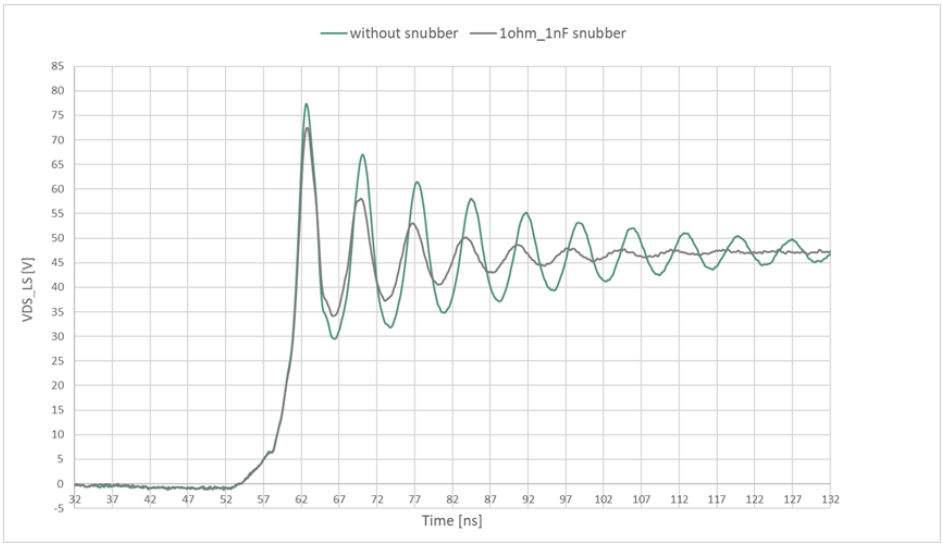


Figure 25 VDS_LS waveform at 200 kHz using 10 µH SER2918H

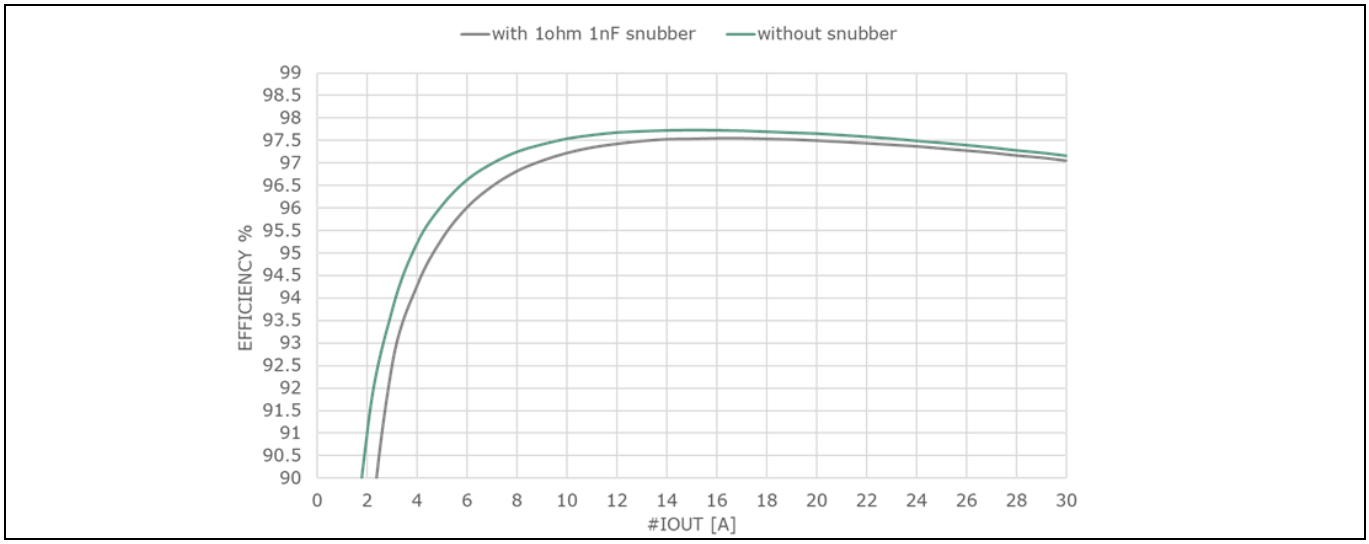


Figure 26 Efficiency slightly drops using the RC snubber

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Glossary

BST
Bootstrap pin

EMI
Electromagnetic interference

FET
Field effect transistor

GND
ground Pin

HS
High side

LS
Low side.

MMCX
Micro-miniature coaxial connectors

PWM
Pulse width modulation
The controller signals generation

SMA
SubMiniature version A Connecter

SSO8
SuperSO 8 package

TDI
Truly differential inputs

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1.00	2024-03-25	Initial release

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