Description

The 9FGV1004C/9FGV1008C are members of Renesas' PhiClock™ programmable clock generator family. The 9FGV1004 provides 1 copy each of 2 integer-related frequencies, 2 copies of a fractional or spread-spectrum frequency. The 9FGV1008 provided 1 integer frequency and 1 copy of a fractional or spread-spectrum frequency. Four user-defined configurations may be selected via two hardware select pins or two I^2C bits, allowing easy software selection of the desired configuration. Any one of the four OTP configurations may be specified as the default when operating in I^2C mode. Four unique I^2C addresses are available, allowing easy I^2C access to multiple components.

Typical Applications

- High-performance Computing (HPC)
- eSSDs
- 10G/25G/100G Ethernet
- Fiber Optic Modules
- Data Center Accelerators

Output Features

- 9FGV1004: 4 programmable output pairs plus 2 LVCMOS REF outputs
- 9FGV1008 2 programmable output pairs plus 1 LVCMOS REF output
- 2 integer and 1 fractional/spread spectrum output frequency per configuration
- 1MHz–325MHz LVDS or LP-HCSL outputs
- 1MHz–200MHz LVCMOS outputs
- 1MHz–156.25MHz spread spectrum or fractional output

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference without spread spectrum (SRnS)
- See AN1001 for Independent Reference with spread-spectrum (SRIS) applications

Features

- 1.8V, 2.5V or 3.3V power supplies
- Individual V_{DDO} for each programmable output pair
- Supports HCSL, LVDS and LVCMOS I/O standards
- Low-Power HCSL technology for improved performance, lower power and higher integration:
  - Programmable output impedance of 85Ω or 100Ω
- Supports LVPECL and CML logic with easy AC coupling – see AN-891 for alternate terminations
- On-board OTP supports up to 4 complete configurations selectable via strapping pins or I^2C
- Internal crystal load capacitors
- Programmable spread-spectrum modulation frequency and amount
- < 150mW at 1.8V with LP-HCSL outputs at 100MHz (9FGV1004)
- < 135mW at 1.8V with LP-HCSL outputs at 100MHz (9FGV1008)
- 4 programmable I^2C addresses: D0, D2, D4, D6
- Easily configured with Renesas Timing Commander™ software or Web Configurator
- Space saving 4 × 4 mm 24-VFQFPN, 24-LGA (9FGV1004) and 3 × 3 mm 16-LGA (9FGV1008) packages
- Integrated crystal option (9FGV1004CQ, 9FGV1008CQ)

Key Specifications

- 12kHz–20MHz typical phase jitter at156.25M Hz (SSC off or on) 224fs RMS (9FGV1008 OUT1)
- 12kHz–20MHz typical phase jitter at156.25MHz (SSC off or on) 267fs RMS (9FGV1004 OUT3)
- PCIe Gen1–4 compliant (spread spectrum off)
- PCIe Gen1–3 compliant (spread spectrum on)
- See AN1001 for generating PCIe Gen5 clocks from the 9FGV1004C/9FGV1008C

Contents

Block Diagram

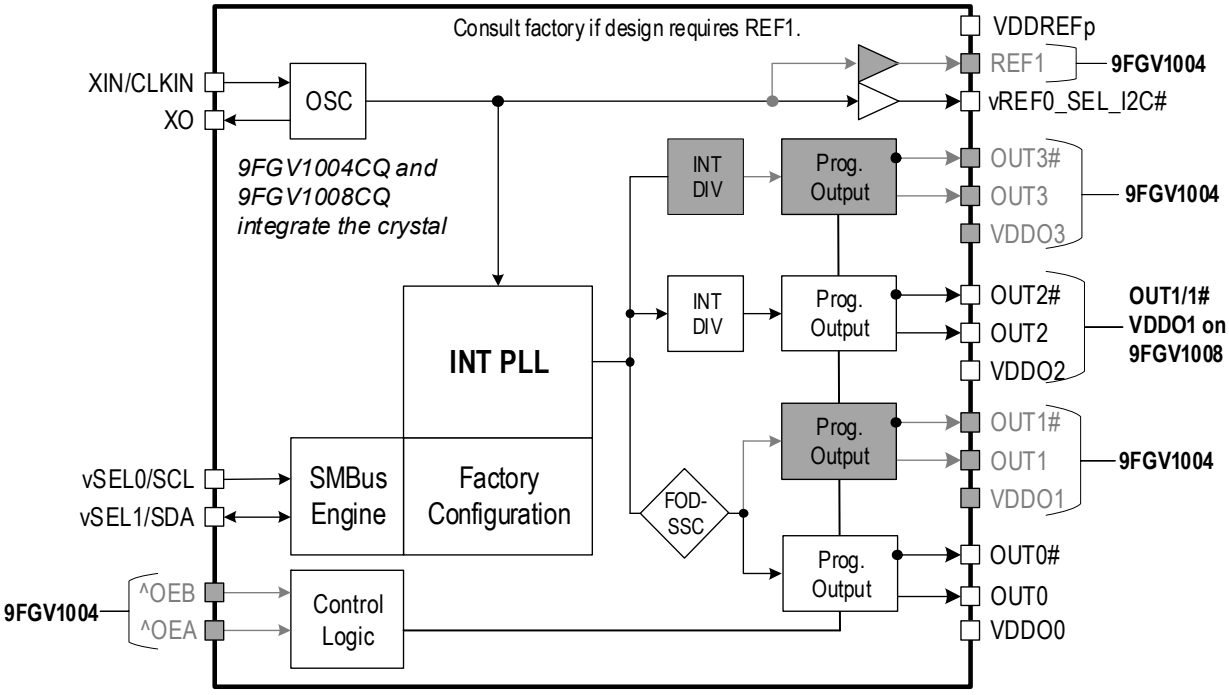
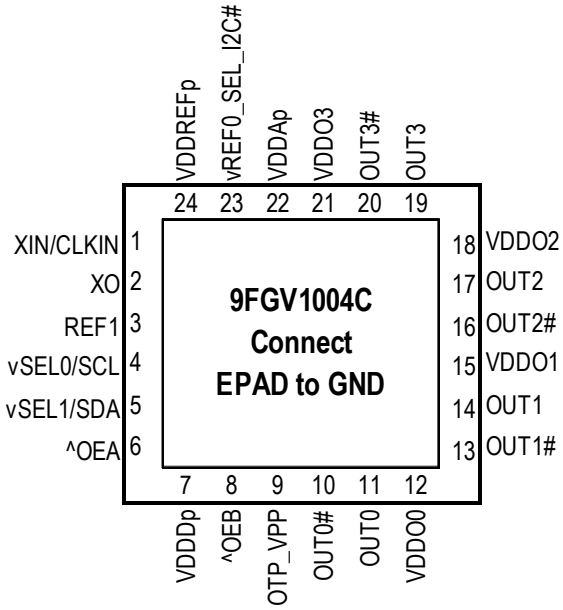


Table 1. OE Mapping

OE[B:A]	OUT0	OUT1	OUT2	OUT3	REF0	REF1
00	Running	Stopped	Running	Stopped	Running	Running
01	Running	Running	Stopped	Stopped	Running	Running
10	Stopped	Stopped	Running	Running	Running	Running
11	Running	Running	Running	Running	Running	Running

Pin Assignments

Figure 1. Pin Assignments for 4 x 4 mm 24-VFQFPN Package – Top View



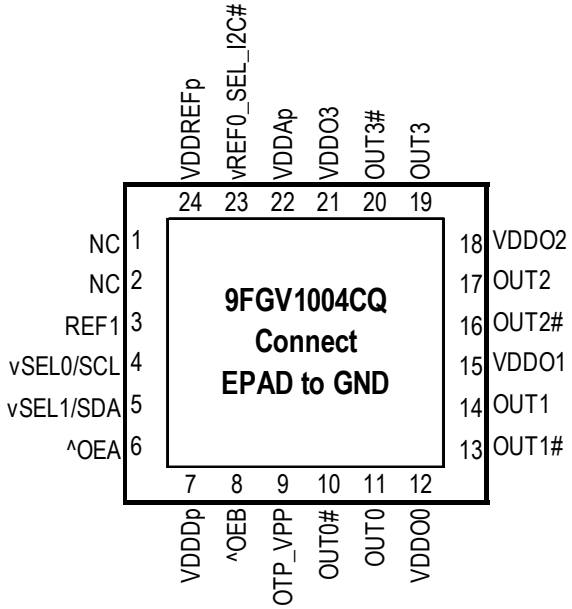
4 × 4 mm 24-VFQFPN, 0.5mm pitch

^ prefix indicates internal pull-up

v prefix indicates internal pull-down resistor

Note: The order of OUT3 is reversed from OUT[0:2]

Figure 2. Pin Assignments for 4 x 4 mm 24-LGA Package – Top View



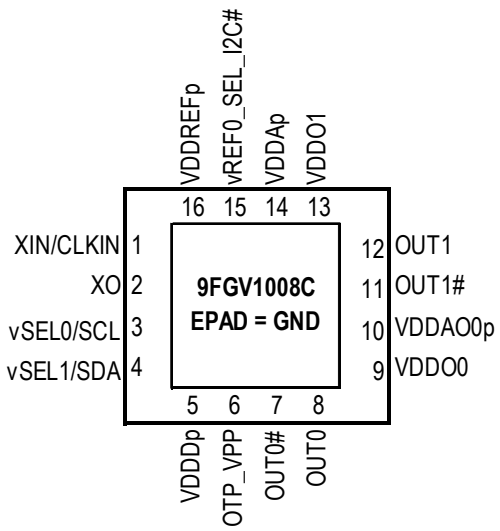
4 × 4 mm 24-LGA, 0.5mm pitch

^ prefix indicates internal pull-up resistor

v prefix indicates internal pull-down resistor

Note: The order of OUT3 is reversed from OUT[0:2]

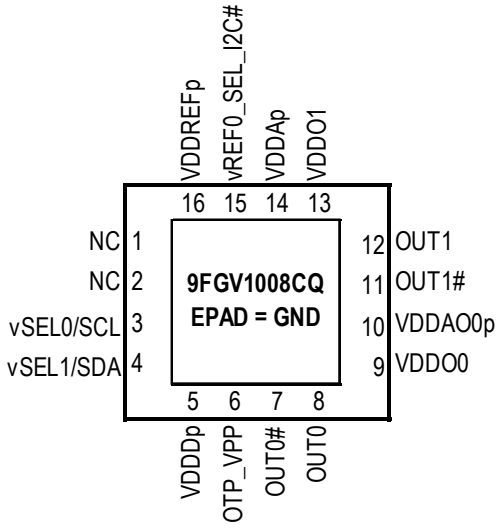
Figure 3. Pin Assignments for 3 x 3 mm 16-LGA Package – Top View



3 x 3 mm 16-LGA , 0.5mm pitch

^ prefix indicates internal pull-up

v prefix indicates internal pull-down



3 x 3 mm 16-LGA , 0.5mm pitch

^ prefix indicates internal pull-up

v prefix indicates internal pull-down

Pin Descriptions

Table 2. 9FGV1004 Pin Descriptions

Number	Name	Type	Description
1[a]	XIN/CLKIN	Input	Crystal input or reference clock input.
2[a]	XO	Output	Crystal output.
3	REF1	Output	LVCMOS reference output.
4	vSEL0/SCL	Input	Select pin for internal frequency configurations/I^2C clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
5	vSEL1/SDA	I/O	Select pin for internal frequency configurations/I^2C data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
6	^OEA	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
7	VDDDp	Power	Digital power. Connect to 1.8V, 2.5V or 3.3V.
8	^OEB	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
9	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as V_{DDD}.
10	OUT0#	Output	Complementary output clock 0.
11	OUT0	Output	Output clock 0.
12	VDDO0	Power	Power supply for output 0.
13	OUT1#	Output	Complementary output clock 1.
14	OUT1	Output	Output clock 1.
15	VDDO1	Power	Power supply for output 1.
16	OUT2#	Output	Complementary output clock 2.
17	OUT2	Output	Output clock 2.
18	VDDO2	Power	Power supply for output 2.
19	OUT3	Output	Output clock 3.
20	OUT3#	Output	Complementary output clock 3.
21	VDDO3	Power	Power supply for output 3.
22	VDDAp	Power	Analog power. Connect to same voltage as VDDDp, with proper filtering.
23	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I^2C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.
24	VDDREFp	Power	Power supply for REF0 and REF1 and the internal XO. Programmable to 1.8V, 2.5V or 3.3V.
25	EPAD	GND	Connect to ground.

Note: Unused outputs can be programmed off and left floating. V_{DDREF} and V_{DDO0} have to be connected.

[a] These pins are 'No Connect' on 9FGV100xQ integrated quartz versions and should have no stubs.

Table 3. 9FGV1008 Pin Descriptions

Number	Name	Type	Description
1[a]	XIN/CLKIN	Input	Crystal input or reference clock input.
2[a]	XO	Output	Crystal output.
3	vSEL0/SCL	Input	Select pin for internal frequency configurations/I^2C clock pin. Function is determined by state of SEL_I2C# upon power up. This pin has an internal pull-down.
4	vSEL1/SDA	I/O	Select pin for internal frequency configurations/I^2C data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
5	VDDDp	Power	Digital power. Connect to 1.8V, 2.5V or 3.3V.
6	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as VDDD.
7	OUT0#	Output	Complementary output clock 0.
8	OUT0	Output	Output clock 0.
9	VDDO0	Power	Power supply for output 0.
10	VDDAO0p	Power	Analog power supply for output 0. This pin should be connected to the same power rail as output 0 and filtered appropriately. Nominal voltages are 1.8V, 2.5V or 3.3V.
11	OUT1#	Output	Complementary output clock 1.
12	OUT1	Output	Output clock 1.
13	VDDO1	Power	Power supply for output 1.
14	VDDAp	Power	Analog power. Connect to same voltage as VDDDp, with proper filtering.
15	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS Output. At power-up, the state of this pin is latched to select the state of the I^2C pins. After power-up, the pin acts as a LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.
16	VDDREFp	Power	Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V.
17	EPAD	GND	Connect to ground.

Note: Unused outputs can be programmed off and left floating. V_{DDREF} and V_{DDO0} have to be connected.

[a] These pins are 'No Connect' on 9FGV100xQ integrated quartz versions and should have no stubs.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGV1004C/9FGV1008C at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.9V
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C
Inputs	
XIN/CLKIN	0V to 1.2V voltage swing
Other Inputs	-0.5V to V_{DDD}
Outputs	
Outputs, V_{DDO} (LVCMOS)	-0.5V to V_{DDO} + 0.5V
Outputs, IO (SDA)	10mA

Thermal Characteristics

Table 5. Thermal Characteristics–24-pin Devices

Parameter	Symbol	Conditions	Package	Typical Values	Unit	Notes
Thermal Resistance (devices with external crystal)	θ_{JC}	Junction to case	NBG24	52	°C/W	1
	θ_{Jb}	Junction to base		2.3	°C/W	1
	θ_{JA0}	Junction to air, still air		44	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow		37	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow		33	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow		32	°C/W	1
Thermal Resistance Q-series (devices with internal crystal)	θ_{JC}	Junction to case	LTG24	57.3	°C/W	1
	θ_{Jb}	Junction to base		24.3	°C/W	1
	θ_{JA0}	Junction to air, still air		79.8	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow		73.9	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow		69.9	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow		67.3	°C/W	1

[1] EPAD soldered to board.

Table 6. Thermal Characteristics–16-pin Devices

Parameter	Symbol	Conditions	Package	Typical Values	Unit	Notes
Thermal Resistance (devices with external crystal)	θ_{JC}	Junction to case	LTG16	66	°C/W	1
	θ_{Jb}	Junction to base		5.1	°C/W	1
	θ_{JA0}	Junction to air, still air		63	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow		56	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow		51	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow		49	°C/W	1
Thermal Resistance Q-series (devices with internal crystal)	θ_{JC}	Junction to case	LTG16	82.1	°C/W	1
	θ_{Jb}	Junction to base		42.3	°C/W	1
	θ_{JA0}	Junction to air, still air		93.6	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow		87.1	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow		83.3	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow		66	°C/W	1

[1] EPAD soldered to board.

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DDOx}	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions.	1.71	-	3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply if available.	1.71	-	3.465	V
T_A	Operating temperature, ambient.	-40	-	85	°C
C_L	Maximum load capacitance (3.3V LVCMOS only).	-	-	15	pF
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic).	0.05	-	5	ms

Electrical Characteristics

V_{DDx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Table 8. Common Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Input Frequency	f_{IN}	Crystal input frequency.	8	-	50	MHz	1
		CLKIN input frequency.	1	-	240	MHz	5
Output Frequency (OUT[3:0])	f_{OUT}	Differential clock output (LVDS/LP-HCSL).	1	-	325	MHz	-
		Single-ended clock output (LVCMOS).	1	-	200	MHz	-
Output Frequency (OUT[1:0])		Spread spectrum or fractional configuration.	1	-	156.25	MHz	6
VCO Frequency	f_{VCO}	VCO operating frequency range.	2400	2500	2600	MHz	-
Loop Bandwidth	f_{BW}	Input frequency = 25MHz.	0.06	-	0.9	MHz	-
Input High Voltage	V_{IH}	SEL[1:0].	0.7 x V_{DDD}	-	V_{DDD} + 0.3	V	-
Input Low Voltage	V_{IL}	SEL[1:0].	GND - 0.3	-	0.8	V	-
Input High Voltage	V_{IH}	REF/SEL_I2C#.	0.65 x V_{DDREF}	-	V_{DDREF} + 0.3	V	-
Input Low Voltage	V_{IL}	REF/SEL_I2C#.	-0.3	-	0.4	V	-
Input High Voltage	V_{IH}	XIN/CLKIN.	0.8	-	1.2	V	-
Input Low Voltage	V_{IL}	XIN/CLKIN.	-0.3	-	0.4	V	-
Input Rise/Fall Time	T_R/T_F	OEA, OEB (24-pin device only)	-	-	10	ns	-
		SEL1/SDA, SEL0/SCL.	-	-	300	ns	-
Input Capacitance	C_{IN}	SEL[1:0].	-	3	7	pF	-
Internal Pull-up Resistor	R_{UP}	-	200	237	300	kΩ	-
Internal Pull-down Resistor	R_{DOWN}	-	200	237	300	kΩ	-
Programmable capacitance at XIN and XO (XIN in parallel with XO)	C_L	XIN/CLKIN, XO.	0	-	8	pF	-
Input Duty Cycle	t2	CLKIN, measured at V_{DDREF}/2.	40	50	60	%	-
Output Duty Cycle	t3	LVCMOS, f_{OUT} > 156.25MHz.	40	50	60	%	-
		LVCMOS, $f_{OUT} \leq$ 156.25MHz.	45	50	55	%	-
		LVDS, LP-HCSL outputs.	45	50	55	%	-

Table 8. Common Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Clock Jitter (9FGV1004)	t6	Cycle-to-cycle jitter (Peak-to-Peak), See "Test Frequencies for Jitter Measurements" for configurations.	-	27	-	ps	4
		Reference clock RMS phase jitter (12kHz to 5MHz integration range). See "Test Frequencies for Jitter Measurements" for configurations.	-	250	-	fs rms	4
		OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See "Test Frequencies for Jitter Measurements" for configurations.	-	267	-	fs rms	4
Clock Jitter (9FGV1008)	t6	Cycle-to-cycle jitter (Peak-to-Peak), See "Test Frequencies for Jitter Measurements" for configurations.	-	27	-	ps	4
		Reference clock RMS phase jitter (12kHz to 5MHz integration range). See "Test Frequencies for Jitter Measurements" for configurations.	-	317	-	fs rms	4
		OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See "Test Frequencies for Jitter Measurements" for configurations.	-	224	-	fs rms	4
Output Skew (9FGV1004)	t7	Skew between the same frequencies, with outputs using the same driver format.	-	34	-	ps	7
Lock Time	t8a	PLL outputs valid from VDDs reaching 1.5V.	-	5	10	ms	2,3
	t8b	REF outputs valid from VDDs reaching 1.5V.	-	5	11	ms	2,3

[1] Practical lower frequency is determined by loop filter settings.

[2] Includes loading the configuration bits from OTP to registers when the configuration number is changed.

[3] Actual PLL lock time depends on the loop configuration.

[4] Actual jitter is configuration dependent. These values are representative of what the device can achieve.

[5] Input doubler off. Maximum input frequency with input doubler on is 160MHz.

[6] With internal low pass filter enabled. When disabled, maximum frequency is 325MHz.

[7] 9FGV1004 OUT0 and OUT1.

Table 9. Test Frequencies for Jitter Measurements

Device	XIN/CLKIN	OUT0	OUT1	OUT2	OUT3	Unit	Notes
9FGV1004 9FGV1004Q5	50	100		125.00	156.25	MHZ	1,2,3
Device	**XIN/CLKIN**	**OUT0**		**OUT1**		**Unit**	**Notes**
9FGV1008 9FGV1008Q5	50	100		156.25		MHZ	1,2,3

[1] All outputs measured with 100MHz outputs both spreading and non-spreading.

[2] Outputs configured as LP-HCSL or LVDS with REF output off unless noted.

[3] This configuration used for 12kHz–20MHz OUT phase jitter measurement. REF off, SSC off.

Table 10. LVCMOS Output Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Slew Rate	S_R	3.3V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	2.6	3.7	4.7	V/ns	-
		2.5V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	1.5	2.4	4.7	V/ns	-
		1.8V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	1.0	1.7	3.2	V/ns	-
Output High Voltage	V_{OH}	I_{OH} = -15mA at 3.3V. I_{OH} = -12mA at 2.5V. I_{OH} = -8mA at 1.8V.	0.8 x V_{DDO}	-	V_{DDO}	V	-
Output Low Voltage	V_{OL}	I_{OL} = 15mA at 3.3V. I_{OL} = 12mA at 2.5V. I_{OL} = 8mA at 1.8V.	-	0.22	0.4	V	-
Output Leakage Current	I_{OZDD}	Outputs tri-stated, V_{DDO}, V_{DDREF} = 3.465V.	-	0	5	µA	-
CMOS Output Driver Impedance	R_{OUT}	T_A = 25°C.	-	17		Ω	-

Table 11. LVDS Output Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Differential Output Voltage for the TRUE Binary State	V_{OT} (+)	247	328	454	mV	-
Differential Output Voltage for the FALSE Binary State	V_{OT} (-)	-454	-332	-247	mV	-
Change in V_{OT} between Complementary Output States	ΔV_{OT}			50	mV	-
Output Common Mode Voltage (Offset Voltage) at 3.3V +5% and 2.5V +5%	V_{OS}	1.125	1.19	1.55	V	-
Output Common Mode Voltage (Offset Voltage) at 1.8V +5%	V_{OS}	0.8	0.86	0.95	V	-
Change in V_{OS} between Complementary Output States	ΔV_{OS}		0	50	mV	-
Outputs Short Circuit Current, V_{OUT}+ or V_{OUT}- = 0V or V_{DD}	I_{OS}		6	12	mA	-
Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT}-	I_{OSD}		3	12	mA	-

Table 11. LVDS Output Electrical Characteristics (Cont.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Rise Times Tested at 20% – 80%	T_R	-	257	375	ps	-
Fall Times Tested at 80% – 20%	T_F	-	287	375	ps	-

Table 12. Low-Power (LP) Push-Pull HCSL Differential Outputs

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Slew Rate	$T_{R/F}$	Scope averaging on.	1	2.5	4	V/ns	2,3,16
Slew Rate Matching	$\Delta T_{R/F}$		-	9	20	%	1,14,16
Crossing Voltage (abs)	V_{CROSS}	Scope averaging off.	250	424	550	mV	1,4,5,16
Crossing Voltage (var)	ΔV_{CROSS}	Scope averaging off.	-	16	140	mV	1,4,9,16
Average Clock Period Accuracy	T_{PERIOD_AVG}	Outputs set to 100MHz for PCIe applications.	-100	0	+2600	ppm	2,10,12,13
Absolute Period	T_{PERIOD_ABS}	Includes jitter and spread modulation.	9.949	10	10.101	ns	2,6
Absolute Maximum Voltage	V_{MAX}	Includes 300mV of overshoot (Vovs).	660	808	1150	mV	1,7,15
Absolute Minimum Voltage	V_{MIN}	Includes -300mV of undershoot (Vuds).	-300	-54	150	mV	1,8,15

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defines as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative ppm tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[10] Refer to Section 8.6 of the PCI Express Base Specification, Revision 4.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single-ended probes must be used for measurements requiring single-ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load C_L = 2pF.

[12] PCIe Gen1 through Gen4 specify ±300ppm frequency tolerances. The PhiClock devices already meet the tighter ±100ppm frequency tolerances proposed for PCIe Gen5 and required by most servers.

[13] “ppm” refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of 100Hz/ppm × 100ppm = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±100ppm applies to systems that do not employ Spread Spectrum Clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock Architectures. Separate Reference Clock Architectures may have a lower allowed spread percentage.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of REFCLK+ should be compared to the fall edge rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default amplitude settings.

[16] Guaranteed by design and characterization.

Table 13. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Unit	Notes
PCIe Phase Jitter	$t_{jphPCIeG1-CC}$	PCIe Gen1.	-	24	43	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz).	-	0.7	1.4	3	ps (rms)	1,2
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz).	-	1.8	2.6	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz).	-	0.44	0.65	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (SSC off) (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz).	-	0.30	0.44	0.5	ps (rms)	1,2,6,7

Table 14. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Unit	Notes
PCIe Phase Jitter	$t_{jphPCIeG2-SRnS}$	PCIe Gen2 (-0.5% SSC) (PLL BW of 16MHz, CDR = 5MHz).	-	1.2	1.53	2	ps (rms)	1,2,4,5
	$t_{jphPCIeG3-SRnS}$	PCIe Gen3 (SSC off) (PLL BW of 2–4MHz, CDR = 10MHz).	-	0.37	0.45	0.7	ps (rms)	1,2,4, 5,6

Notes for all PCIe Filtered Phase Jitter tables:

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Based on PCIe Base Specification Rev4.0 version 1.0. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures.

[5] According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted *industry* limits using widely accepted *industry* filters are used to populate this table. The PCIe Base Specification Rev5.0 is expected to resolve this.

[6] For improved PCIe performance, including PCIe Gen5, see application note AN1001.

[7] SSC off.

Table 15. Current Consumption–9FGV1004

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
V_{DDREF} Supply Current	I_{DDREF}	50MHz REFCLK, subtract 3mA for 25MHz REFCLK.	-	7	11	mA	
Core Supply Current	I_{DDCORE}	2500MHz VCO, 50MHz REFCLK.	-	30	42	mA	3
Output Buffer Supply Current (VDDO3)	I_{DDOx}	LVDS, 325MHz	-	18	24	mA	2
		LP-HCSL, 100MHz	-	12	21	mA	2
		LVCMOS, 50MHz	-	14	19	mA	1,2
		LVCMOS, 200MHz	-	21	35	mA	1,2
Output Buffer Supply Current (VDDO2)		LVDS, 325MHz	-	18	24	mA	2
		LP-HCSL, 100MHz	-	16	21	mA	2
		LVCMOS, 50MHz	-	14	19	mA	1,2
		LVCMOS, 200MHz	-	21	35	mA	1,2
Output Buffer Supply Current (VDDO1)		LVDS, 325MHz, SSC Off	-	8	11	mA	2
		LP-HCSL, 100MHz, SSC Off	-	6	8	mA	2
		LP-HCSL, 100MHz, SSC On	-	14	18	mA	2
		LVCMOS, 50MHz, SSC Off	-	5	7	mA	1,2
		LVCMOS, 50MHz, SSC On	-	9	12	mA	1,2
		LVCMOS, 200MHz, SSC Off	-	13	24	mA	1,2
Output Buffer Supply Current (VDDO0)		LVDS, 325MHz	-	16	21	mA	2
		LP-HCSL, 100MHz	-	15	18	mA	2
		LVCMOS, 50MHz	-	13	17	mA	1,2
		LVCMOS, 200MHz	-	21	34	mA	1,2
Total Power Down Current	I_{DDPD}	Programmable outputs in HCSL mode, B37[0] = 0.	-	20	26	mA	1,2
		Programmable outputs in LVDS mode, B37[0] = 0.	-	31	43	mA	1,2
		Programmable outputs in LVCMOS1 mode, B37[0] = 0.	-	16	20	mA	1,2

[1] Single CMOS driver active for each output pair.

[2] See Test Loads for details.

[3] $I_{DDCORE} = I_{DDA} + I_{DDD}$.

Table 16. Current Consumption–9FGV1008

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
V_{DDREF} Supply Current	I_{DDREF}	50MHz REFCLK.	-	5	7	mA	-
Core Supply Current	I_{DDCORE}	2500MHz VCO, SSC off.	-	32	45	mA	3
		2500MHz VCO, SSC on.	-	39	56	mA	3
Output Buffer Supply Current (VDDO1)	I_{DDOx}	LVDS, 325MHz.	-	18	22	mA	2
		LP-HCSL, 100MHz.	-	16	21	mA	2
		LVCMOS, 50MHz.	-	14	18	mA	1,2
		LVCMOS, 200MHz.	-	22	34	mA	1,2
Output Buffer Supply Current (VDDO0)		LVDS, 325MHz.	-	16	21	mA	2
		LP-HCSL.	-	16	20	mA	2
		LVCMOS, 50MHz.	-	13	18	mA	1,2
		LVCMOS, 200MHz.	-	21	33	mA	1,2
Total Power Down Current	I_{DDPD}	Programmable outputs in HCSL mode, B37[0] = 0.	-	19	25	mA	1,2
		Programmable outputs in LVDS mode, B37[0] = 0.	-	25	35	mA	1,2
		Programmable outputs in LVCMOS1 mode, B37[0] = 0.	-	17	23	mA	1,2

[1] Single CMOS driver active for each output pair.

[2] See Test Loads for details.

[3] $I_{DDCORE} = I_{DDA} + I_{DDD} + I_{DDAO}$.

Table 17. 9FGV1004C/9FGV1008C Spread Spectrum Programmability

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Mod Frequency	$f_{MODPCIe}$	PCIe Compliant -0.5% spread modulation.	30	31.5	33	kHz
Mod Frequency	f_{MOD}	Modulation frequency.	30	-	63	kHz
Spread%	SSC%	Spread amount – down spread.	-0.1	-	-3	%
Spread%	SSC%	Spread amount – center spread.	±0.05	-	±1.5	%

I²C Bus Characteristics

Table 18. I²C Bus DC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input High Level	V_{IH}	-	0.7 x V_{DDD}	-	-	V
Input Low Level	V_{IL}	-	-	-	0.3 x V_{DDD}	V
Hysteresis of Inputs	V_{HYS}	-	0.05 x V_{DDD}	-	-	V
Input Leakage Current	I_{IN}	-	-1	-	30	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA.	-	-	0.4	V

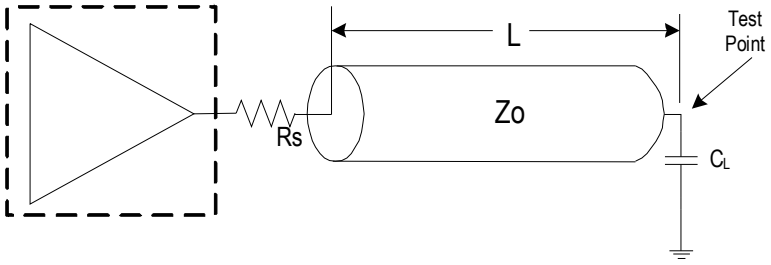
Table 19. I²C Bus AC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Serial Clock Frequency (SCL)	F_{SCLK}	-	10	-	400	kHz
Bus free time between STOP and START	t_{BUF}	-	1.3	-	-	µs
Setup Time, START	$t_{SU:START}$	-	0.6	-	-	µs
Hold Time, START	$t_{HD:START}$	-	0.6	-	-	µs
Setup Time, Data Input (SDA)	$t_{SU:DATA}$	-	0.1	-	-	µs
Hold Time, Data Input (SDA) [1]	$t_{HD:DATA}$	-	0	-	-	µs
Output Data Valid from Clock	t_{OVD}	-	-	-	0.9	µs
Capacitive Load for Each Bus Line	C_B	-	-	-	400	pF
Rise Time, Data and Clock (SDA, SCL)	t_R	-	20 + 0.1 x C_B	-	300	ns
Fall Time, Data and Clock (SDA, SCL)	t_F	-	20 + 0.1 x C_B	-	300	ns
High Time, Clock (SCL)	t_{HIGH}	-	0.6	-	-	µs
Low Time, Clock (SCL)	t_{LOW}	-	1.3	-	-	µs
Setup Time, STOP	$t_{SU:STOP}$	-	0.6	-	-	µs

[1] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Test Loads

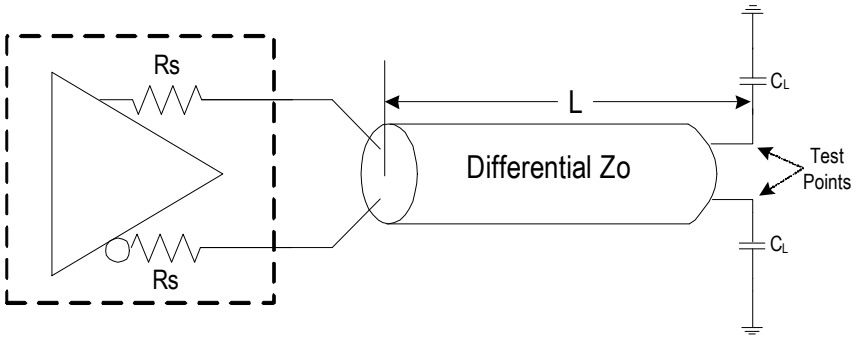
Figure 4. LVCMOS AC/DC Test Load



Rs	Zo	L	C_L
33Ω	50Ω	5 inches	4.7pF

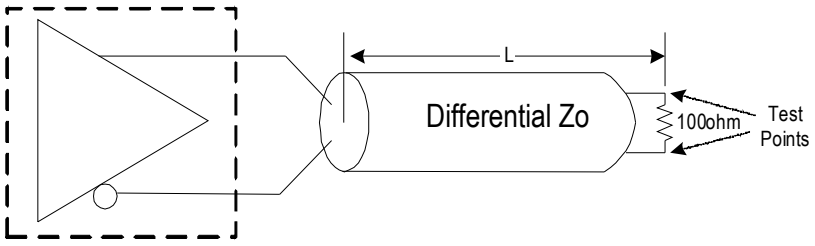
Figure 5. LP-HCSL AC/DC Test Load

(Standard PCIe source-terminated test load)



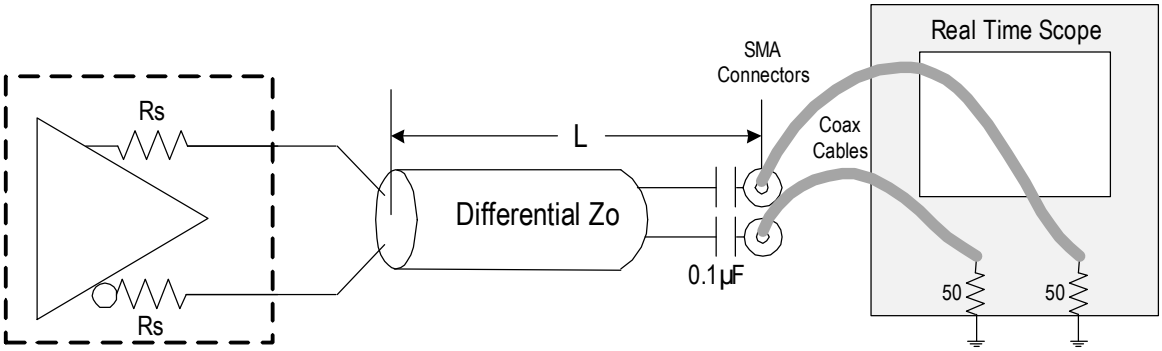
Rs	Zo	L	C_L
Internal	100Ω	5 inches	2pF
Internal	85Ω	5 inches	2pF

Figure 6. LVDS AC/DC Test Load



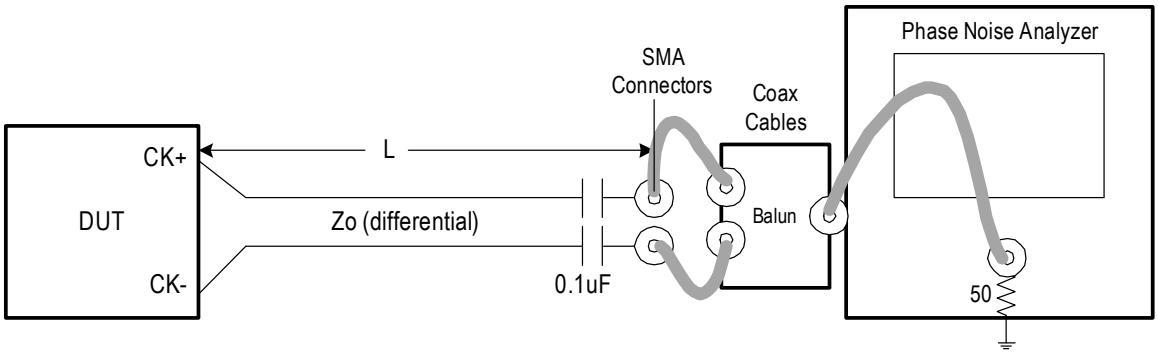
Rs	Zo	L	C_L
N/A	100Ω	5 inches	N/A

Figure 7. Test Setup for PCIe Measurement Using a Real-Time Scope



Rs	Zo	L	C_L
Internal	100Ω	5 inches	N/A

Figure 8. Test Setup for PCIe Measurement Using a Phase Noise Analyzer



Rs	Zo	L	C_L
Internal	100Ω	5 inches	N/A

Crystal Characteristics

Table 20. Recommended Crystal Characteristics

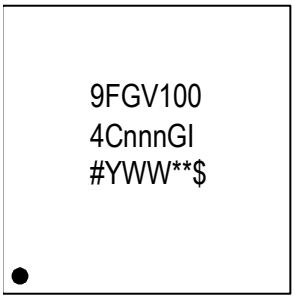
Parameter	Value	Unit
Frequency	8 – 50	MHz
Resonance Mode	Fundamental	-
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, REF at 25°C Over Operating Temperature Range	±20	ppm maximum
Temperature Range (commercial)	0 to +70	°C
Temperature Range (industrial)	-40 to +85	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C_O)	7	pF maximum
Load Capacitance (C_L)	8	pF maximum
Drive Level	0.1	mW maximum
Aging per year	±5	ppm maximum

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

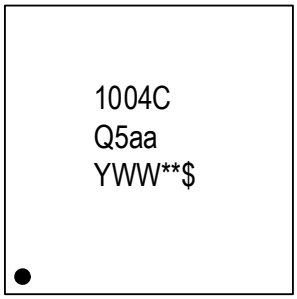
Marking Diagrams

24-VFQFPN



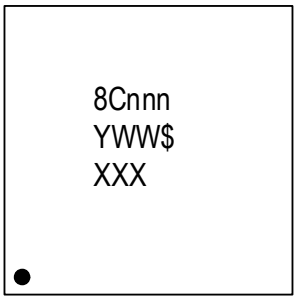
- Lines 1 and 2 are the truncated part number.
- Line 3:
  - “#” denotes the stepping number.
  - “YWW” denotes the last digits of the year and week the part was assembled.
  - “**” denotes the lot sequence.
  - “$” denotes the mark code.

24-LGA (with internal crystal)



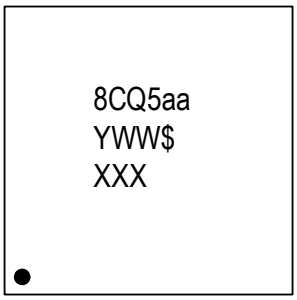
- Lines 1 and 2 are the truncated part number.
- Line 3:
  - “YWW” denotes the last digits of the year and week the part was assembled.
  - “**” denotes the lot sequence.
  - “$” denotes the mark code.

16-LGA



- Line 1 is the truncated part number.
- Line 2:
  - “YWW” denotes the last digits of the year and week the part was assembled.
  - “$” denotes the mark code.
- Line 3:
  - “XXX” denotes the last three characters of the assembly lot number.

16-LGA (with internal crystal)



- Line 1 is the truncated part number.
- Line 2:
  - “YWW” denotes the last digits of the year and week the part was assembled.
  - “$” denotes the mark code.
- Line 3:
  - “XXX” denotes the last three characters of the assembly lot number.

Standard Configurations

Table 21. 9FGV1004C/9FGV1008C Standard Configurations

Supply Voltage–all pins (V)	Output Impedance (ohms)	Number of PCIe Clock Outputs	XTAL Frequency (MHz)	Orderable Part Number (Bulk)	Orderable Part Number (Tape and Reel)
3.3 and 1.8	100 (LP-HCSL)	4	50 – external	9FGV1004C001NBGI	9FGV1004C001NBGI8
			50 – internal	9FGV1004CQ501LTGI	9FGV1004CQ501LTGI8
		2	50 – external	9FGV1008C001LTGI	9FGV1008C001LTGI8
			50 – internal	9FGV1008CQ501LTGI	9FGV1008CQ501LTGI8

Table 22. Common Features of 9FGV1004C/9FGV1008C Standard Configurations

Configuration	9FGV1004 Output	9FGV1008 Output	Output Frequency (MHz)	Supply Voltage (V)	Output Type	Ref Outputs
0	OUT0	OUT0	100	1.8	LP-HCSL	OFF
	OUT1	-	100	1.8	LP-HCSL	
	OUT2	OUT1	125	1.8	LVDS	
	OUT3	-	50	1.8	LP-HCSL	
1	OUT0	OUT0	100	1.8	LP-HCSL	OFF
	OUT1	-	100	1.8	LP-HCSL	
	OUT2	OUT1	156.25	1.8	LVDS	
	OUT3	-	50	1.8	LP-HCSL	
2	OUT0	OUT0	100	3.3	LP-HCSL	OFF
	OUT1	-	100	3.3	LP-HCSL	
	OUT2	OUT1	125	3.3	LVDS	
	OUT3	-	50	3.3	LP-HCSL	
3	OUT0	OUT0	100	3.3	LP-HCSL	OFF
	OUT1	-	100	3.3	LP-HCSL	
	OUT2	OUT1	156.25	3.3	LVDS	
	OUT3	-	50	3.3	LP-HCSL	

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature	Crystal
9FGV1004CnnnNBGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tray	-40 to +85°C	External
9FGV1004CnnnNBGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40 to +85°C	External
9FGV1004CQ5aaLTGI	4 × 4 mm, 0.5mm pitch 24-LGA	Tray	-40 to +85°C	50MHz Internal
9FGV1004CQ5aaLTGI8	4 × 4 mm, 0.5mm pitch 24-LGA	Tape and Reel	-40 to +85°C	50MHz Internal
9FGV1008CnnnLTGI	3 × 3 mm, 0.5mm pitch 16-LGA	Tray	-40 to +85°C	External
9FGV1008CnnnLTGI8	3 × 3 mm, 0.5mm pitch 16-LGA	Tape and Reel	-40 to +85°C	External
9FGV1008CQ5aaLTGI	3 × 3 mm, 0.5mm pitch 16-LGA	Tray	-40 to +85°C	50MHz Internal
9FGV1008CQ5aaLTGI8	3 × 3 mm, 0.5mm pitch 16-LGA	Tape and Reel	-40 to +85°C	50MHz Internal

"G" indicates RoHS 6.6 compliance.

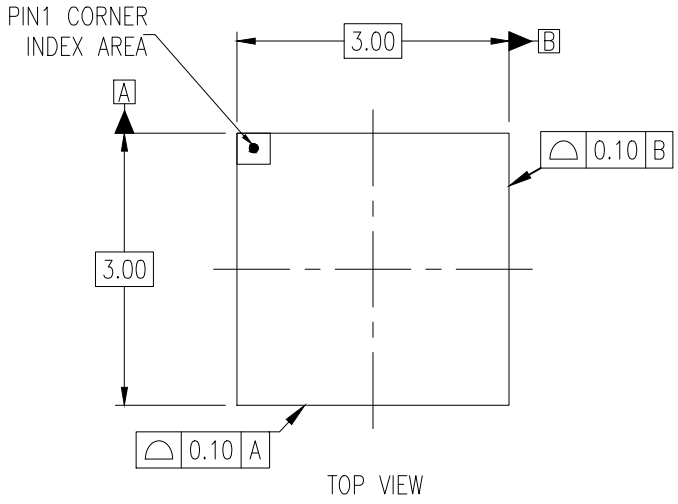
"nnn" are decimal digits indicating a specific configuration.

"aa" are alphanumeric digits indicating a specific configuration.

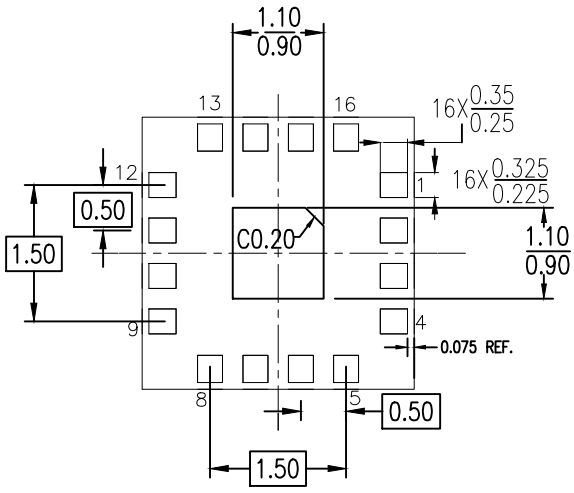
"Q5" indicates internal 50MHz crystal.

Revision History

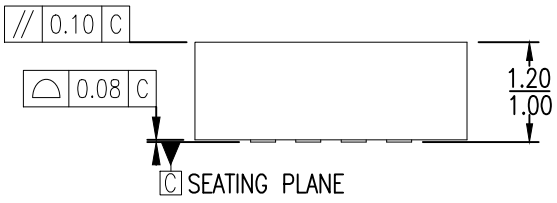
Revision Date	Description of Change
July 18, 2024	Updated the 24-LGA POD link to the LTG24T2 package in Ordering Information.
March 29, 2023	▪ Updated footnote 2 in Table 8. ▪ Moved package outline drawings links to Ordering Information.
January 31, 2023	Updated POD links in Package Outline Drawings.
October 29, 2020	Updated pin descriptions for VDDAp and VDDDp.
October 20, 2020	Added Test Loads section and diagrams.
September 28, 2020	Added Standard Configurations section and tables.
September 22, 2020	Correct all f_{OUT} minimum frequencies from 10MHz to 1MHz in Common Electrical Characteristics table.
August 18, 2020	Updated 9FGV1008CQ (16-LGA with internal crystal) marking diagram.
August 14, 2020	Updated Slew Rate 1.8V minimum value from 0.8 to 1.0V/ns.
August 13, 2020	Updated Carrier Type in Ordering Information table from "Trays" to "Tray".
July 20, 2020	Corrected internal resistors from pull-up to pull-down on SEL0/SCL and SEL1/SDA pins.
April 16, 2020	Initial release.



TOP VIEW

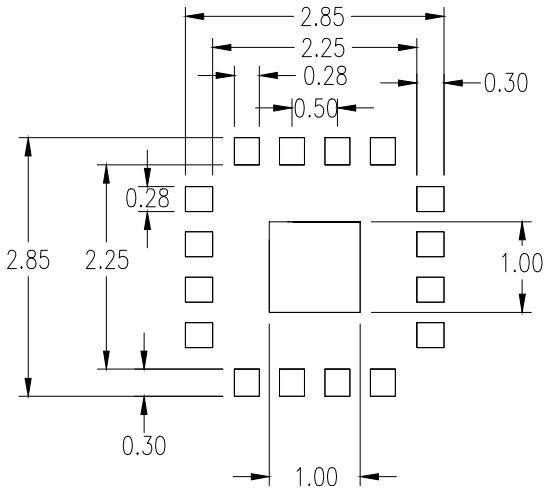


BOTTOM VIEW



SIDE VIEW

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



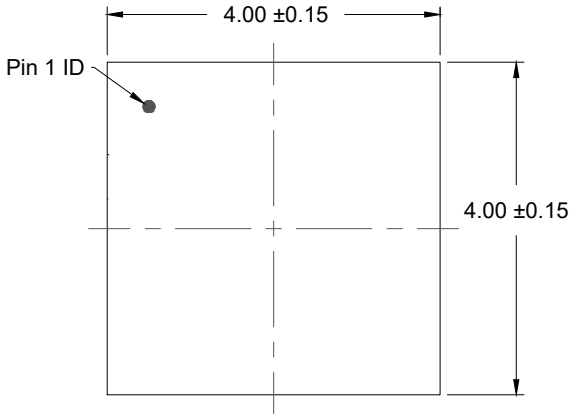
RECOMMENDED LAND PATTERN DIMENSION

NOTES:

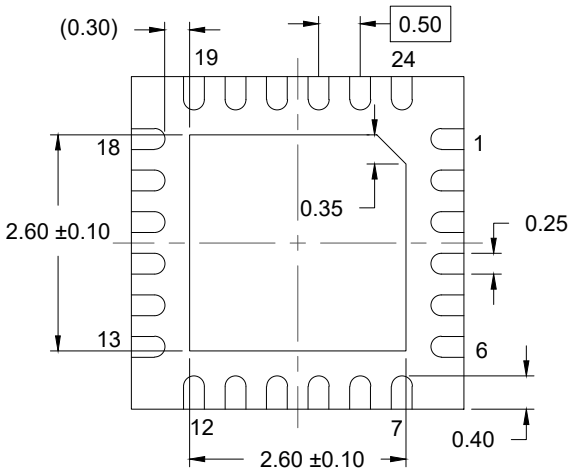
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Outline Drawing

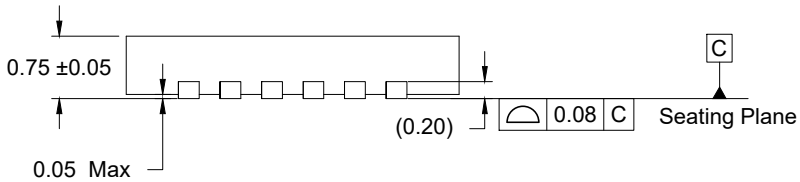
Package Code:NBG24P2
24-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.50 mm Pitch
PSC-4313-02, Revision: 03, Date Created: Jul 20, 2023



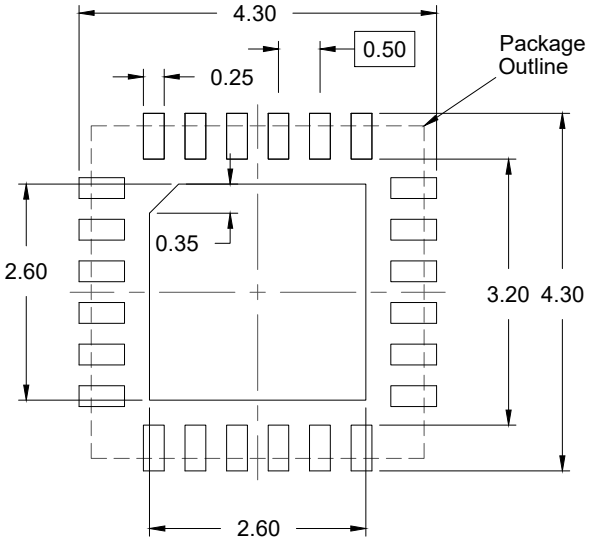
TOP VIEW



BOTTOM VIEW



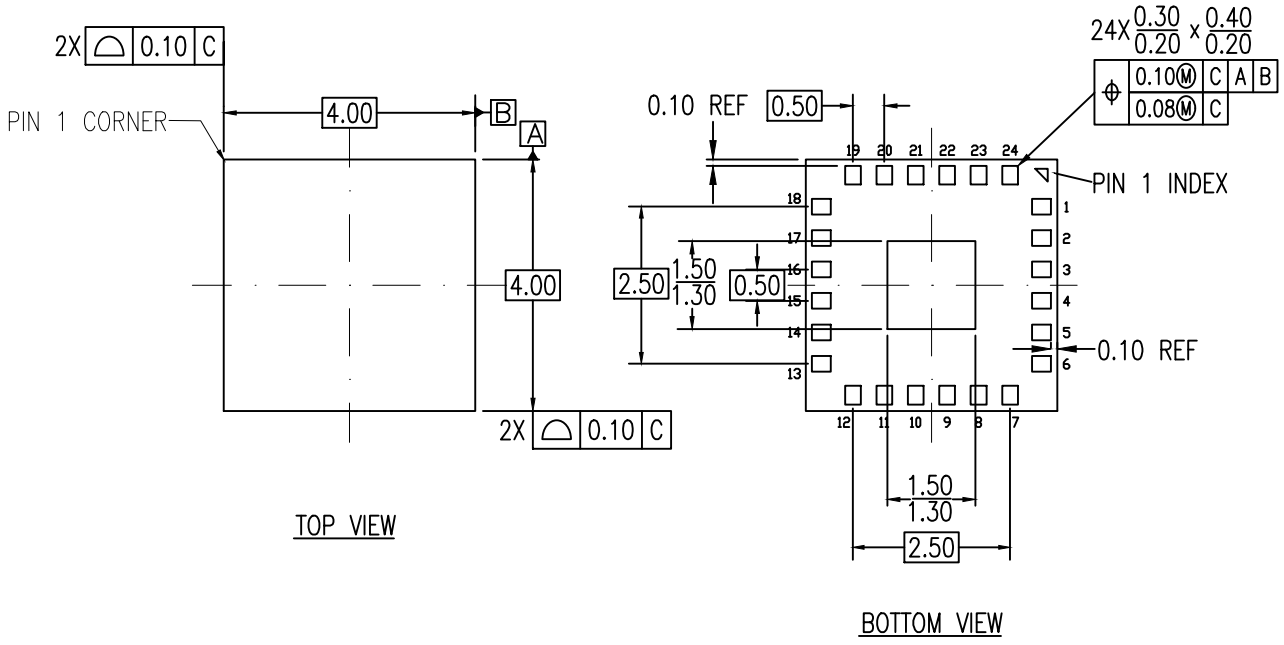
SIDE VIEW

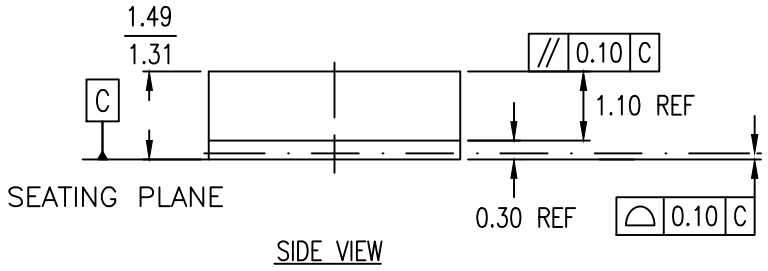


RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

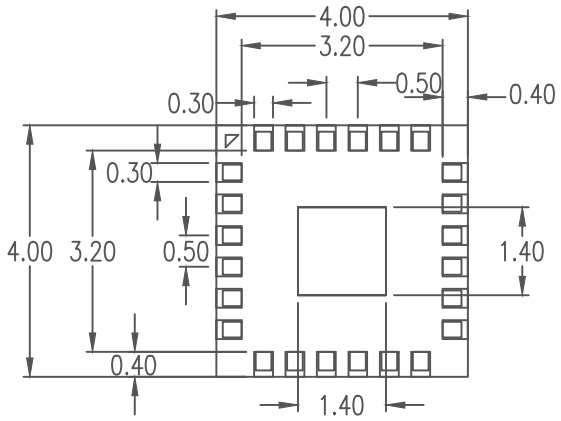
NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.





NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 15, 2017	Rev 00	Initial Release

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