NSi6801

Single-Channel Isolated Gate Driver

Datasheet (EN) 0. 1

Product Overview

The NSi6801 is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. The device can drive IGBTs, power MOSFETs and SiC MOSFETs in many applications such as motor control systems, solar inverters and power supplies. It can source and sink 5A peak current.

The NSi6801 provides 5700Vrms isolation per UL1577 in Strenched-SO6 package. System robustness is supported by 100kV/us minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 35V, and 13-V UVLO (under voltage lock-out). While the input circuit imitates the characters of LEDs, it has performance advantages compared to standard opto isolated gate drivers, including better reliability and aging performance, higher working temperature, shorter propagation delay and smaller pulse width distortion.

As a result, the NSi6801 is suitable to replace opto-isolated driver in high reliability, power density and efficiency switching power system.

Key Features

- Isolated single-channel driver
- Pin compatible, drop in upgrade for opto isolated gate drivers
- Driver side supply voltage: up to 35V with 13V UVLO
- 5A peak source and 5A peak sink output current
- High CMTI: ±100kV/us
- 80ns typical propagation delay
- 35ns maximum pulse width distortion
- 25ns maximum part to part delay matching
- Accepts minimum input pulse width 30ns
- Operation ambient temperature: -40°C ~125°C
- RoHS-compliant packages:
  - SOIC-6 wide body
  - DUB-8

Safety Regulatory Approvals

- UL recognition: 5700Vrms for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

Applications

- Isolated DC/DC and AC/DC power supplies in server, telecom and industry
- High Voltage PFC
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

Functional Block Diagram

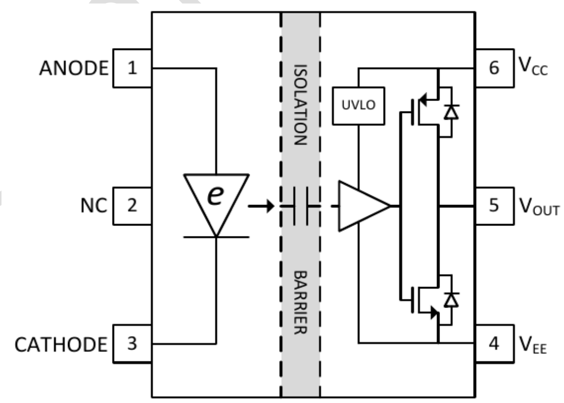


Figure 1. NSi6801 Block Diagram

INDEX

1. Pin Configuration and Functions

NSi6801 Top View

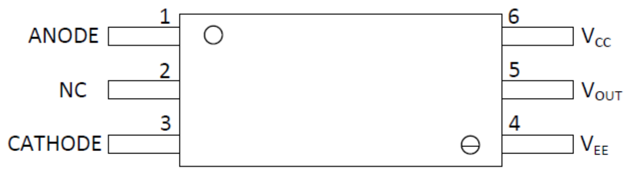


Table 1.1 NSi6601 Pin Configuration and Description

PIN NO.	*SYMBOL*	*FUNCTION*
1	ANODE	Anode of LED emulator
2	NC	No Connection
3	CATHODE	Cathode of LED emulator
4	V_{EE}	Negative output supply rail
5	V_{OUT}	Gate-drive output
6	V_{CC}	Positive output supply rail

2. Absolute Maximum Ratings

2.1. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Average Input Current	I_{F_AVG}		25	mA
Peak Transient Input Current	I_{F_PEAK}		0.2	A
Reverse Input Voltage	V_{R_MAX}		6.5	V
Driver Side Supply Voltage	V_{CC}-V_{EE}	-0.3	35	V
Output Signal Voltage	V_{OUT}	V_{EE}-0.3	V_{CC}+0.3	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C
Electrostatic discharge	V_{ESD_HBM}(1)		±2000	V
	V_{ESD_CDM}(2)		±500	V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

2.2. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(off)}$	-5.5	0.9	V
Driver Side Supply Voltage	V_{CC}- V_{EE}	14	33	V
Ambient Temperature	T_A	-40	125	°C

2.3. DC Electrical Characteristics

(Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_J=-40°C to 150°C, V_{CC}=15V to 30V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= –5V to 0.8V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Driver Side Supply						
High Level Supply Current	I_{CCH}		2	3	mA	I_F=10mA, I_{OUT}=0mA
Low Level Supply Current	I_{CCL}		2	3	mA	V_F=0V, I_{OUT}=0mA
VCC UVLO Rising Threshold	V_{CC_ON}	12.5	13	13.5	V	I_F=10mA
VCC UVLO Falling Threshold	V_{CC_OFF}	11.5	12	12.5	V	
VCC UVLO Hysteresis	V_{CC_HYS}		1		V	
Input Pin Characteristic						
Input Forward Threshold Current Low to High	I_{FLH}	1.5	2.8	4	mA	V_{OUT}>5V, Cg=1nF
Threshold Input Voltage High to Low	V_{FHL}	0.9			V	V_{OUT}<5V, Cg=1nF
Input Forward Voltage	V_F	1.9	2.2	2.5	V	I_F=10mA
Temp Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T$		1	1.35	mV/°C	I_F=10mA
Input Reverse Breakdown Voltage	V_R	6.5			V	I_R=10uA
Input Capacitance	C_{IN}		15		pF	f=0.5MHz
Output Pin Characteristic						
High Level Output Voltage	V_{OH}	V_{CC}-0.36	V_{CC}-0.26		V	I_{OUT}=-100mA, I_F=10mA
			V_{CC}			I_{OUT}=0mA, I_F=10mA
Low Level Output Voltage	V_{OL}		40	60	mV	I_{OUT}=100mA, V_F=0V
High Level Peak Output Current	I_{OH}	3	5		A	V_{CC}=15V, pulse width<10us
Low Level Peak Output Current	I_{OL}	3	5		A	V_{CC}=15V, pulse width<10us

2.4. Switching Electrical Characteristics

(Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_J=-40°C to 150°C, V_{CC}=15V to 30V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= –5V to 0.8V)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Minimum Pulse Width	t_{PWmin}	30	40		ns	C_{LOAD}=1nF, f=20kHz (50% Duty Cycle)
Propagation Delay	t_{pHL}, t_{pLH}		80	105	ns	
Pulse Width Distortion $\|t_{PLH}-t_{PHL}\|$	t_{PWD}			35	ns	
Part to Part Delay Matching [(1)]	t_{DM}			25	ns	
Output Rise Time (20% to 80%)	t_R			28	ns	
Output Fall Time (80% to 20%)	t_F			25	ns	
VCC Power-Up Time Delay	t_{start_VCC}		20		us	V_{CC} rising from 0V to 15V
Common Mode Transient Immunity	CMTI	100			kV/us	

(1) t_{DM} is the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads ensured by characterization.

2.5. Typical Performance characteristics

Figure 2.1 Supply currents versus Temperature

Figure 2.2 Supply current versus Supply Voltage

Figure 2.3 Forward threshold current versus Temperature

Figure 2.4 Forward current versus Forward voltage drop

Figure 2.5 Forward voltage drop versus Temperature

Figure 2.6 V_{OH} (No Load) versus Temperature

Figure 2.9 V_{OH} (20mA Load) versus Temperature

Figure 2.10 V_{OL} versus Temperature

Figure 2.11 Output Drive currents versus Temperature

Figure 2.12 Propagation delay versus Temperature

Figure 2.13 Propagation delay versus Supply voltage

Figure 2.14 Propagation delay versus Forward current

2.6. Parameter Measurement Information

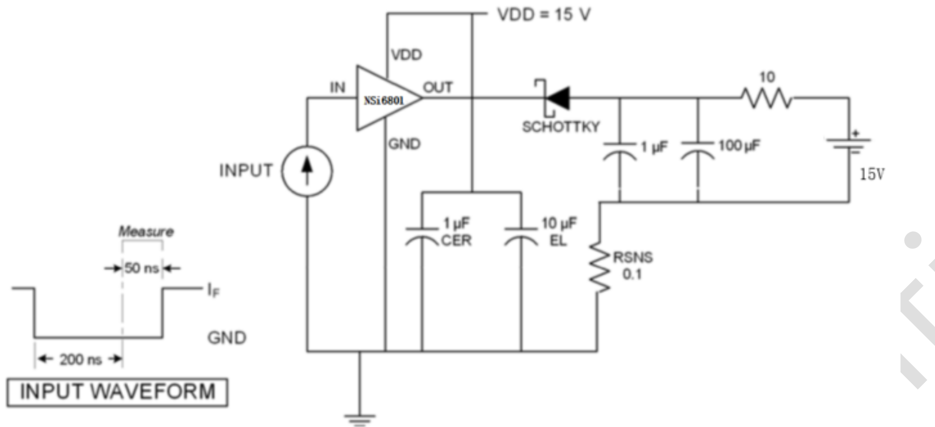


Figure 2.15 I_{OL} Sink Current Test Circuit

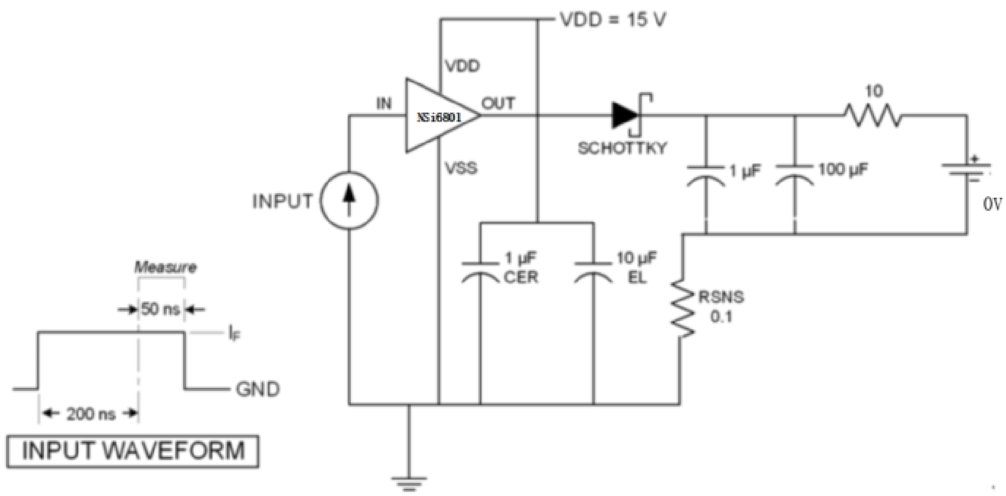


Figure 2.16 I_{OH} Source Current Test Circuit

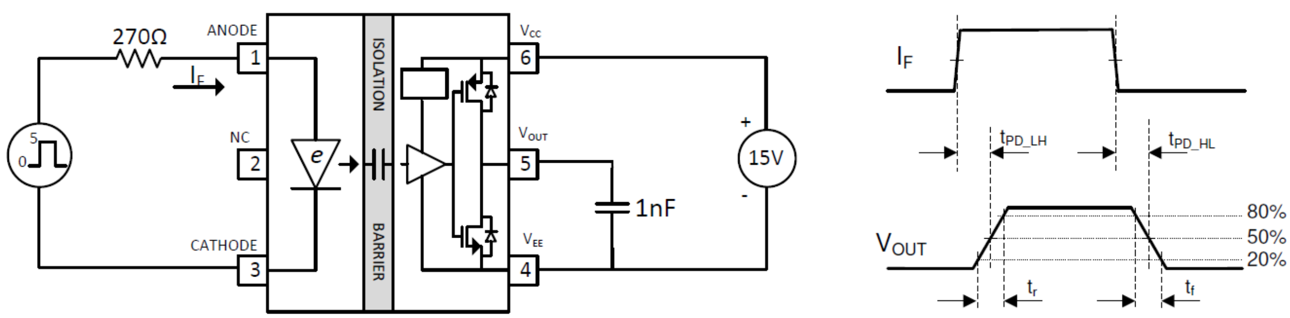


Figure 2.17 I_F to V_{OUT} Propagation Delay, Rise Time and Fall Time

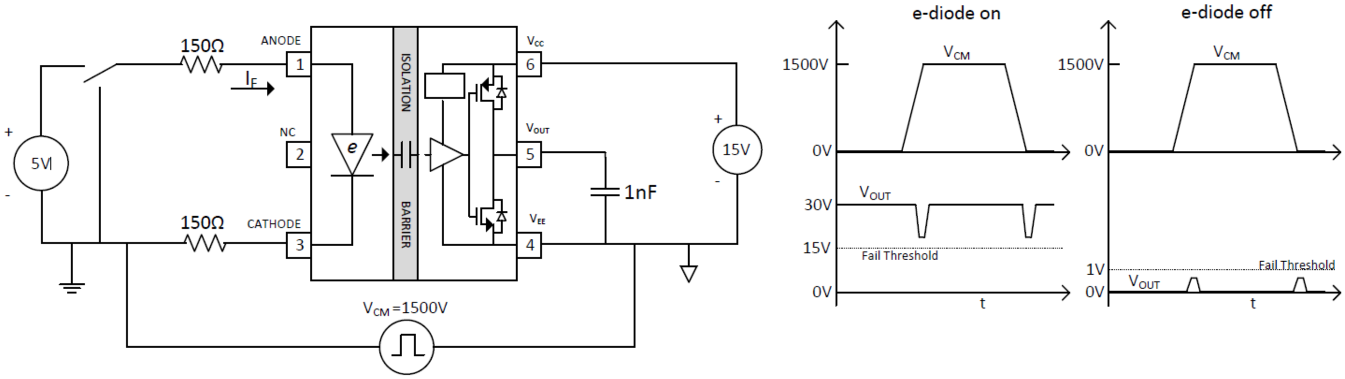


Figure 2.18 Common Mode Transient Immunity Test Circuit

3. High Voltage Feature Description

3.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20	um	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

3.2. DIN VDE V 0884-11: 2017-01 INSULATION CHARATERISTICS

Description	Test Condition	Symbol	Value	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ $600V_{RMS}$			I to IV	
For Rated Mains Voltage ≤ $1000V_{RMS}$			I to III	
Climatic Category			40/125/21	
Pollution Degree			2	
Maximum Working Isolation Voltage		V_{IOWM}	1500	V_{RMS}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{pd(m)}=V_{IORM}\times1.875$, 100% production test, $t_{ini}=t_m=1s$, partial discharge<5pC	$V_{pd(m)}$	3977	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{pd(m)}=V_{IORM}\times1.6$, $t_{ini}=60s$, $t_m=10s$, partial discharge <5pC	$V_{pd(m)}$	3394	V_{PEAK}
After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}=V_{IORM}\times1.2$, $t_{ini}=60s$, $t_m=10s$, partial discharge <5pC	$V_{pd(m)}$	2545	V_{PEAK}
Maximum Transient Isolation Voltage	t = 60 s	V_{IOTM}	8000	V_{PEAK}
Maximum Withstanding Isolation Voltage	$V_{TEST}= V_{ISO}$, t = 60 s (qualification); $V_{TEST}= 1.2 \times V_{ISO}$, t = 1 s (100%production)	V_{ISO}	5700	V_{RMS}

Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=V_{IOSM}×1.6$	V_{IOSM}	8000	V_{PEAK}
Isolation Resistance	V_{IO} =500V at $T_A=T_S$=150°C	R_{IO}	>10^9	Ω
	V_{IO} =500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF

3.3. Safety-Limiting Values

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Maximum input power dissipation	$R_{θJA}$=126°C/W, T_J=150°C, T_A=25°C	P_S		mW
Maximum channel A and B output current	$R_{θJA}$=126°C/W, V_{CC}=15V, T_J=150°C, T_A=25°C	I_S		mA
	$R_{θJA}$=126°C/W, V_{CC}=30V, T_J=150°C, T_A=25°C	I_S		mA
Maximum ambient safety temperature		T_S	150	°C

Figure 3.1 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Figure 3.2 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

3.4. Regulatory Information

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5700V_{RMS} Isolation Voltage	Single Protection, 5700V_{RMS} Isolation voltage	Reinforced Insulation V_{IORM}=2121V_{PEAK}, V_{IOTM}=8000V_{PEAK}, V_{IOSM}=8000V_{PEAK}	Reinforced Insulation
File (pending)	File (pending)	File (pending)	File (pending)

4. Function Description

The NSi6801 is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. The integrated galvanic isolation between control input logic and driving output stage grants additional safety. The device can source and sink 5A peak current, which can drive IGBTs, power MOSFETs and SiC MOSFETs in many applications such as motor control systems, solar inverters and power supplies.

4.1. Functional Block Diagram

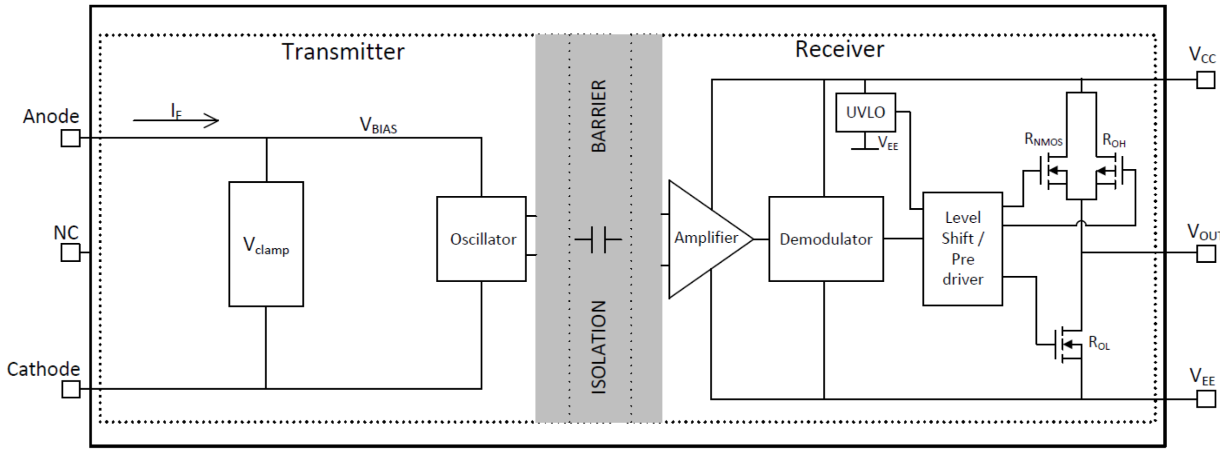


Figure 4.1 NSi6801 Functional Block Diagram

4.2. Truth Tables

Table 4.1 Driver Function Table (1)

e-diode	*V_{CC} status*	*Outputs*
X	Powered Down	L
$I_F>I_{FLH}$	Powered Up	H
$V_F<V_{FHL}$	Powered Up	L

(1) H= Logic High; L= Logic Low; X= Irrelevant

4.3. Output Stage

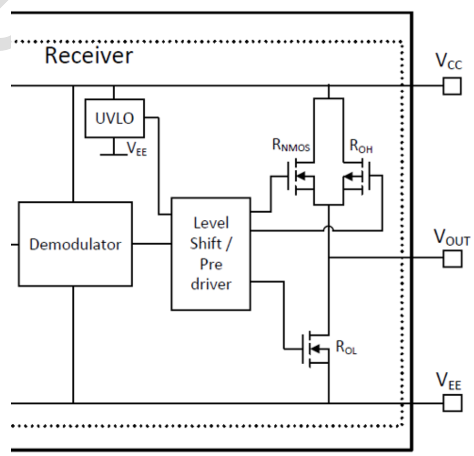


Figure 4.2 NSi6801 Output Stage

Table 4.2 NSi6801 Output Stage On-Resistance

R_{NMOS}	R_{OH}	R_{OL}	Unit
0.8	2.6	0.4	Ω

The NSi6801 has P-channel and N-channel MOSFET in parallel to pull up the OUT+ pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSi6801 N-channel MOSFET turns on to pull up OUT+ more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSi6801. The equivalent pull-up resistance of NSi6801 is the parallel combination ROH || RNMOS. The result is quite small, indicating the strong driving capability of NSi6801.

The pull-down structure of NSi6801 is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSi6801.

4.4. V_{CC} and Under Voltage Lock Out (UVLO)

The recommended driver side supply voltage (V_{CC}) for the NSi6801 device is from 14V to 30V. The lower limit of V_{CC} is determined by the internal UVLO protection feature of the device. V_{CC} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low.

A local bypass capacitor should be placed between the V_{CC} and V_{EE} pins, with a value of 220-nF to 10-µF for device biasing. An additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

4.5. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC} is not connected to the power supply. When V_{CC} is floating, the driver output is held low and clamping V_{OUT} pin to approximately 2V higher than V_{EE}.

4.6. Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the Miller capacitance. The diode between V_{OUT} and V_{CC} pins inside the driver limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

5. Application Note

5.1. Typical Application

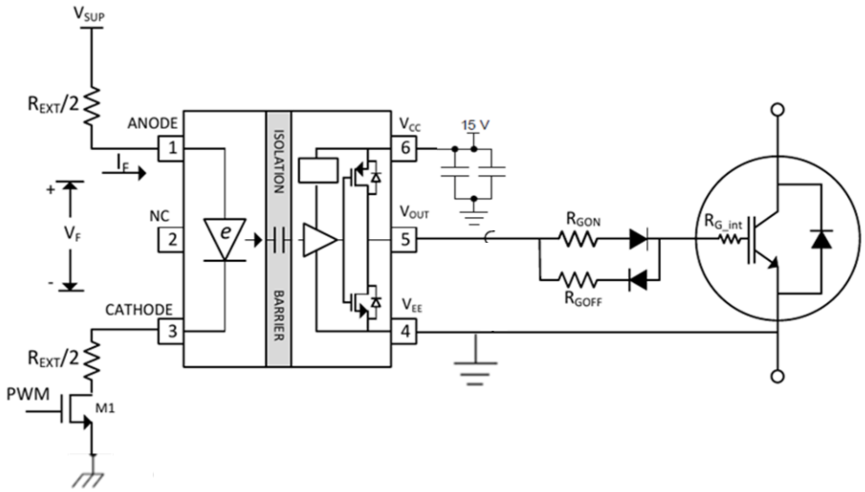


Figure 5.1 NSi6801 typical application circuit with NMOS driving input stage

Bypassing capacitors connecting between V_{CC} and V_{EE} are needed to achieve reliable performance. To filter noise, 0.1µF/50V ceramic capacitor is recommended to place as close as possible to NSi6801. To support high peak currents when turning on external power transistor, additional 10µF/50V ceramic capacitor is recommended. If the V_{CC} power supply is located long distance from the IC, bigger capacitance is needed.

NSi6801 requires 7mA to 16mA bias current that flows into the e-diode for normal operation. The PWM from MCU is not suitable to provide such current directly and external circuit is needed. In Figure 5.1, one NMOS is used with split input resistors. Another input drive method is using one buffer, as shown in Figure 5.2. The details to calculate input drive parameters are in Chapter 5.3.

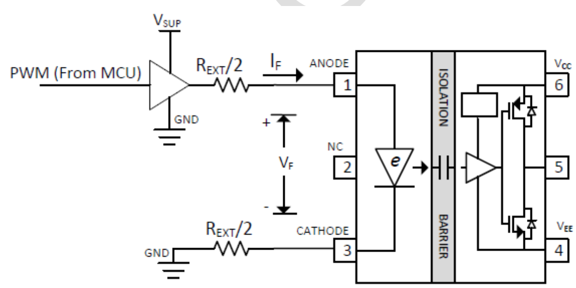


Figure 5.2 NSi6801 typical application circuit with one buffer driving input stage

5.2. Interlock Protection

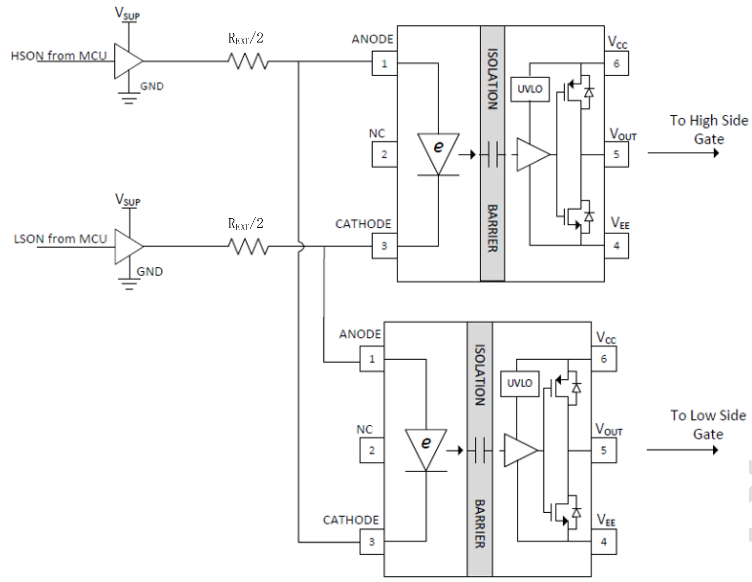


Figure 5.3 Interlock Protection using NSi6801

For applications to drive power transistors in half bridge configuration, two NSi6801 can be used. Interlock protection is possible as shown in Figure 5.3. If the controller has some mistake, leading to negative dead time, the output PWM of NSi6801 is adjusted to avoid power transistor shoot through. The input side reverse breakdown voltage of NSi6801 is greater than 6.5V, which supports interlock protection of 3.3V or 5V PWM signal source.

5.3. Selecting Input Resistor

The recommended forward current range for NSi6801 is 7mA to 16mA. The value of input resistor, buffer supply voltage and buffer internal resistance influence the forward current, as shown in Equation (1). In Figure 5.1, R_{Buffer} is the on-resistance of the external NMOS. In Figure 5.2, R_{Buffer} is the buffer output impedance in output “High” state. In Figure 5.3, R_{Buffer} is the summary of buffer output impedance in “High” and “Low” state.

$$R_{EXT} = \frac{V_{SUP}-V_F}{I_F} - R_{Buffer} \quad (1)$$

The parameter variation needs to be taken into consideration when selecting input resistor. Table 5.1 lists parameter variation in this example. The corresponding external resistor calculation result is 196Ω min, 262Ω typ and 300Ω max.

Table 5.1 External parameters range when calculating input resistor

Parameters	Min	Typ	Max
NSi6801 forward current I_F	7mA	10mA	16mA
NSi6801 forward voltage V_F	1.8V	2.1V	2.4V
Buffer supply voltage V_{SUP}	5V*95%	5V	5V*105%
Buffer internal resistance R_{Buffer}	13Ω	18Ω	22Ω

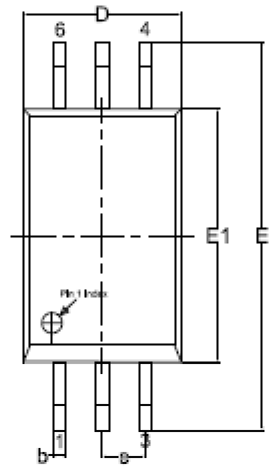
5.4. PCB Layout

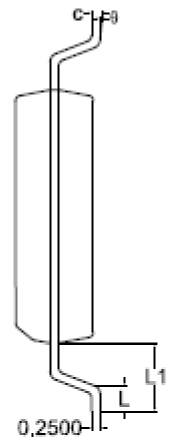
Carful PCB layout is essential for optimal performance. Some key guidelines are:

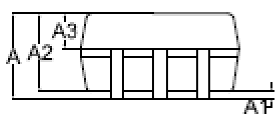
- The bypass capacitors should be placed close to NSi6801, between V_{CC} to V_{EE}.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSi6801 close to power transistor.
- Place large amount of copper connecting to V_{EE} pin and V_{CC} pin for thermal dissipation, with priority on V_{EE} pin. If the system has multi V_{EE} or V_{CC} layers, use multiple vias of adequate size for connection.

- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

6. Package Information







	DIMENSIONS IN MILLIMETERS		
REF.	MIN.	NOM.	MAX.
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
E	11.25	11.50	11.75
E1	7.40	7.50	7.60
D	4.58	4.68	4.78
L	0.50	—	1.00
b	0.28	—	0.51
c	0.25	—	0.29
θ	0°	—	8°
e	1.27 BSC		
L1	2.00 BSC		

SSO6 Package Shape and Dimension

Dimensions shown in millimeters

7. Order Information

Part No.	*Input Type*	*Package*	*PINs*	*Temperature*	*MSL*	*SPQ*
NSi6801C-DSWFR	LED Imitates	SOW	6	-40 to 125°C	Level 2	850
NSi6801C-DDBR	LED Imitates	DUB	8	-40 to 125°C	Level 2	350
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260°C according to the JEDEC industry standard classifications and peak solder temperatures.						

8. Reversion History

Revision	Description	Date
0.1		2019/7/15