2 Ω CMOS, ±5 V/+5 V, SPST Switches

ADG601/ADG602

FEATURES

Low on resistance 2.5 Ω maximum
<0.6 Ω on resistance flatness
Dual ±2.7 V to ±5.5 V or single +2.7 V to +5.5 V supplies
Rail-to-Rail input signal range
Tiny 6-lead SOT-23 and 8-lead MSOP packages
Low power consumption
TTL-/CMOS-compatible inputs

APPLICATIONS

Automatic test equipment
Power routing
Communication systems
Data acquisition systems
Sample-and-hold systems
Avionics
Relay replacement
Battery-powered systems

FUNCTIONAL BLOCK DIAGRAM

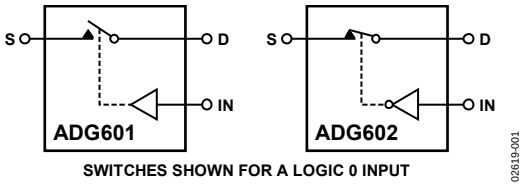

Figure 1.

Table 1. Truth Table

ADG601 In	ADG602 In	Switch Condition
0	1	OFF
1	0	ON

GENERAL DESCRIPTION

The ADG601/ADG602 are monolithic CMOS SPST (single pole, single throw) switches with on resistance typically less than 2.5 Ω. The low on resistance flatness makes the ADG601/ADG602 ideally suited to many applications, particularly those requiring low distortion. These switches are ideal for replacements for mechanical relays because they are more reliable, have lower power requirements, and are available in much smaller package sizes.

The ADG601 is a normally open (NO) switch, while the ADG602 is normally closed (NC). Each switch conducts equally well in both directions when ON, with the input signal range extending to the supply rails.

The switches are available in tiny 6-lead SOT-23 and 8-lead MSOP packages.

PRODUCT HIGHLIGHTS

1. Low On Resistance (2 Ω typical).
2. Dual ±2.7 V to ±5.5 V or Single +2.7 V to +5.5 V Supplies.
3. Tiny 6-Lead SOT-23 and 8-Lead MSOP Packages.
4. Rail-to-Rail Input Signal Range.

Rev. B

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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
				V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance (R_{ON})	2		Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 14
	2.5	5.5	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.35	0.4	Ω typ	V_S = ±3.3 V, I_S = −10 mA
	0.5	0.6	Ω max	
LEAKAGE CURRENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage I_S (Off)	±0.01		nA typ	V_S = +4.5 V/−4.5 V, V_D = −4.5 V/+4.5 V; see Figure 15
	±0.25	±1	nA max	
Drain Off Leakage I_D (Off)	±0.01		nA typ	V_S = +4.5 V/−4.5 V, V_D = −4.5 V/+4.5 V; see Figure 15
	±0.25	±1	nA max	
Channel On Leakage I_D, I_S (On)	±0.01		nA typ	V_S = V_D = +4.5 V or −4.5 V; see Figure 16
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	80		ns typ	R_L = 300 Ω, C_L = 35 pF
	120	155	ns max	V_S = 3.3 V; see Figure 17
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	90	ns max	V_S = 3.3 V; see Figure 17
Charge Injection	250		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 18
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Bandwidth −3 dB	180		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 20
C_S (OFF)	50		pF typ	f = 1 MHz
C_D (OFF)	50		pF typ	f = 1 MHz
C_D, C_S (ON)	145		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	
I_{SS}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Temperature range is as follows: B Version: −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.[1]

Table 3.

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
				V_{DD} = 4.5 V
On Resistance (R_{ON})	3.5		Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA; see Figure 14
	5	8	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.2	0.2	Ω typ	V_S = 1.5 V to 3.3 V, I_S = −10 mA
		0.35	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage I_S (Off)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V; see Figure 15
	±0.25	±1	nA max	
Drain Off Leakage I_D (Off)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V; see Figure 15
	±0.25	±1	nA max	
Channel On Leakage I_D, I_S (On)	±0.01		nA typ	V_S = V_D = 4.5 V or 1 V; see Figure 16
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	110		ns typ	R_L = 300 Ω, C_L = 35 pF
	220	280	ns max	V_S = 3.3 V; see Figure 17
t_{OFF}	50		ns typ	R_L = 300 Ω, C_L = 35 pF
	80	110	ns max	V_S = 3.3 V; see Figure 17
Charge Injection	20		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 18
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Bandwidth −3 dB	180		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 20
C_S (OFF)	50		pF typ	f = 1 MHz
C_D (OFF)	50		pF typ	f = 1 MHz
C_D, C_S (ON)	145		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Temperature range is as follows: B Version: −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +6.5 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, or whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D	
(Pulsed at 1 ms, 10% Duty Cycle Max)	200 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Resistance	
MSOP Package	
θ_{JA}	206 °C/W
θ_{JC}	44 °C/W
SOT-23 Package	
θ_{JA}	229.6 °C/W
θ_{JC}	91.99 °C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

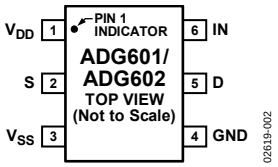


Figure 2. 6-Lead SOT-23 (RT-6)

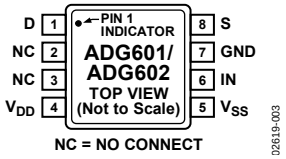


Figure 3. 8-Lead MSOP (RM-8)

Table 5. Pin Function Descriptions

Pin No.			
6-Lead SOT-23	**8-Lead MSOP**	**Mnemonic**	**Description**
1	4	V_{DD}	Most Positive Power Supply Potential.
2	8	S	Source Terminal. May be an input or output.
3	5	V_{SS}	Most Negative Power Supply Potential.
4	7	GND	Ground (0 V) Reference.
5	1	D	Drain Terminal. May be an input or output.
6	6	IN	Logic Control Input.
–	2, 3	NC	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

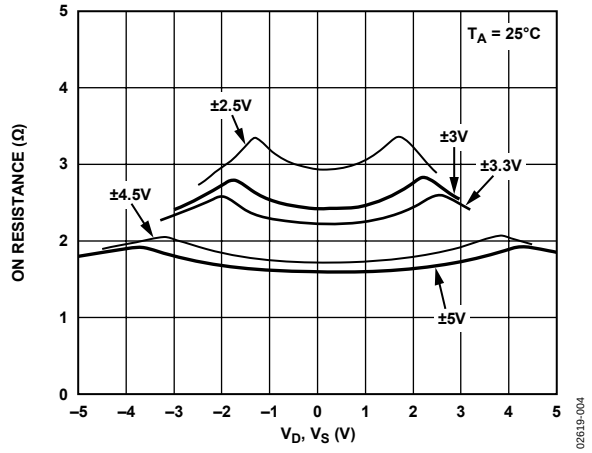


Figure 4. On Resistance vs. V_D (V_S) (Dual Supply)

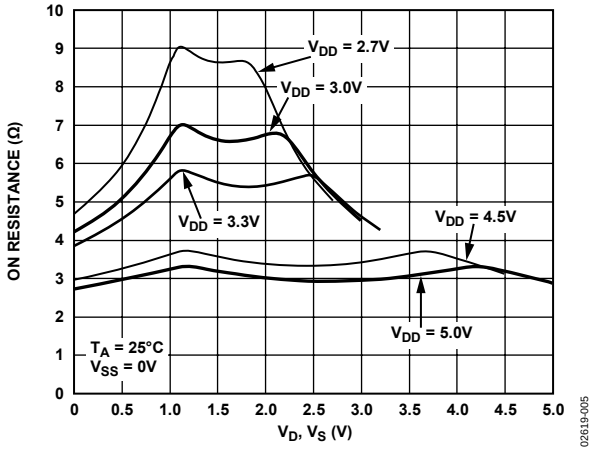


Figure 5. On Resistance vs. V_D (V_S) (Single Supply)

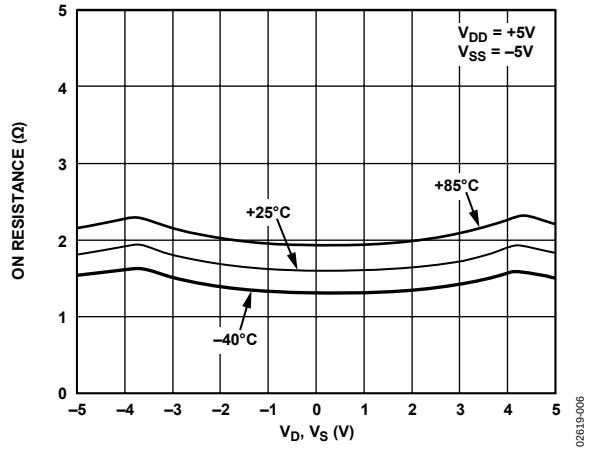


Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures (Dual Supply)

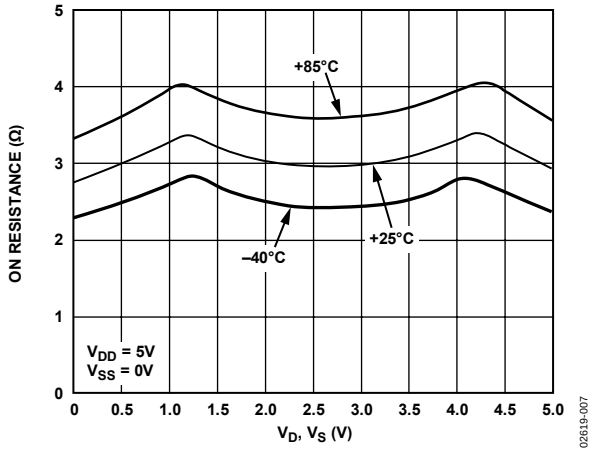


Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

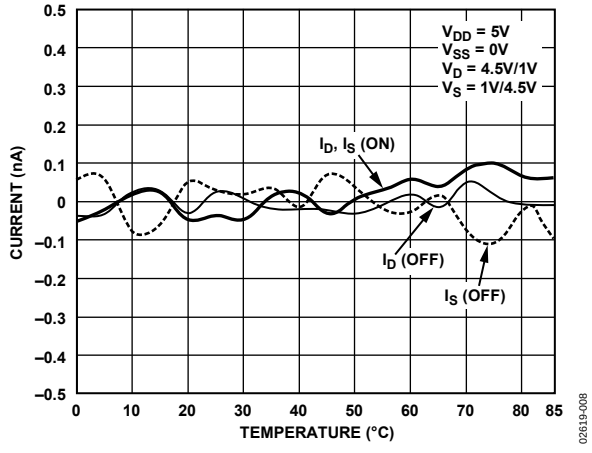


Figure 8. Leakage Currents vs. Temperature (Single Supply)

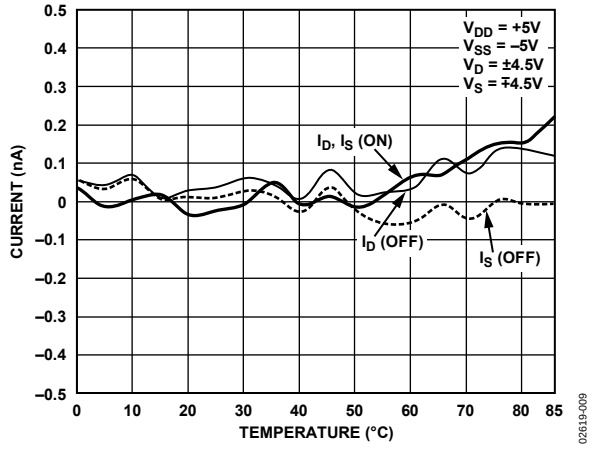


Figure 9. Leakage Currents vs. Temperature (Dual Supply)

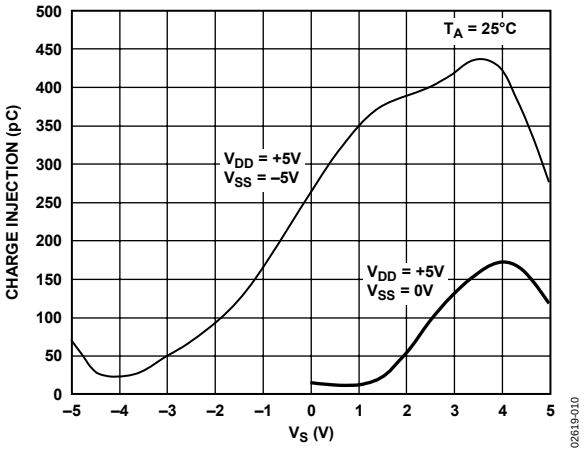


Figure 10. Charge Injection vs. Source Voltage

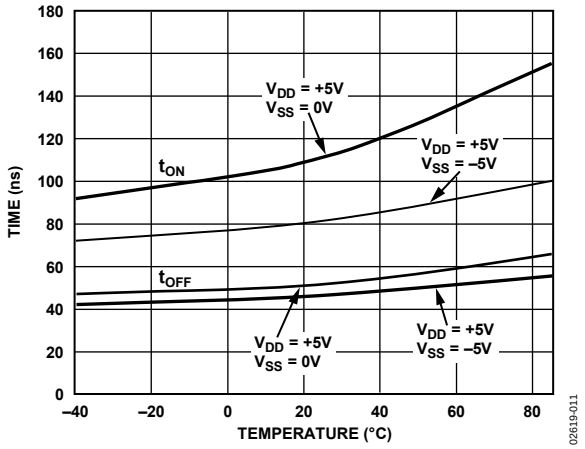


Figure 11. t_{ON}/t_{OFF} Times vs. Temperature

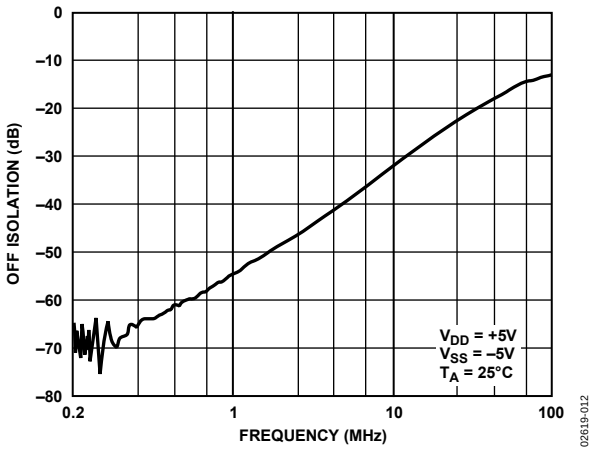


Figure 12. Off Isolation vs. Frequency

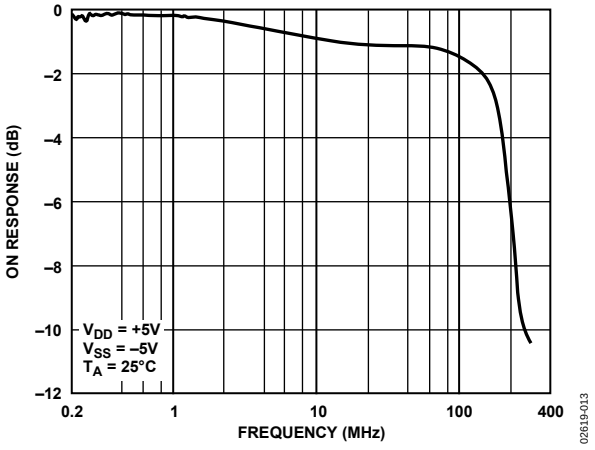


Figure 13. On Response vs. Frequency

TEST CIRCUITS

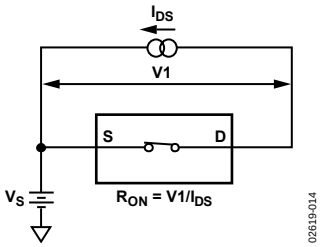


Figure 14. On Resistance

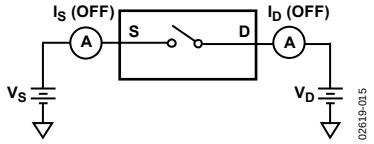


Figure 15. Off Leakage

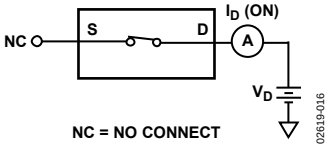
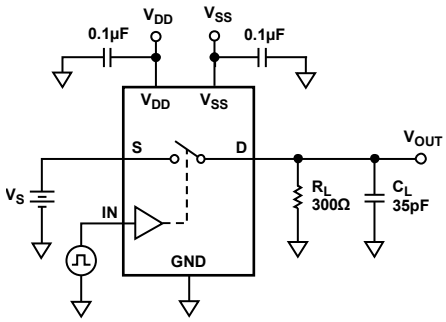


Figure 16. On Leakage



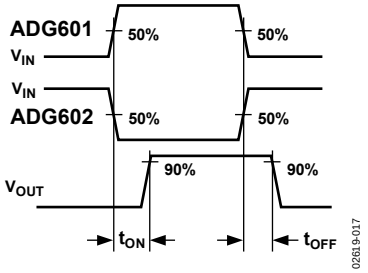
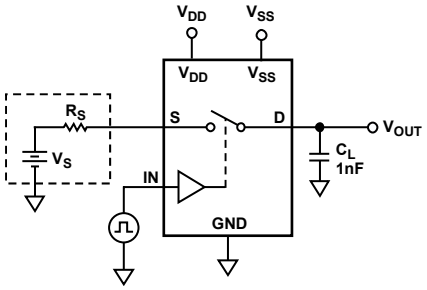


Figure 17. Switching Times



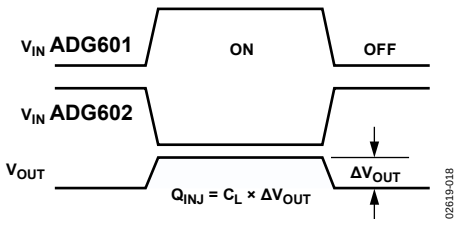


Figure 18. Charge Injection

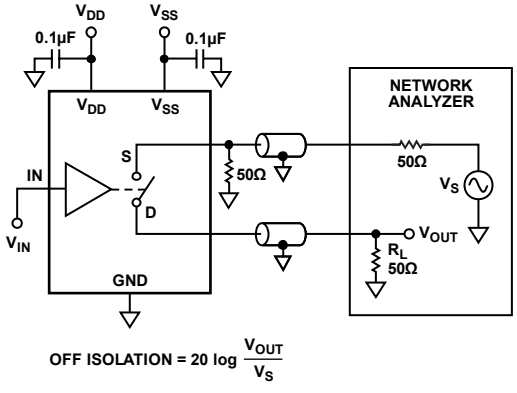


Figure 19. Off Isolation

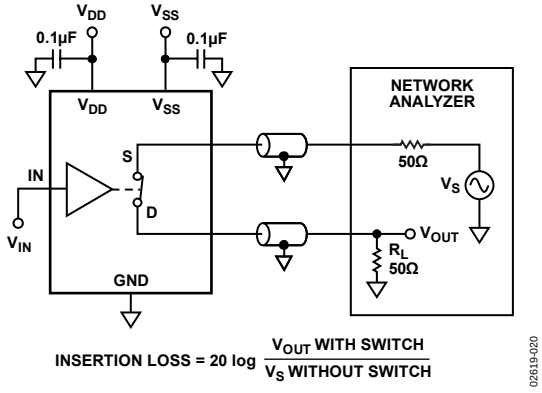


Figure 20. Bandwidth

TERMINOLOGY

V_{DD}

Most positive power supply potential.

V_{SS}
Most negitive power supply potential.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

GND
Ground (0 V) reference.

S
Source terminal. May be an input or an output.

D
Drain terminal. May be an input or an output.

IN
Logic control input.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum values of on resistance as measured over the specified analog signal range.

I_S (OFF)
Source leakage current with the switch off.

I_D (OFF)
Drain leakage current with the switch off.

I_D, I_S (ON)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (OFF)
Off switch source capacitance. Measured with reference to ground.

C_D (OFF)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (ON)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay between applying the digital control input and the output switching on.

t_{OFF}
Delay between applying the digital control input and the output switching off.

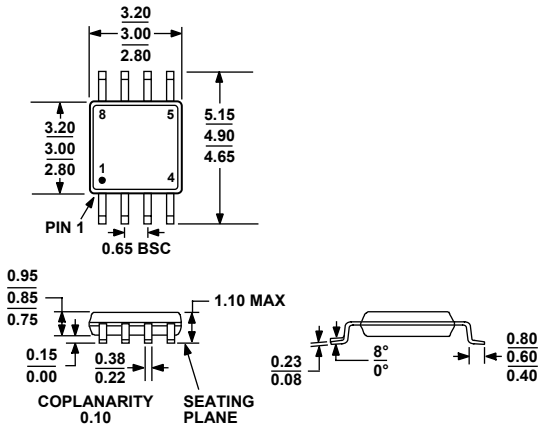
Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

On Response
Frequency response of the on switch.

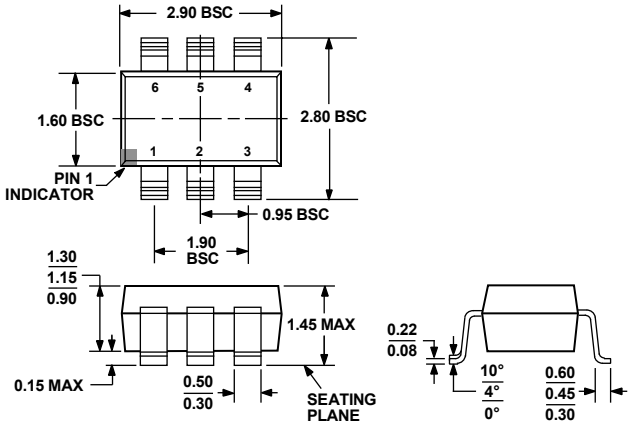
Insertion Loss
Loss due to the on resistance of the switch.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 21. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 22. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG601BRT-REEL	−40°C to +85°C	6-Lead SOT-23	RJ-6	STB
ADG601BRT-REEL7	−40°C to +85°C	6-Lead SOT-23	RJ-6	STB
ADG601BRTZ-REEL[2]	−40°C to +85°C	6-Lead SOT-23	RJ-6	STB#
ADG601BRTZ-REEL7[2]	−40°C to +85°C	6-Lead SOT-23	RJ-6	STB#
ADG601BRM	−40°C to +85°C	8-Lead MSOP	RM-8	STB
ADG601BRM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	STB
ADG601BRM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	STB
ADG601BRMZ[2]	−40°C to +85°C	8-Lead MSOP	RM-8	S1G
ADG601BRMZ-REEL[2]	−40°C to +85°C	8-Lead MSOP	RM-8	S1G
ADG601BRMZ-REEL7[2]	−40°C to +85°C	8-Lead MSOP	RM-8	S1G
ADG602BRT-REEL	−40°C to +85°C	6-Lead SOT-23	RJ-6	SUB
ADG602BRT-REEL7	−40°C to +85°C	6-Lead SOT-23	RJ-6	SUB
ADG602BRTZ-REEL[2]	−40°C to +85°C	6-Lead SOT-23	RJ-6	S18
ADG602BRTZ-REEL7[2]	−40°C to +85°C	6-Lead SOT-23	RJ-6	S18
ADG602BRM	−40°C to +85°C	8-Lead MSOP	RM-8	SUB
ADG602BRM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	SUB
ADG602BRM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	SUB
ADG602BRMZ[2]	−40°C to +85°C	8-Lead MSOP	RM-8	S18
ADG602BRMZ-REEL7[2]	−40°C to +85°C	8-Lead MSOP	RM-8	S18

[1] Branding on SOT-23 and MSOP packages is limited to three characters due to space constraints.
[2] Z = Pb-free part, # denotes lead-free, may be top or bottom marked.

NOTES

D02619-0-3/06(B)