- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Provides Extra Bus Driving Latches Necessary For Wider Address/Data Paths or Buses With Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic “Small Outline” Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

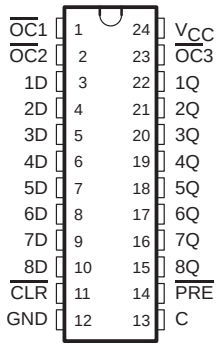
## description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

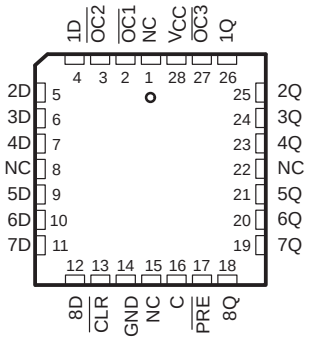
The eight latches are transparent D-type. The ′ALS29845 has noninverting data (D) inputs. The ′ALS29846 has inverting $\overline{D}$ inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need

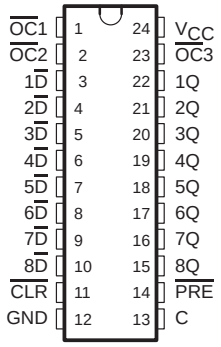
SN74ALS29845 . . . DW or NT Package
(Top View)



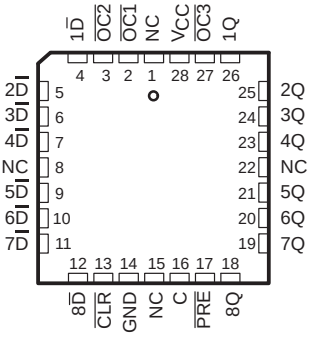

SN74ALS29845 . . . FN Package
(Top View)




SN74ALS29846 . . . DW or NT Package
(Top View)




SN74ALS29846 . . . FN Package
(Top View)




NC — No internal connection

## description (continued)

for interface or pullup components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALS29845 and SN74ALS29846 are characterized for operation from 0°C to 70°C

**FUNCTION TABLES**

**′ALS29845**

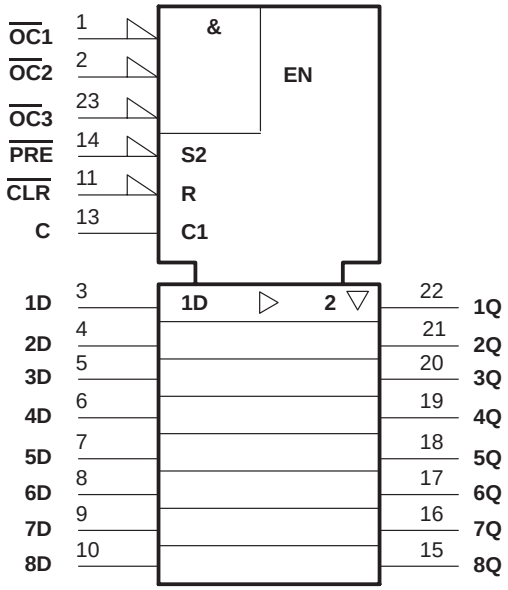
| INPUTS | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | $\overline{OC1}$ | $\overline{OC2}$ | $\overline{OC3}$ | C | D | Q |
| L | X | L | L | L | X | X | H |
| H | L | L | L | L | X | X | L |
| H | H | L | L | L | H | L | H |
| H | H | L | L | L | H | H | L |
| H | H | L | L | L | L | X | $Q_0$ |
| X | X | X | X | H | X | X | Z |
| X | X | X | H | X | X | X | Z |
| X | X | H | X | X | X | X | Z |

**′ALS29846**

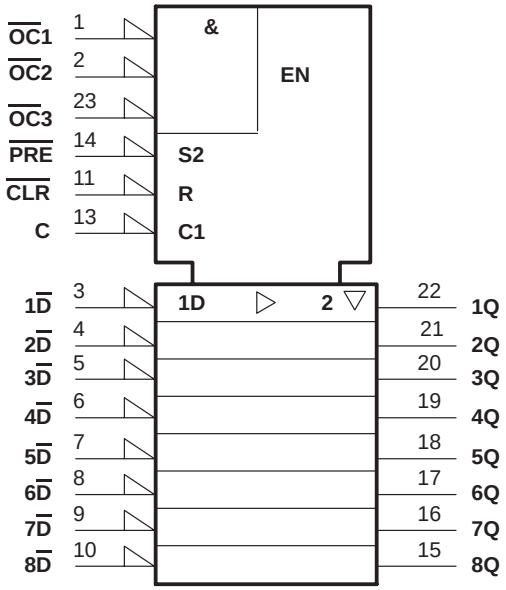
| INPUTS | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | $\overline{OC1}$ | $\overline{OC2}$ | $\overline{OC3}$ | C | D | Q |
| L | X | L | L | L | X | X | H |
| H | L | L | L | L | X | X | L |
| H | H | L | L | L | H | L | H |
| H | H | L | L | L | H | H | L |
| H | H | L | L | L | L | X | $Q_0$ |
| X | X | X | X | H | X | X | Z |
| X | X | X | H | X | X | X | Z |
| X | X | H | X | X | X | X | Z |

## logic symbols†

**′ALS29845**

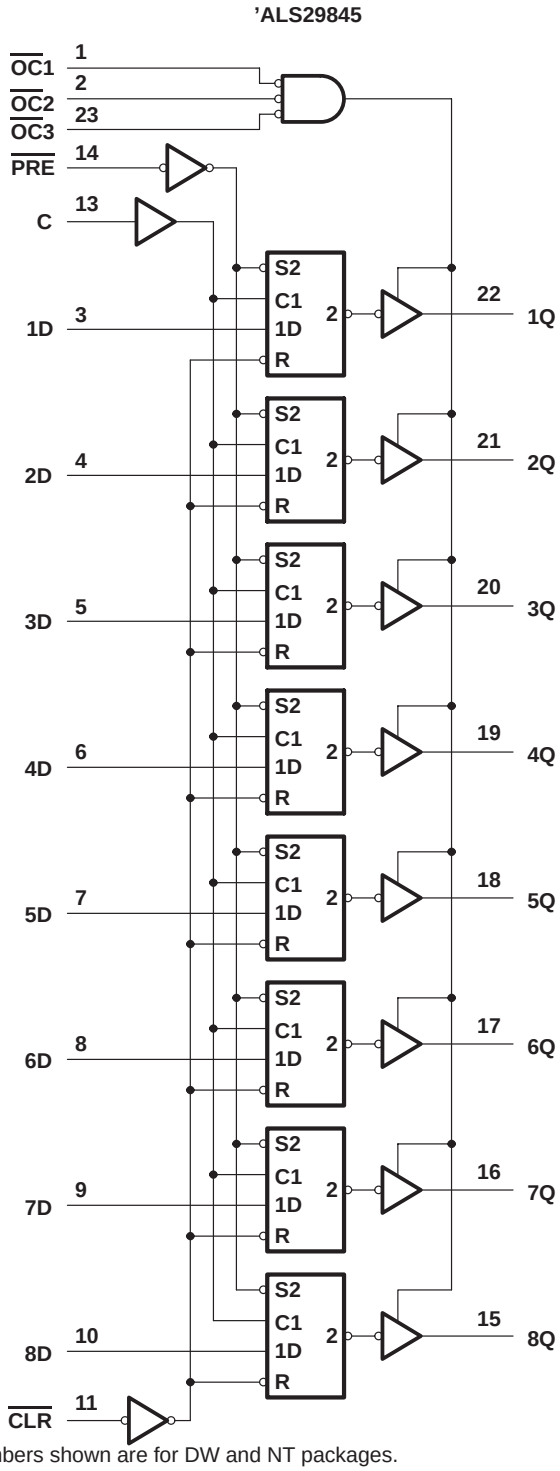


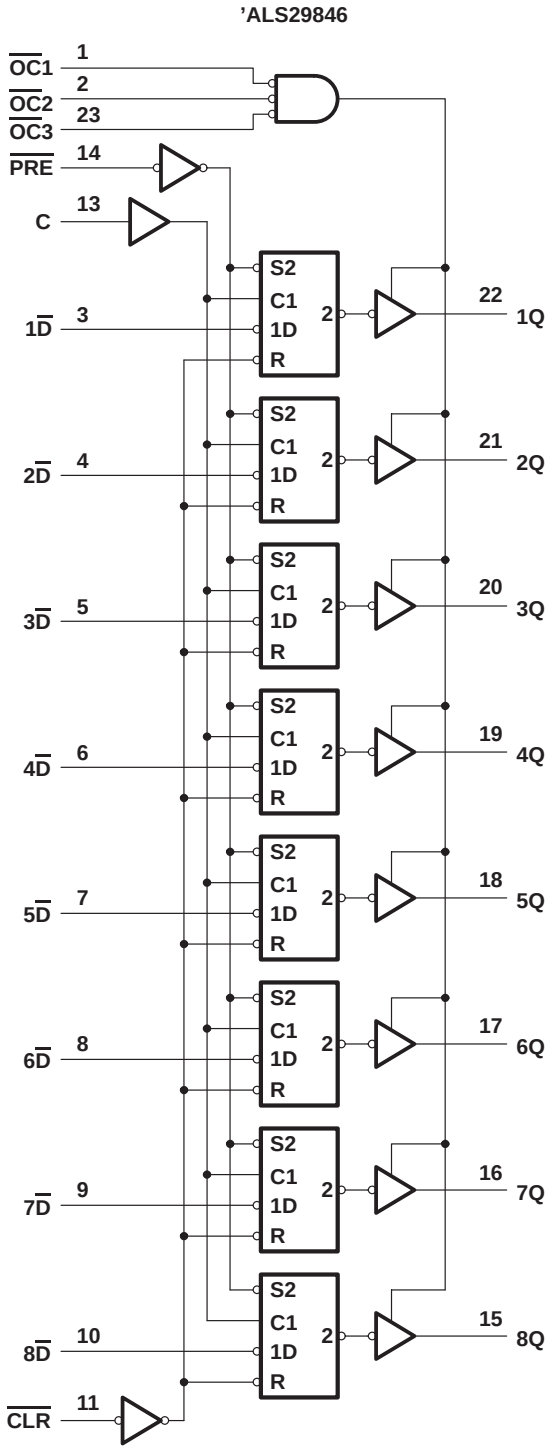

**′ALS29846**




† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

## logic diagrams (positive logic)




Pin numbers shown are for DW and NT packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to GND.

### recommended operating conditions

| | | | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 5 | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | | | | – 24 | mA |
| $I_{OL}$ | Low-level output current | | | | | | | 48 | mA |
| $t_w$ | Pulse duration | $\overline{PRE}$ low | 5 | | | 8 | | | ns |
| | | $\overline{CLR}$ low | 6 | | | 8 | | | |
| | | C high | 4 | | | 6 | | | |
| $t_{su}$ | Setup time before enable C↓ | Data | 2.5 | | | 2.5 | | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$, inactive state | 12 | | | 14 | | | |
| $t_h$ | Hold time, data after enable C↓ | | 4.5 | | | 4.5 | | | ns |
| $T_A$ | Operating free-air temperature | | | 25 | | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.75 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –15 mA | 2.4 | 3.3 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 24 mA | 2 | 3.1 | | |
| $V_{OL}$ | $V_{CC}$ = 4.75 V, | $I_{OL}$ = 48 mA | | 0.35 | 0.5 | V |
| $I_{OZH}$ | $V_{CC}$ = 5.25 V, | $V_O$ = 2.7 V | | | 20 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.25 V, | $V_O$ = 0.4 V | | | – 20 | µA |
| $I_I$ | $V_{CC}$ = 5.25 V, | $V_I$ = 5.5 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.25 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.25 V, | $V_I$ = 0.4 V | | | – 0.2 | mA |
| $I_O$§ | $V_{CC}$ = 5.25 V, | $V_O$ = 0 | – 75 | | – 250 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.25 V, | Outputs low | | 55 | 85 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = MIN TO MAX†, $T_A$ = MIN TO MAX† | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | D | Any Q | $C_L$ = 50 pF | 2 | 5.7 | 8 | 2 | | 9.5 | ns |
| $t_{PHL}$ | | | | 2 | 6.2 | 8 | 2 | | 9.5 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | 10 | 12.5 | | | 14 | |
| $t_{PHL}$ | | | | | 10 | 14 | | | 14 | |
| $t_{PLH}$ | C | Any Q | $C_L$ = 50 pF | | 8 | 10.5 | | | 12 | ns |
| $t_{PHL}$ | | | | | 7.5 | 10 | | | 12 | |
| $t_{PLH}$ | | | $C_L$ = 300 pF | | | 15 | | | 16 | |
| $t_{PHL}$ | | | | | | 15 | | | 16 | |
| $t_{PLH}$ | $\overline{PRE}$ | Any Q | $C_L$ = 50 pF | | 6.5 | 9 | | | 12 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | $C_L$ = 50 pF | | 7 | 10 | | | 13 | ns |
| $t_{PZH}$ | OC | Any Q | $C_L$ = 50 pF | | 7.3 | 12 | | | 14 | ns |
| $t_{PZL}$ | | | | | 9.7 | 12 | | | 14 | |
| $t_{PZH}$ | | | $C_L$ = 300 pF | | | 17 | | | 20 | |
| $t_{PZL}$ | | | | | | 21 | | | 23 | |
| $t_{PHZ}$ | OC | Any Q | $C_L$ = 50 pF | | 10.4 | 14 | | | 15 | ns |
| $t_{PLZ}$ | | | | | 4.7 | 11 | | | 12 | |
| $t_{PHZ}$ | | | $C_L$ = 5 pF | | 3.4 | 8 | | | 9 | |
| $t_{PLZ}$ | | | | | 3.8 | 8 | | | 9 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## PARAMETER MEASUREMENT INFORMATION

SWITCH POSITION TABLE

| TEST | S1 | S2 |
|---|---|---|
| $t_{PLH}$ | Closed | Closed |
| $t_{PHL}$ | Closed | Closed |
| $t_{PZH}$ | Open | Closed |
| $t_{PZL}$ | Closed | Open |
| $t_{PHZ}$ | Closed | Closed |
| $t_{PLZ}$ | Closed | Closed |

Missing illustration

NOTES: A. $C_L$ includes proge and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by henerators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.

**Figure 1**

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