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AK4191

Premium Digital ΔΣ Modulator

1. General Description

The AK4191 is a 64-bit Stereo Digital Delta-Sigma Modulator, achieving high quality sound reproduction. It corresponds to a 1536kHz PCM input and an DSD1024 input at maximum, suitable for playback of high resolution audio sources that are becoming widespread in Network Audio and USB-DACs Audio systems. In addition, it is capable of supporting a wide range of signals and achieving low out-of-band noise. The AK4191 has six types of 64-bit digital filters, realizing simple and flexible sound reproduction in wide range of applications.

2. Features

- Digital Delta-Sigma Modulator
  - 7-bit Modulator Data output
  - Delta-Sigma Modulator Option
- 256x/128x Over Sampling
- Sampling Rate: 44.1 kHz to 1536 kHz (PCM, EXDF)
- 64-bit 256x/128x Digital Filter
  - Ripple: ±0.001 dB, Attenuation: 150 dB (Sharp Roll-Off Filter Setting)
  - Six Types of High Quality Sound Filter Option
    - ・Short Delay Sharp Roll-off, GD = 9.0/fs
    - ・Short Delay Slow Roll-off, GD = 5.4/fs
    - ・Sharp Roll-off
    - ・Slow Roll-off
    - ・Super Slow Roll-off
    - ・Low Dispersion Short Delay Filter
    - ・Programmable Filter
- DSD64, DSD128, DSD256, DSD512, DSD1024 Input Support
  - Filter1 (fc = 19 kHz, DSD64 mode)
  - Filter2 (fc = 39 kHz, DSD64 mode)
- Digital De-emphasis for 32, 44.1 and 48 kHz sampling
- Soft Mute
- Digital Attenuator (0 dB to -127 dB, 0.5 dB step + mute)
- 7-bit Modulator Data input Interface
  - Volume (+6.0 dB to -127 dB, 0.5 dB step + mute)
- External Digital Filter Interface (EXDF Mode)
- Audio I/F Format
  - Dual PCM I/F
    - MSB Justified
    - LSB Justified
    - I^2S
  - DSD
  - TDM
- PCM/DSD, EXDF/DSD Mode Automatic Mode Switching Function
- Data Synchronization to Master Clock
- Mono Mode

- Master Clock
  - 11.2896MHz/12.288MHz
- Register Control Mode with 4-wire Serial or I^2C interface
- Power Supply:
  PVDD = 3.0 to 3.6 V
  TVDD1/2/3/4 = 1.7 to 3.6 V, DVDD = 1.14 to 1.3 V
- Operational Temperature: -40 to 85 °C
- Digital Input Level: CMOS
- Package: 64-pin HTQFP

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3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram

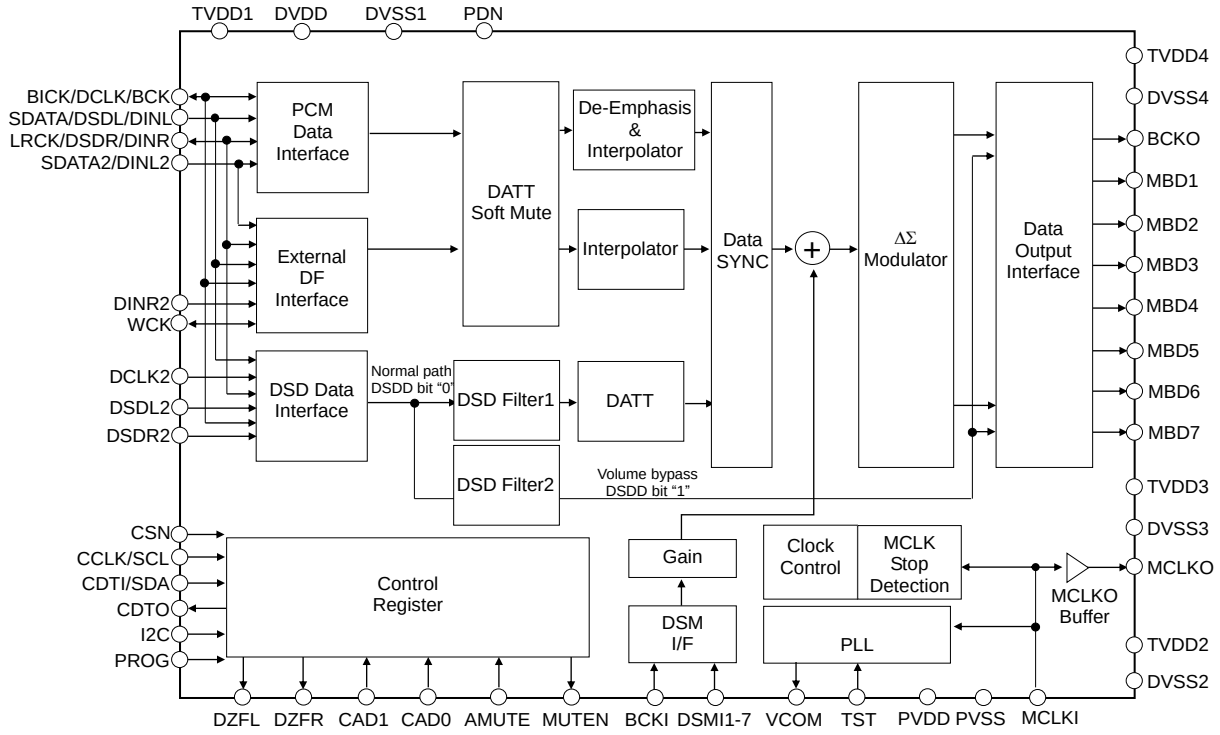


Figure 1. AK4191 Block Diagram1 (Synchronous Mode)

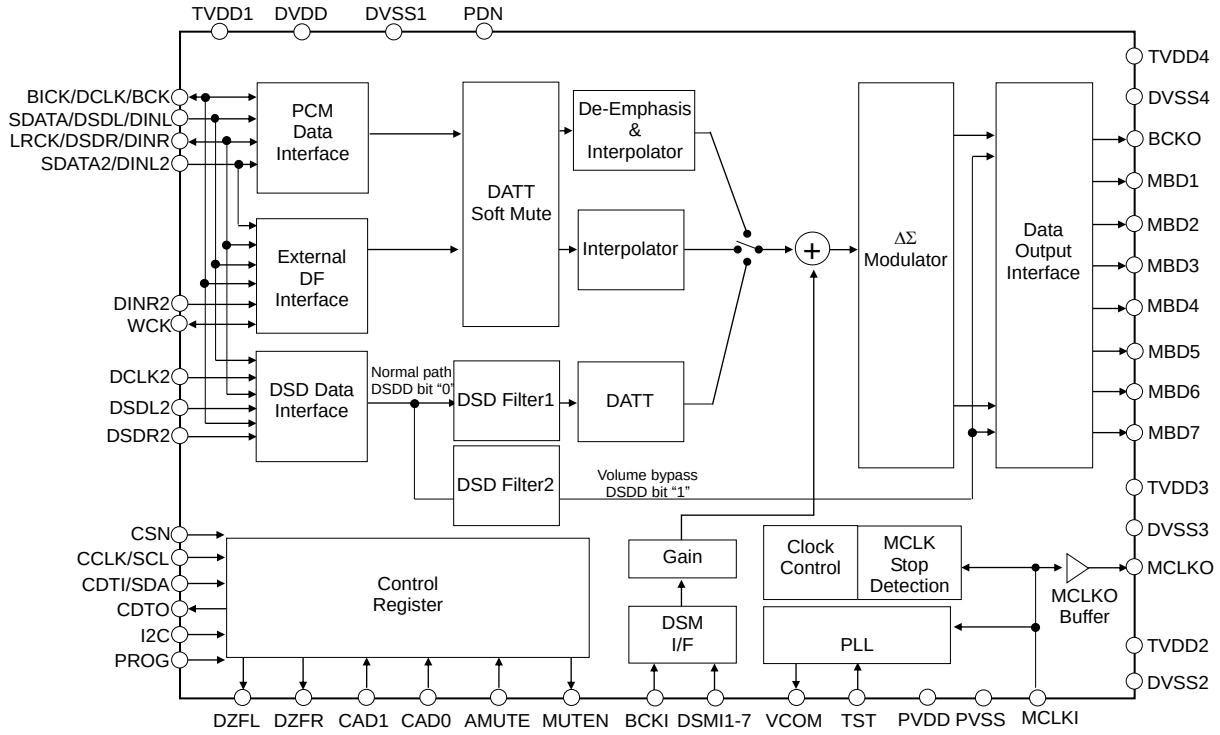


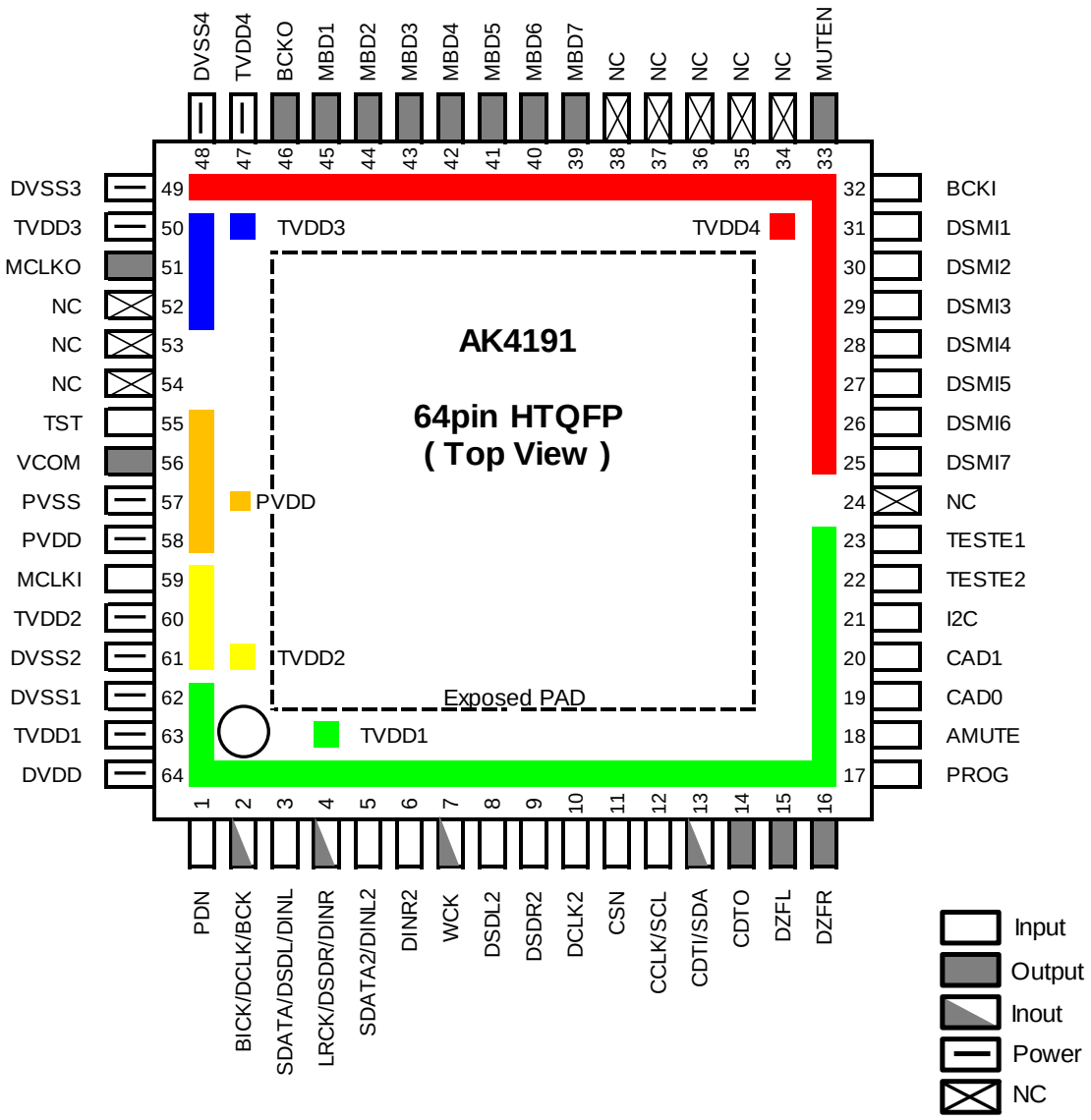
Figure 2. AK4191 Block Diagram2 (Asynchronous Mode)

4.2. Functions

Block	Function
PCM Data Interface	Execute serial/parallel conversion of SDATA, SDATA2 input data by synchronizing with LRCK and BICK.
External DF Interface	Receive external digital filter outputs. Execute serial/parallel conversion of DINL/L2 and DINR/R2 input data by synchronizing with BICK.
DSD Data Interface	1-bit data that is input from DSDL and DSDR pins is received by synchronizing with DCLK.
DSD Filter 1/2	FIR filter that reduces high frequency noise of DSD input data
DATT, Soft Mute	Apply DATT and Soft Mute process to input data.
De-emphasis & Interpolator	A digital filter that applies De-emphasis process to input data and executes over sampling.
ΔΣ Modulator	Output multi-bit data to Analog-DAC. This block consists of a third-order digital delta-sigma modulator.
Control Register	Keep register settings for each mode. Control registers are accessed in 4-wire (CSN, CCLK, CDTI) or I2C-Bus (SCL, SDA) control mode.
PLL	Generates internal master clock from the input clock of the MCLKI pin.
Clock Control	Divide internal master clock. In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode
MCLK Stop Detection	Detects when the master clock input is absent.
MCLKO Buffer	MCLKO level shifter.
Data SYNC	Data synchronization block
DSM I/F	Multi-bit Delta-Sigma data that is input from DSM1-7 pins is received by synchronizing with BCK.
Gain	Apply Gain Control process to Multi-bit ADC data

5. Pin Configurations and Functions

5.1. Pin Configurations



Note 1: The exposed pad on the bottom surface of the package should be connected to PVSS.

5.2. Functions

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
1	PDN	I	TVDD1/DVSS1	Power-Up, Power-Down Pin When at “L”, the AK4191 is in power-down mode. The AK4191 must always be in power-down mode upon power on.	Hi-Z (PDN=“L”)
2	BICK	I/O	TVDD1/DVSS1	Audio Serial Data Clock Pin in PCM mode	Pull-down to DVSS1 (46 kΩ, typ)
	BCK	I/O		Audio Serial Data Clock Pin in EXDF mode	
	DCLK	I		Audio Serial Data Clock PIN in DSD mode (@DSDPATH bit = ”1”)	
3	SDATA	I	TVDD1/DVSS1	Audio Serial MSB Data Input Pin in PCM mode	Hi-Z
	DINL	I		Audio Serial MSB Data Input Pin in EXDF mode	
	DSDL	I		Audio Serial Data Input Pin in DSD mode	
4	LRCK	I/O	TVDD1/DVSS1	Input Channel Clock pin in PCM mode	Pull-down to DVSS1 (46 kΩ, typ)
	DINR	I		Audio Serial MSB Data Input Pin in EXDF mode	
	DSDR	I		Audio Serial Data Input Pin in DSD mode	
5	SDATA2	I	TVDD1/DVSS1	Audio Serial LSB Data Input pin in PCM mode	Hi-Z
	DINL2	I		Audio Serial LSB Data Input pin in EXDF mode	
6	DINR2	I	TVDD1/DVSS1	Audio Serial LSB Data Input pin in EXDF mode	Hi-Z
7	WCK	I/O	TVDD1/DVSS1	Word Clock input pin in EXDF mode	Pull-down to DVSS1 (46 kΩ, typ)
8	DSDL2	I	TVDD1/DVSS1	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = “0”)	Hi-Z
9	DSDR2	I	TVDD1/DVSS1	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = “0”)	Hi-Z
10	DCLK2	I	TVDD1/DVSS1	DSD Clock pin in DSD mode (@DSDPATH bit = “0”)	Hi-Z
11	CSN	I	TVDD1/DVSS1	Chip Select pin in 4-wire serial Register Control mode	Hi-Z
12	CCLK	I	TVDD1/DVSS1	Control Data Clock pin in 4-wire serial Register Control mode	Hi-Z
	SCL	I		Control Data Clock Input pin in I^2C Bus Register Control mode	
13	CDTI	I	TVDD1/DVSS1	Control Data Input pin in 4-wire serial Register Control mode	Hi-Z
	SDA	I/O		Control Data Input pin in I^2C Bus Register Control mode	
14	CDTO	O	TVDD1/DVSS1	Control Data Output pin in 4-wire serial Register Control mode	Hi-Z
15	DZFL	O	TVDD1/DVSS1	Lch Zero Input Detect pin	“L” Output
16	DZFR	O	TVDD1/DVSS1	Rch Zero Input Detect pin	“L” Output
17	PROG	I	TVDD1/DVSS1	Programmable Filter Coefficient Setting Enable	Hi-Z

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
18	AMUTE	I	TVDD1/DVSS1	MUTE Control	Hi-Z
19	CAD0	I	TVDD1/DVSS1	Chip Address 0 pin in Register Control mode	Hi-Z
20	CAD1	I	TVDD1/DVSS1	Chip Address 1 pin in Register Control mode	Hi-Z
21	I2C	I	TVDD1/DVSS1	Serial Control Interface Select pin in Register Control mode. "L": 4-wire serial control interface. "H": I^2C Bus serial control interface.	Hi-Z
22	TESTE2	I	TVDD1/DVSS1	Connect to DVSS (Internal pull-down pin)	Pull-down to DVSS1 (46 kΩ, typ)
23	TESTE1	I	TVDD1/DVSS1	Connect to DVSS (Internal pull-down pin)	Pull-down to DVSS1 (46 kΩ, typ)
24	NC	-	-	No internal bonding. Connect to PVSS	-
25	DSMI7	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
26	DSMI6	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
27	DSMI5	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
28	DSMI4	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
29	DSMI3	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
30	DSMI2	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
31	DSMI1	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
32	BCKI	I	TVDD4/DVSS4	Digital Audio Data Input Pin	Hi-Z
33	MUTEN	O	TVDD4/DVSS4	MUTE_N Output for Analog-DAC	"L" Output
34-38	NC	-	-	No internal bonging. Connect to PVSS	-
39	MBD7	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
40	MBD6	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
41	MBD5	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
42	MBD4	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
43	MBD3	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
44	MBD2	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
45	MBD1	O	TVDD4/DVSS4	Digital Audio Data Output Pin	"L" Output
46	BCKO	O	TVDD4/DVSS4	Digital Audio Data Clock Output Pin	"L" Output

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
47	TVDD4	-	-	Digital Output Power Supply Pin, TVDD4 = TVDD3 - 0.1 V to TVDD3 + 0.1 V	-
48	DVSS4	-	-	Digital Ground Pin	-
49	DVSS3	-	-	Digital Ground Pin	-
50	TVDD3	-	-	MCLKO Output Power Supply Pin, TVDD3 = 1.7 to 3.6 V	-
51	MCLKO	O	TVDD3/DVSS3	MCLK Output Pin	Pull-down to DVSS3 (46 kΩ, typ)
52-54	NC	-	-	No internal bonding. Connect to PVSS	-
55	TST	I	PVDD/PVSS	Test pin	Hi-z
56	VCOM	O	PVDD/PVSS	Analog Block Common Voltage Output. Connect 2.2uF capacitor between this pin and PVSS. This pin must not be connected to external circuit.	Pull-down to PVSS (500 Ω, typ)
57	PVSS	-	-	Analog Ground Pin	-
58	PVDD	-	-	Analog Power Supply Pin, PVDD = 3.0 to 3.6 V	-
59	MCLKI	I	TVDD2/DVSS2	MCLK Input pin	Hi-Z
60	TVDD2	-	-	Digital Power Supply Pin, TVDD2 = 1.7 to 3.6 V	-
61	DVSS2	-	-	Digital Ground Pin	-
62	DVSS1	-	-	Digital Ground Pin	-
63	TVDD1	-	-	Digital Power Supply Pin, TVDD1 = 1.7 to 3.6 V	-
64	DVDD	-	-	1.2V Power Input Pin	-
Exposed PAD		-	-	No internal bonging. Connect to PVSS	-