PMDPB55XPA

20 V, dual P-channel Trench MOSFET

18 March 2024 **Product data sheet**

1. General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- AEC-Q101 qualified

3. Applications

- DC to DC conversion
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

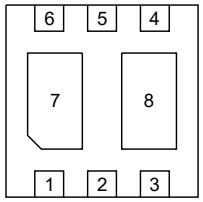
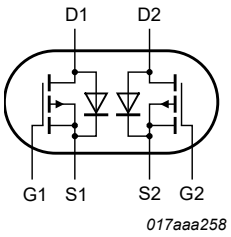
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-20	V
V_{GS}	gate-source voltage			-10	-	10	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-3.6	A
Static characteristics (per transistor)							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -3.6 A; T_j = 25 °C		-	50	66	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2.

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 Transparent top view **DFN2020-6 (SOT1118)**	
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB55XPA	DFN2020-6	plastic, leadless thermal enhanced ultra thin small outline package; no leads; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1118

7. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB55XPA	8N

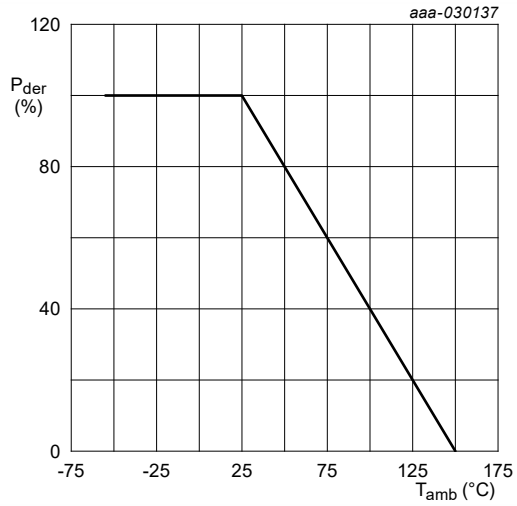
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

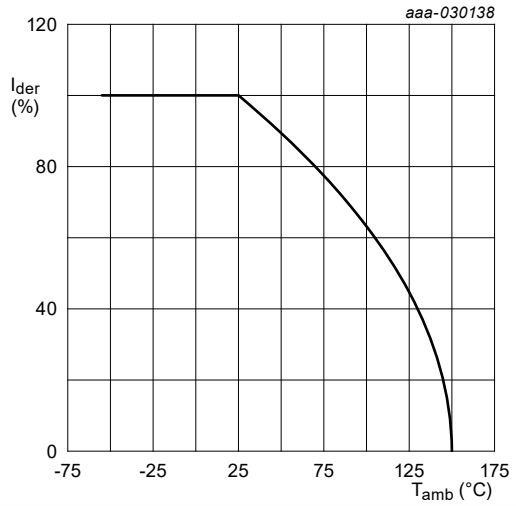
Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	T_j = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-10	10	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-3.6	A
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-2.3	A
		V_{GS} = -4.5 V; T_{sp} = 25 °C		-	-9.3	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \leq$ 10 µs		-	-37	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	490	mW
			[1]	-	1.2	W
		T_{sp} = 25 °C		-	8.3	W
Per device						
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	640	mW
			[1]	-	1.6	W
		T_{sp} = 25 °C		-	11	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode (per transistor)						
I_S	source current	T_{amb} = 25 °C	[1]	-	-1.2	A
Avalanche ruggedness (per transistor)						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = -0.65 A; DUT in avalanche (unclamped)		-	4.4	mJ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_{D(25\,°C)}} \times 100\,\%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature

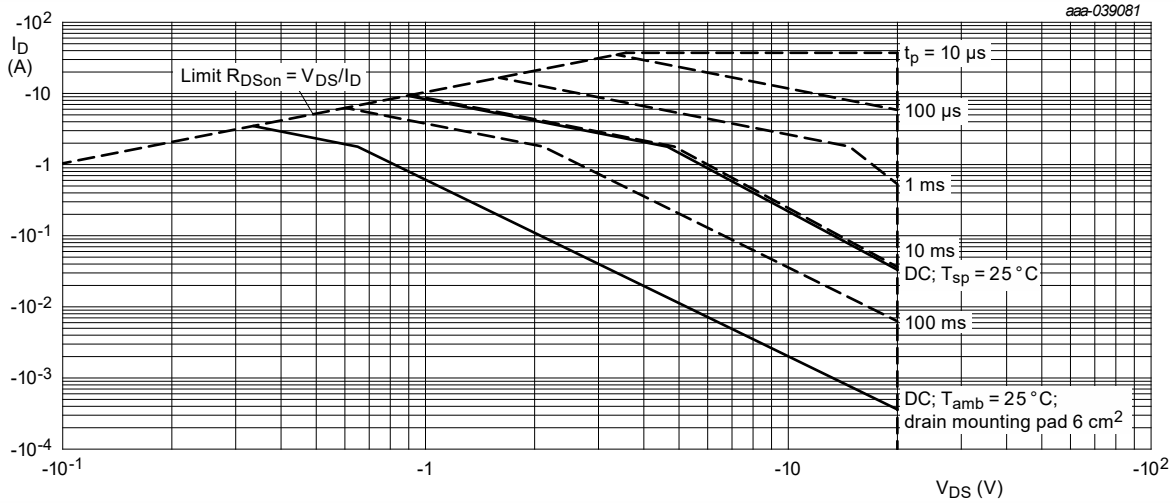


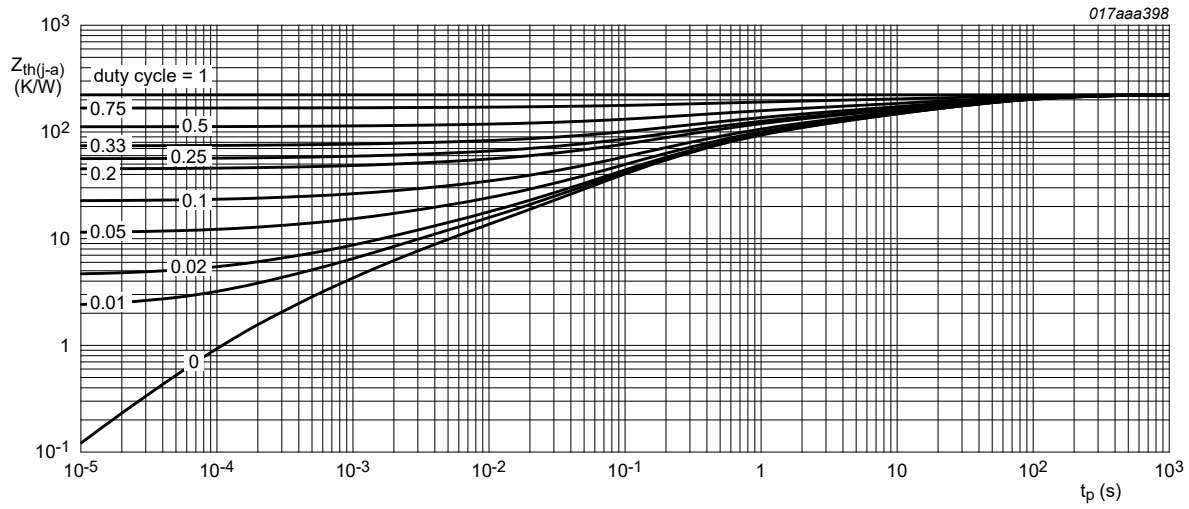
Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

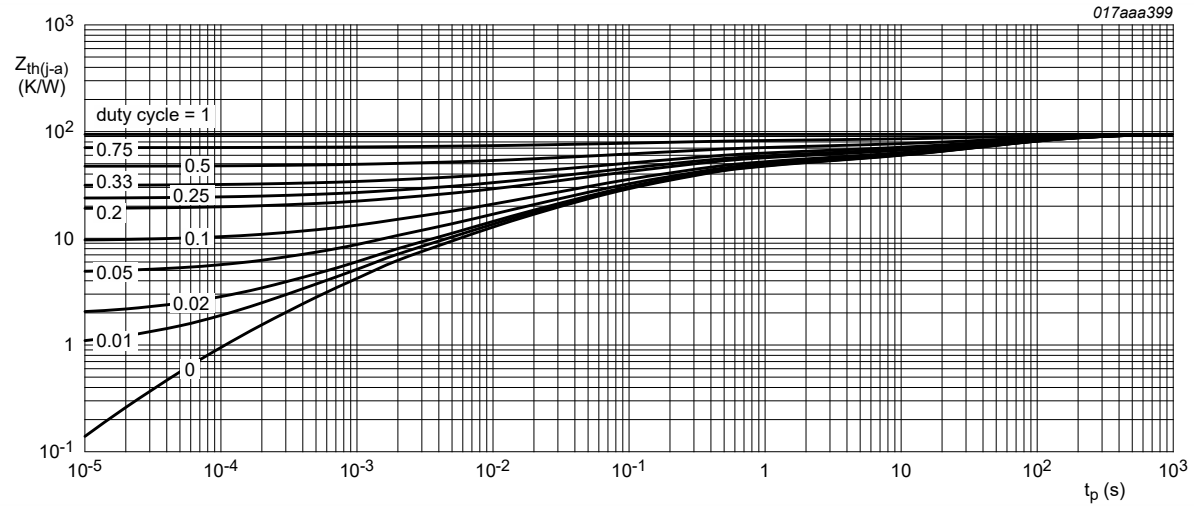
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	223	256	K/W
			[2]	-	93	107	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	190	K/W
			[2]	-	-	80	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	11	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



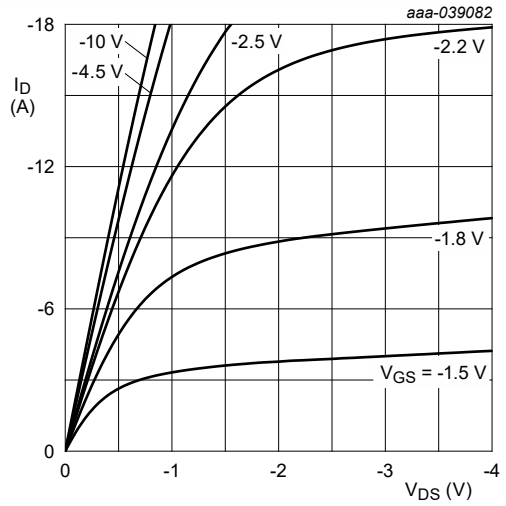
FR4 PCB, mounting pad for drain 6 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

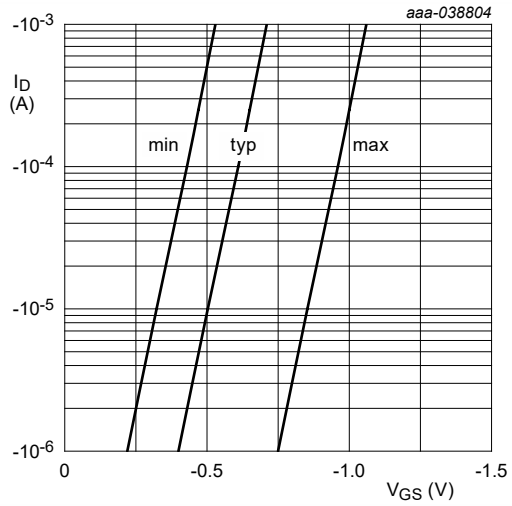
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C		-20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C		-0.47	-0.65	-1	V
I_{DSS}	drain leakage current	V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-1	µA
I_{GSS}	gate leakage current	V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
		V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -3.6 A; T_j = 25 °C		-	50	66	mΩ
		V_{GS} = -4.5 V; I_D = -3.6 A; T_j = 150 °C		-	73	96	mΩ
		V_{GS} = -2.5 V; I_D = -2.6 A; T_j = 25 °C		-	62	87	mΩ
		V_{GS} = -1.8 V; I_D = -0.5 A; T_j = 25 °C		-	83	135	mΩ
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -3.6 A; T_j = 25 °C		-	12	-	S
Dynamic characteristics (per transistor)							
$Q_{G(tot)}$	total gate charge	V_{DS} = -10 V; I_D = -3.6 A; V_{GS} = -4.5 V; T_j = 25 °C		-	8.8	13	nC
Q_{GS}	gate-source charge			-	1.2	-	nC
Q_{GD}	gate-drain charge			-	2.4	-	nC
C_{iss}	input capacitance	V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	785	-	pF
C_{oss}	output capacitance			-	70	-	pF
C_{rss}	reverse transfer capacitance			-	62	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -10 V; I_D = -3.6 A; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	11	-	ns
t_r	rise time			-	2	-	ns
$t_{d(off)}$	turn-off delay time			-	55	-	ns
t_f	fall time			-	135	-	ns
Source-drain diode (per transistor)							
V_{SD}	source-drain voltage	I_S = -1.2 A; V_{GS} = 0 V; T_j = 25 °C		-	-0.8	-1.2	V
t_{rr}	reverse recovery time	I_S = -2 A; dI_S/dt = 60 A/µs; V_{GS} = -4.5 V; V_{DS} = -20 V; T_j = 25 °C		-	14	-	ns
Q_r	recovered charge			-	4.8	-	nC



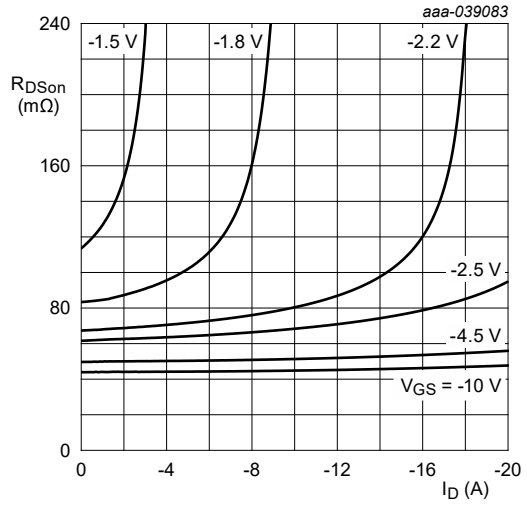
T_j = 25 °C

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



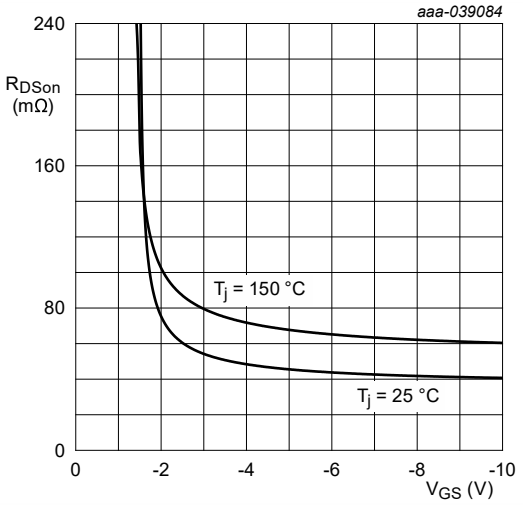
V_{DS} = -5 V; T_j = 25 °C

Fig. 7. Sub-threshold drain current as a function of gate-source voltage



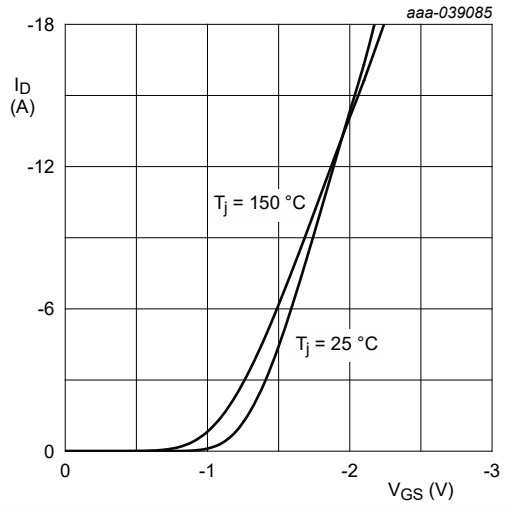
T_j = 25 °C

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



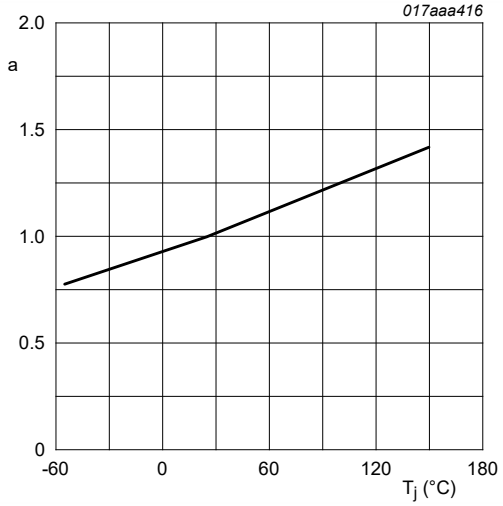
I_D = -3.6 A

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



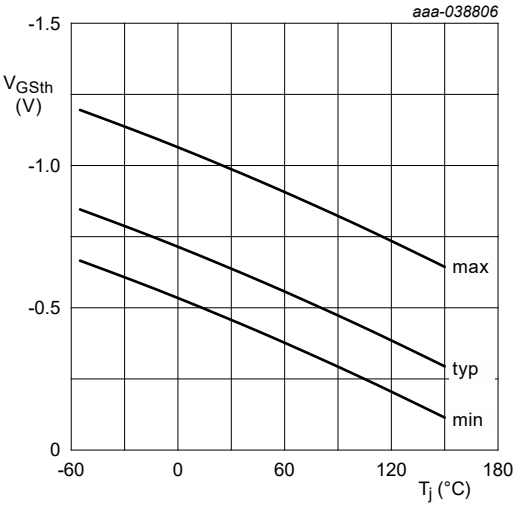
V_{DS} = -5 V

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



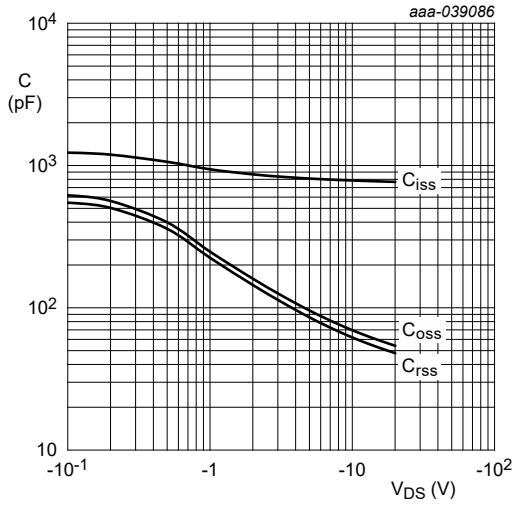
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



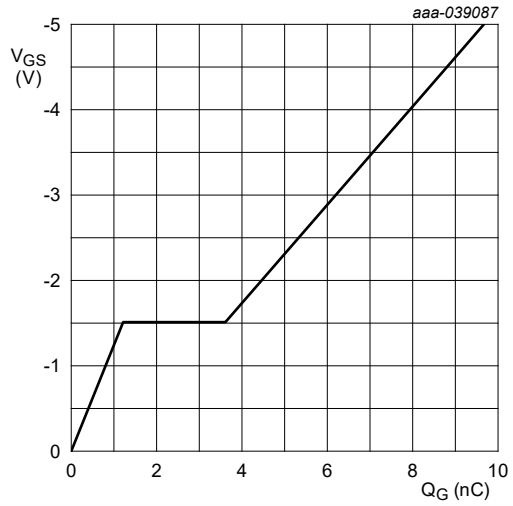
I_D = -250 µA; V_{DS} = V_{GS}

Fig. 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{DS} = -10 V; I_D = -3.6 A; T_{amb} = 25 °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

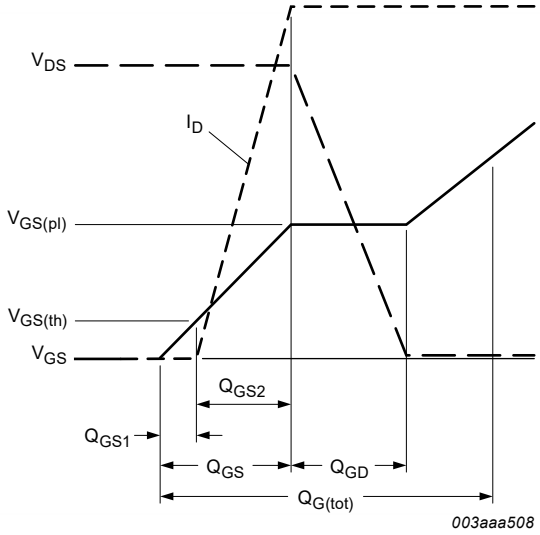
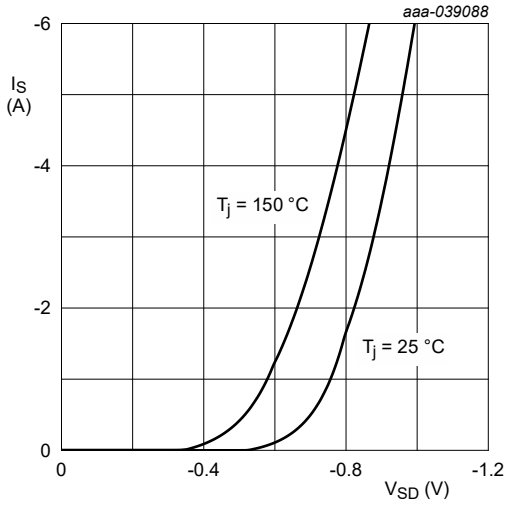


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

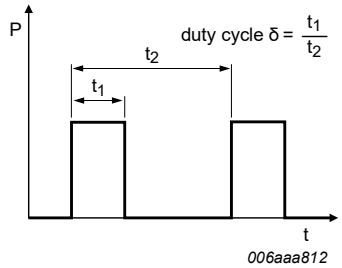


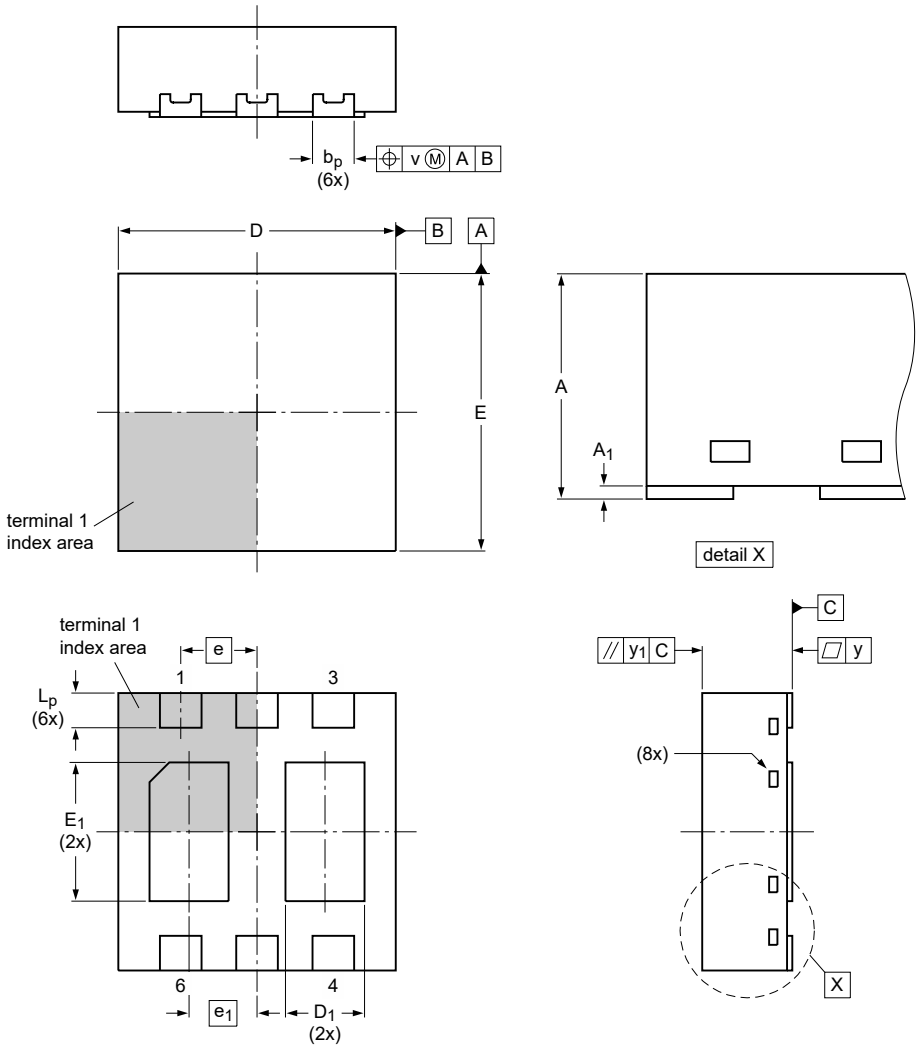
Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

HUSON6: plastic, thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm **SOT1118**



Dimensions

Unit		$A^{(1)}$	A_1	b_p	D	D_1	E	E_1	e	e_1	L_p	v	y	y_1
mm	max	0.65	0.04	0.35	2.1	0.77	2.1	1.1		0.54	0.3			
	nom								0.65			0.1	0.05	0.05
	min			0.25	1.9	0.57	1.9	0.9		0.44	0.2			

Note
1. Dimension including plating thickness.

sot1118_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1118		---				~~10-08-16~~ 13-06-06

Fig. 18. Package outline DFN2020-6 (SOT1118)

13. Soldering

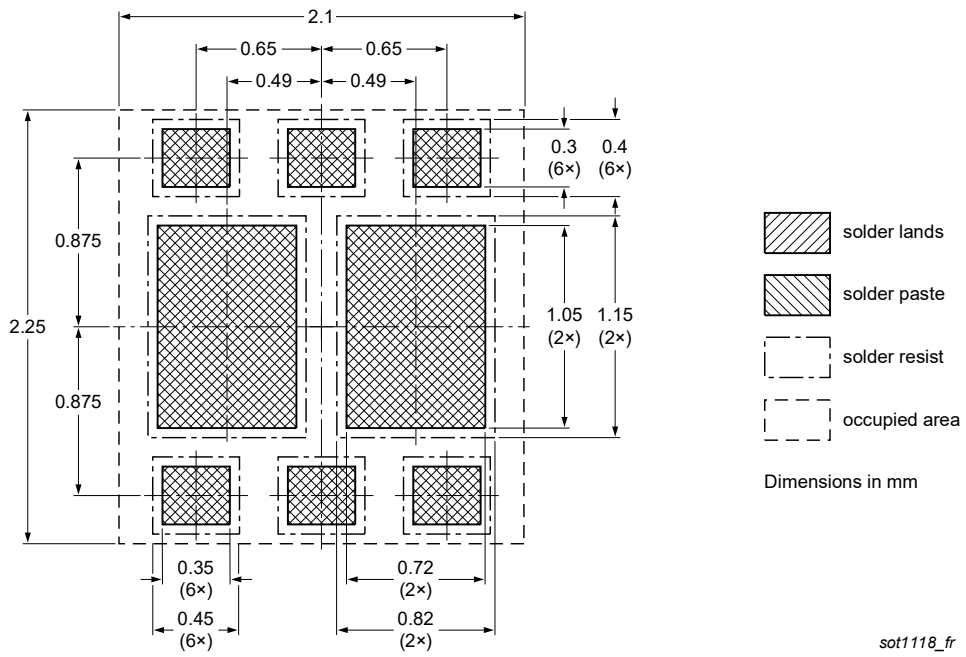


Fig. 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB55XPA v.1	20240318	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 18 March 2024