User's Guide
SLVU325–August 2009

TPS727xxDSEEVM-406

This User's Guide describes the characteristics, operation, and use of the TPS727xxDSEEVM-406. This EVM demonstrates the Texas Instruments TPS727xx, a Low Drop Out (LDO) linear regulator in a 1,5 × 1,5mm SON-6 package that is capable of 200mA of output current. This user's guide includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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1 Introduction

The TPS727xxDSEEVM-406 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS727xx LDO in the 1,5 × 1,5mm SON-6 package. The TPS727xx is a 200mA, ultra-low Iq, fast transient response, linear regulator.

2 Setup

This chapter describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS727xxEVM.

2.1 Input / Output Connector Descriptions

2.1.1 J1 –VIN

This is the positive input supply voltage. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added between J1 and J3 if the supply leads are greater than six inches. An additional 47µF or greater capacitor improves the transient response of the TPS727xx and helps to reduce ringing on the input when long supply wires are used.

2.1.2 J3 – VOUT

This is the positive connection from the output. Connect this pin to the positive input of the load.

2.1.3 J2 – GND

This is the return connection for the input power supply of the regulator.

2.1.4 J4 – GND

This is the return connection for the output.

2.1.5 JP1 – ENABLE

This jumper is used to enable or disable the output of the TPS727xx. Placing a shorting jumper between pins 1 and 2 (‘ON’ position) will enable the TPS727xx. Placing the shorting jumper between pins 2 and 3 (‘OFF’ position) will disable the TPS727xx.

3 Operation

This chapter provides information about the operation of the TPS727xxEVM.

3.1 Operation

Connect the positive input power supply to J1. Connect the input power return (ground) to J2. The TPS727xxEVM has an absolute maximum input voltage of 6.0V. The recommended maximum operating voltage is 5.5V. The actual highest input voltage may be less than 5.5V due to thermal conditions. See the Thermal Considerations section of this manual to determine if the highest input voltage.

Connect the desired load between J3 (positive lead) and J4 (negative or return lead). Configure jumper J6 for the desired output voltage.

4 Thermal Guidelines

This chapter provides guidelines for the thermal management of the TPS727xxDSEEVM-406 board.

4.1 Thermal Considerations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. To better help you design the TPS727xx family into your application, the following formula should be used to approximate the maximum power dissipation at a particular ambient temperature:

$$T_J = T_A + P_d \times \theta_{JA} \quad (1)$$

Where

T_J is the junction temperature,
T_A is the ambient temperature,
P_d is the power dissipation in the IC and
θ_{JA} is the thermal resistance from junction to ambient.
All temperatures are in degrees Celsius.

The measured thermal resistance from junction to ambient for the TPS727xxEVM has a typically value of 130°C/W. The recommended maximum operating junction temperature specified in the datasheet for the TPS727xx family is 125°C. With these two pieces of information, the maximum power dissipation can be found by using Equation 1.

Example Calculation:

For example, what is the maximum input voltage that can be applied to a TPS727xx with a 1.5V output voltage if the ambient temperature is 85°C and the full 200mA of load current is required?

Given: $T_J = 125°C$, $T_A = 85°C$, $\theta_{JA} = 130°C/W$

Using Equation 1, we substitute in the given values above and find that the maximum power dissipation for the part is $P_d = 0.307W$.

$$125°C = 85°C + P_d\ (130°C/W) \quad (2)$$

This means that the total power dissipation of the TPS727xx must be less than 0.833W. Now the input voltage can be calculated.

$$P_d = (V_{in} - V_{out}) \times I_{out} = (Vin - 1.5V) \times 0.2A = 0.307W \quad (3)$$

So the maximum input voltage would need to be 3.04V or less in order to maintain a safe junction temperature.

Similar analysis can be performed to determine the maximum input voltage at room temperature (25°C) or 85°C to provide full output current while maintaining the junction temperature at or below 125°C. The answer will depend on the output voltage.

	Ambient	Temperature
VOUT	**25°C**	**85°C**
1.5	5.35	3.04
1.8	5.50 (1)	3.34
2.8	5.50 (1)	4.34

(1) limited by recommended operating maximum, not thermal

5 Board Layout

This chapter provides the TPS727xxDSEEVM-406 board layout and illustrations.

5.1 Layout

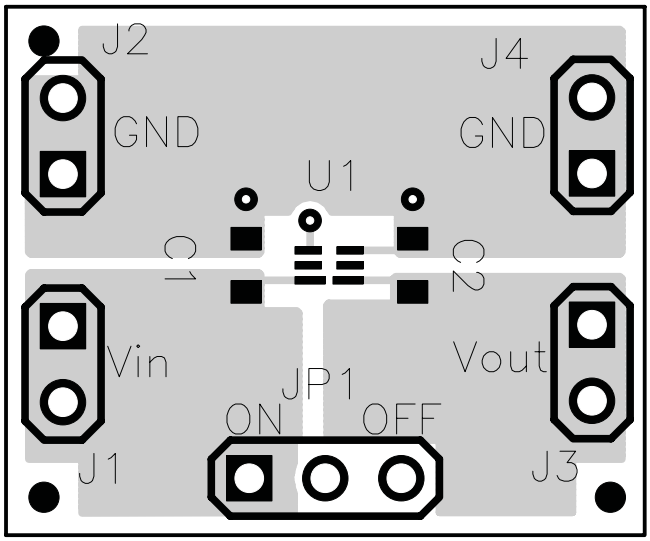


Figure 1. Top Layer Assembly

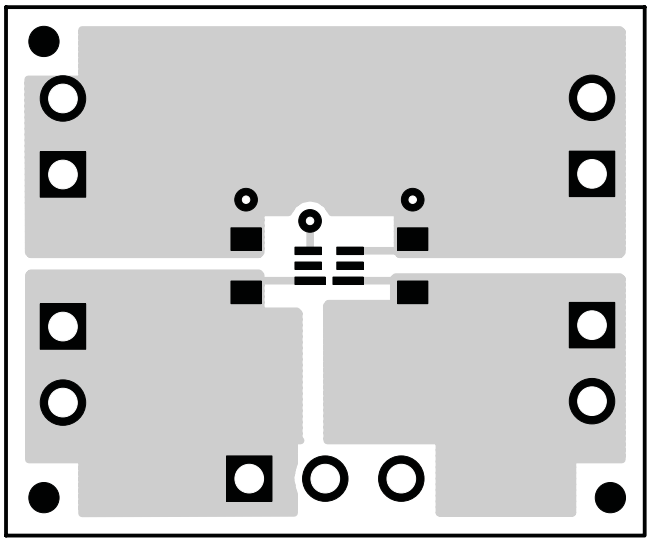


Figure 2. Top Layer Routing

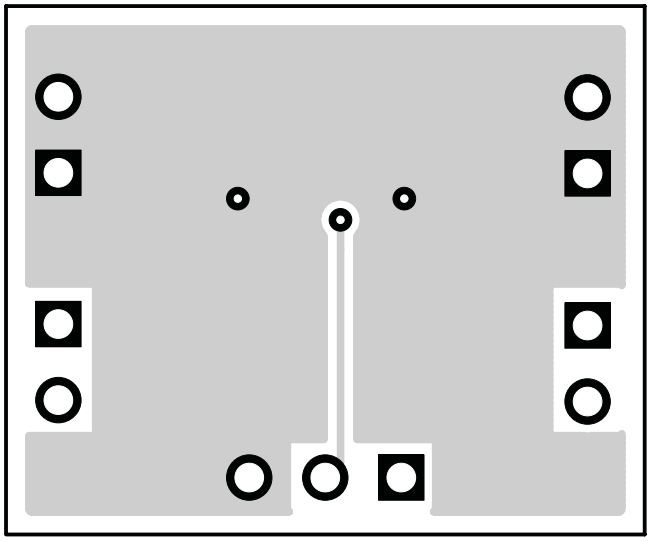


Figure 3. Bottom Layer Routing

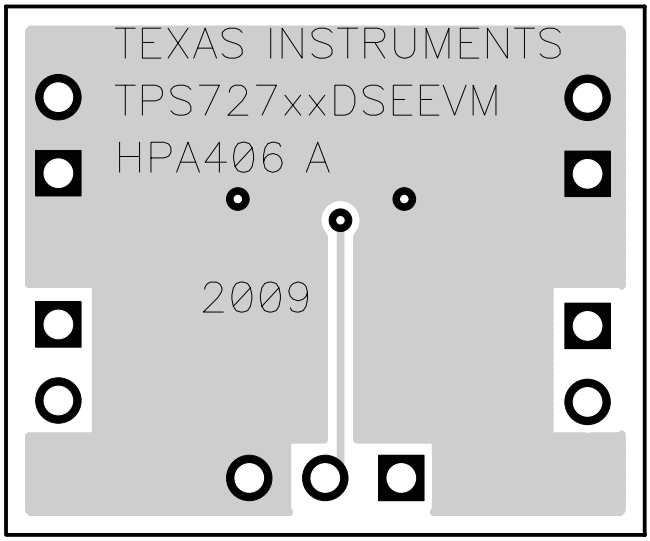
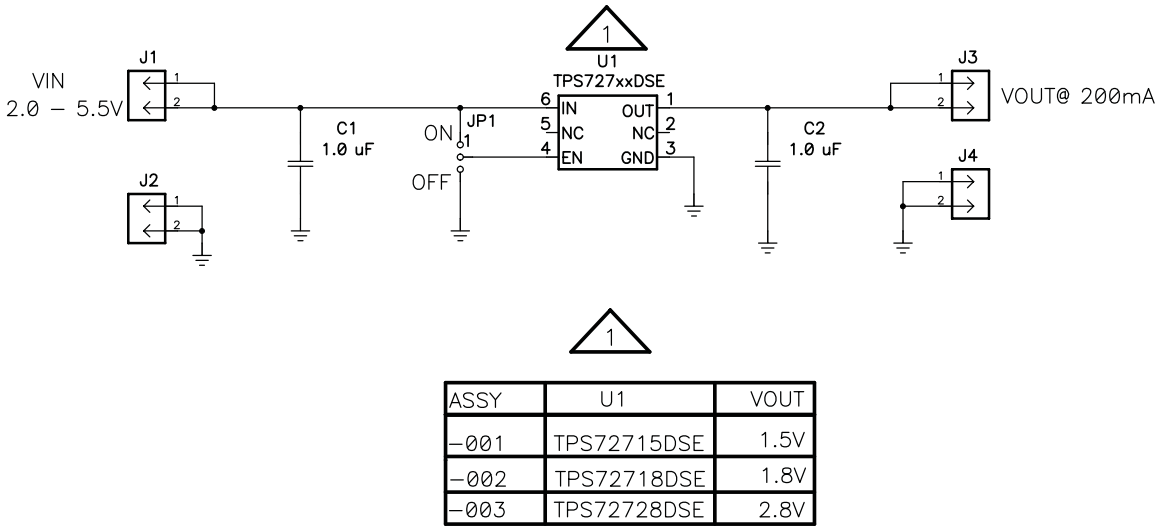


Figure 4. Bottom Layer Assembly

6 Schematic and Bill of Materials

This chapter provides the TPS727xxDSEEVM-406 schematic and bill of materials.

6.1 Schematic



1

ASSY	U1	VOUT
–001	TPS72715DSE	1.5V
–002	TPS72718DSE	1.8V
–003	TPS72728DSE	2.8V

Figure 5. TPS727xxDSEEVM-406 Schematic

6.2 Bill of Materials

Table 1. TPS727xxDSEEVM-406 BOM

-001	-002	-003	RefDes	Value	Description	Size	Part Number	MFR
2	2	2	C1, C2	1.0 µF	Capacitor, Ceramic, 6.3V, X5R, 20%.	0603	STD	Any
4	4	4	J1, J2, J3, J4	PEC02SAAN	Header, 2-pin, 100mil spacing	TH	PEC02SAAN	Sullins
1	1	1	JP1	PEC03SAAN	Header, 3-pin, 100mil spacing	TH	PEC03SAAN	Sullins
1	0	0	U1	TPS72715DSE	IC, 200mA Ultra-low IQ LDO with Auto-Low Power Mode	SON-6	TPS72715DSE	TI
0	1	0	U1	TPS72718DSE	IC, 200mA Ultra-low IQ LDO with Auto-Low Power Mode	SON-6	TPS72718DSE	TI
0	0	1	U1	TPS72728DSE	IC, 200mA Ultra-low IQ LDO with Auto-Low Power Mode	SON-6	TPS72728DSE	TI
1	1	1	N/A		PCB, FR-4, 4-Layer, SMOBC, 0.695" x 0.840" × 0.062"		HPA406**	Any
1	1	1	N/A		Shunt, Open-top		151-8000-E	Kobiconn

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.0 V to 5.5 V and the output voltage range of 0.9 V to 5.0 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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