

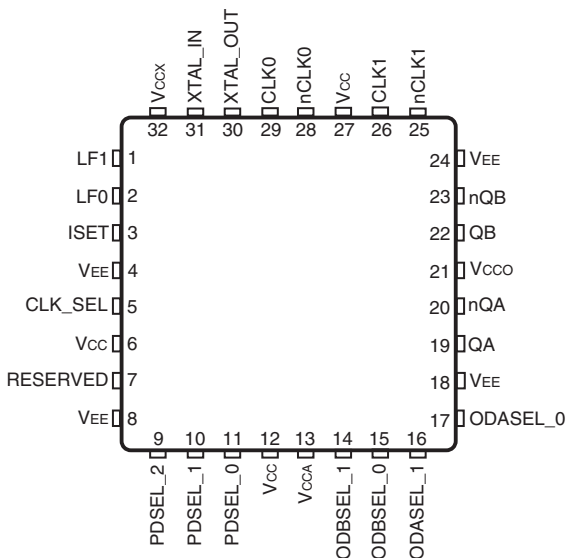
## General Description

The 813N252I-04 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock® NG frequency multiplier that provides the low jitter, high frequency Ethernet output clock that easily meets Gigabit and 10 Gigabit Ethernet jitter requirements. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The VCXO requires the use of an external, inexpensive pullable crystal. The VCXO uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics. The device is packaged in a space-saving 32-VFQFN package and supports industrial temperature range.

## Features

- Fourth generation FemtoClock® Next Generation (NG) technology
- One LVPECL output pair and one LVDS output pair  
Each output supports independent frequency selection at 25MHz, 125MHz, 156.25MHz and 312.5MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Accepts input frequencies from 8kHz to 155.52MHz including 8kHz, 1.544MHz, 2.048MHz, 19.44MHz, 25MHz, 77.76MHz, 125MHz and 155.52MHz
- Attenuates the phase jitter of the input clock by using a low-cost pullable fundamental mode VCXO crystal
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock NG frequency multiplier provides low jitter, high frequency output
- Absolute pull range: 100ppm
- FemtoClock NG VCO frequency: 625MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz – 20MHz): 0.3ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Pin Assignment



**813N252I-04**

**32 Lead VFQFN**

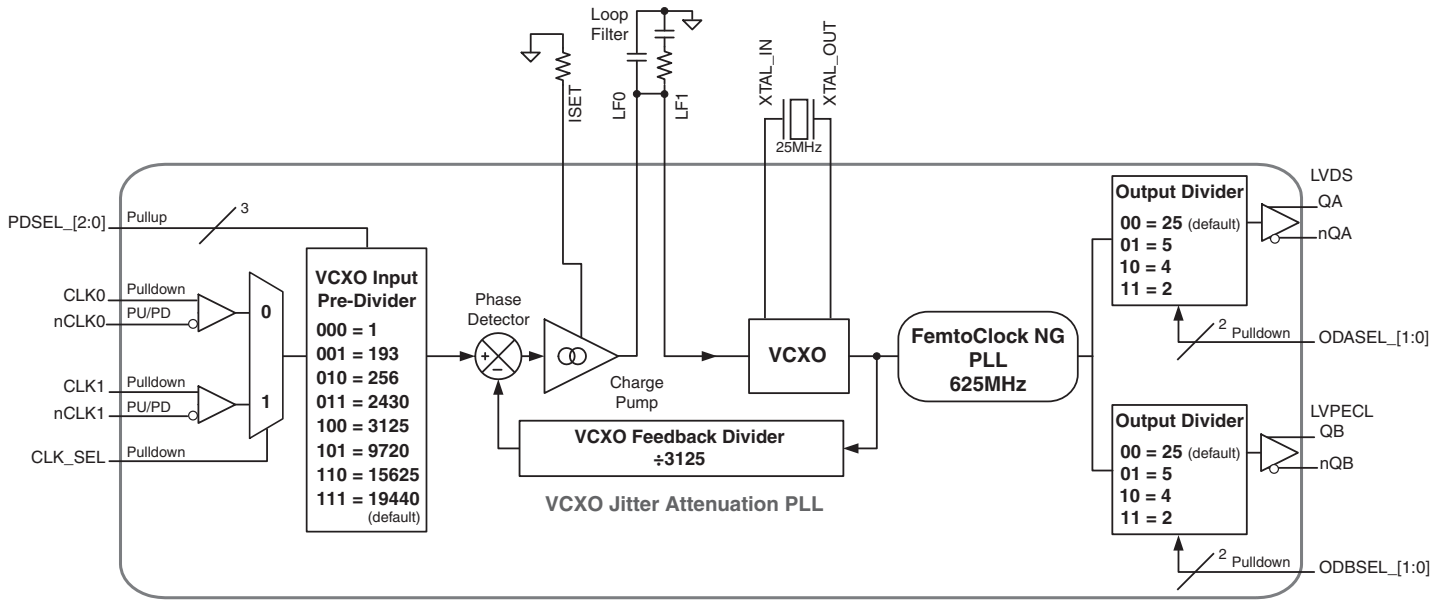
**5mm x 5mm x 0.925mm package body**

**3.15mm x 3.15mm EPad**

**K Package**

**Top View**

# Block Diagram



## Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins. LF0 is the output. LF1 is the input.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 8, 18, 24	V <sub>EE</sub>	Power		Negative supply pins.
5	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS / LVTTTL interface levels.
6, 12, 27	V <sub>CC</sub>	Power		Core supply pins.
7	RESERVED	Reserved		Reserve pin. Do not connect.
9, 10, 11	PDSEL_2, PDSEL_1, PDSEL_0	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTTL interface levels. See Table 3A.
13	V <sub>CCA</sub>	Power		Analog supply pin.
14, 15	ODBSEL_1, ODBSEL_0	Input	Pulldown	Frequency select pins for QB, nQB outputs. See Table 3B. LVCMOS/LVTTTL interface levels.
16, 17	ODASEL_1, ODASEL_0	Input	Pulldown	Frequency select pins for QA, nQA outputs. See Table 3B. LVCMOS/LVTTTL interface levels.
19, 20	QA, nQA	Output		Differential clock outputs. LVDS interface levels.
21	V <sub>CCO</sub>	Power		Output supply pin.
22, 23	QB, nQB	Output		Differential clock outputs. LVPECL interface levels.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
28	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 bias voltage when left floating.
29	CLK0	Input	Pulldown	Non-inverting differential clock input.
30, 31	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
32	V <sub>CCX</sub>	Power		Power supply pin for the XTAL oscillator regulator.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Tables

**Table 3A. Pre-Divider Selection Function Table**

Inputs			Pre-Divider Value
PDSEL_2	PDSEL_1	PDSEL_0	
0	0	0	1
0	0	1	193
0	1	0	256
0	1	1	2430
1	0	0	3125
1	0	1	9720
1	1	0	15625
1	1	1	19440 (default)

**Table 3B. Output Divider Function Table**

Inputs		Output Divider Value
ODxSEL_1	ODxSEL_0	
0	0	25 (default)
0	1	5
1	0	4
1	1	2

**Table 3C. CLK\_SEL Function Table**

Input	Selected Input
CLK_SEL	
0	CLK0, nCLK0
1	CLK1, nCLK1

**Table 3D. Frequency Function Table**

Input Frequency (MHz)	Pre-Divider Value	VCXO Frequency (MHz)	FemtoClock Feedback Divider Value	FemtoClock VCO Frequency (MHz)	Output Divider Value	Output Frequency (MHz)
0.008	1	25	25	625	25	25
0.008	1	25	25	625	5	125
0.008	1	25	25	625	4	156.25
0.008	1	25	25	625	2	312.5
1.544	193	25	25	625	25	25
1.544	193	25	25	625	5	125
1.544	193	25	25	625	4	156.25
1.544	193	25	25	625	2	312.5
2.048	256	25	25	625	25	25
2.048	256	25	25	625	5	125
2.048	256	25	25	625	4	156.25
2.048	256	25	25	625	2	312.5
19.44	2430	25	25	625	25	25
19.44	2430	25	25	625	5	125
19.44	2430	25	25	625	4	156.25
19.44	2430	25	25	625	2	312.5
25	3125	25	25	625	25	25
25	3125	25	25	625	5	125
25	3125	25	25	625	4	156.25
25	3125	25	25	625	2	312.5
77.76	9720	25	25	625	25	25
77.76	9720	25	25	625	5	125
77.76	9720	25	25	625	4	156.25
77.76	9720	25	25	625	2	312.5
125	15625	25	25	625	25	25
125	15625	25	25	625	5	125
125	15625	25	25	625	4	156.25
125	15625	25	25	625	2	312.5
155.52	19440	25	25	625	25	25
155.52	19440	25	25	625	5	125
155.52	19440	25	25	625	4	156.25
155.52	19440	25	25	625	2	312.5

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	3.63V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	37°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.20$	3.3	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$V_{CCX}$	Charge Pump Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				225	mA
$I_{CCA}$	Analog Supply Current				20	mA
$I_{CCX}$	Charge Pump Supply Current				20	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		PDSEL_[0:2]	$V_{CC} = V_{IN} = 3.465V$		10	$\mu A$
$I_{IL}$	Input Low Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	$V_{CC} = 3.465V, V_{IN} = 0V$	-10		$\mu A$
		PDSEL_[0:2]	$V_{CC} = 3.465, V_{IN} = 0V$	-150		$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK0, nCLK0, CLK1, nCLK1 $V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1 $V_{CC} = 3.465V, V_{IN} = 0V$	-10			$\mu A$
		nCLK0, nCLK1 $V_{CC} = 3.465V, V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE}$		$V_{CC} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode voltage is defined at the cross point.

**Table 4D. LVPECL DC Characteristics,  $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.10$		$V_{CCO} - 0.75$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.60$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ . See Parameter Measurement Information section, *3.3V Output Load Test Circuit*.

**Table 4E. LVDS DC Characteristics,  $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				60	mV
$V_{OS}$	Offset Voltage		1.125		1.375	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	25MHz crystal Frequency	0.008		155.52	MHz
$f_{OUT}$	Output Frequency		25		312.5	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 1	$f_{OUT} = 125MHz, 156.25MHz, 312.5MHz,$ 25MHz crystal, Integration Range: 12kHz – 20MHz		0.3	0.7	ps
$f_{jit}(pk-pk)$	Peak-to-Peak Jitter	QA	1e -12BER		60	ps
		QB	1e -12BER		25	ps
$t_{sk}(o)$	Output Skew; NOTE 2, 3				75	ps
$t_R / t_F$	Output Rise/Fall Time	QA	20% to 80%	150	400	ps
		QB	20% to 80%	150	500	ps
odc	Output Duty Cycle		48		52	%
$t_{LOCK}$	PLL Lock Time			6		s

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized with outputs at the same frequency using the loop filter components for the mid loop bandwidth. Refer to VCXO-PLL Loop Bandwidth Selection Table.

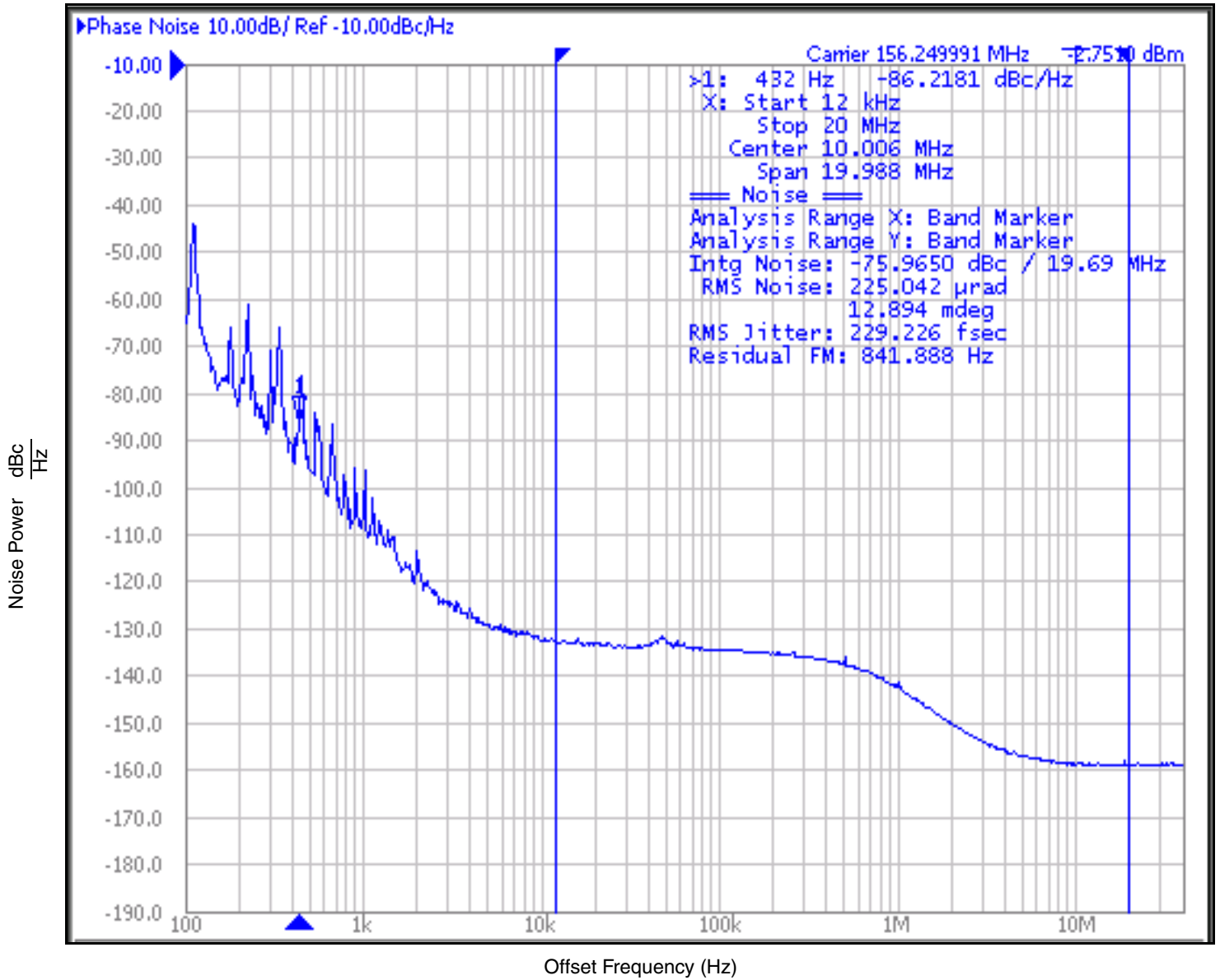
NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

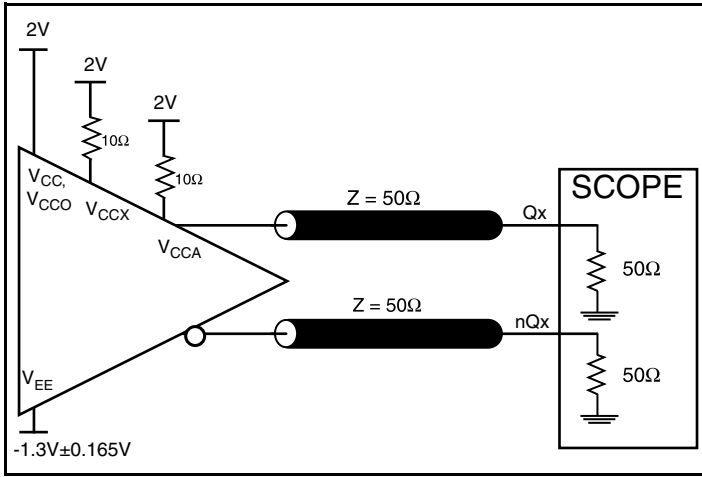
NOTE 3: Defined as skew between outputs at the same supply voltage. Measured at the output differential cross points.



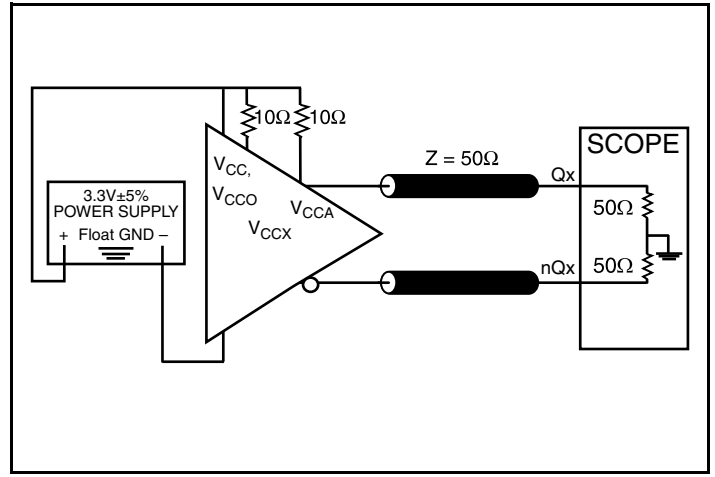
Typical Phase Noise



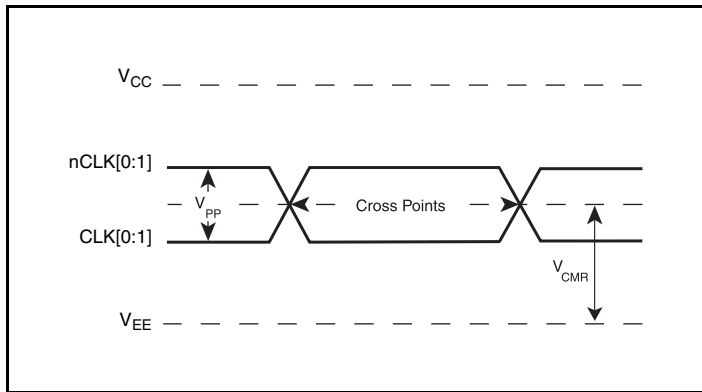
## Parameter Measurement Information



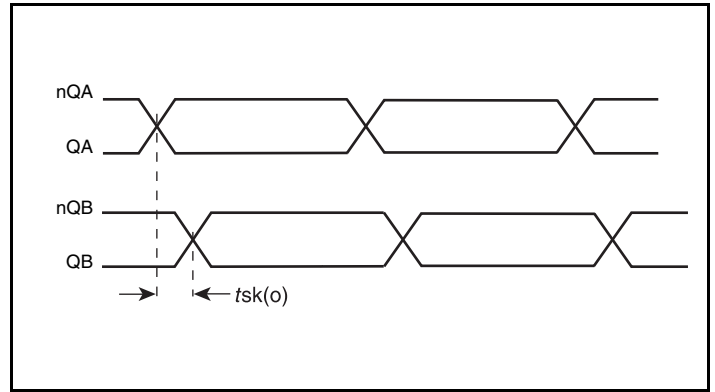
3.3V LVPECL Output Load Test Circuit



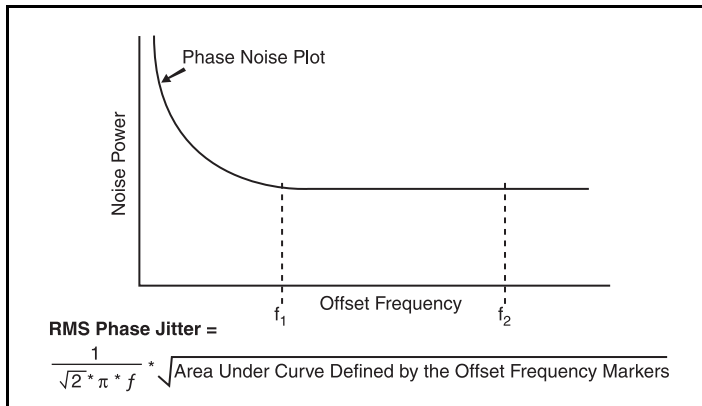
3.3V LVDS Output Load Test Circuit



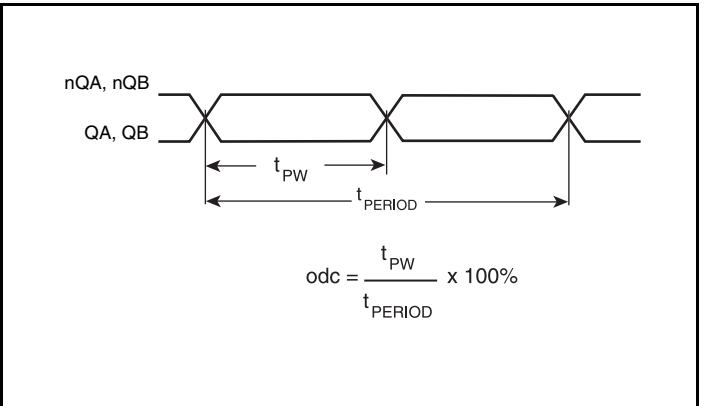
Differential Input Level



Output Skew

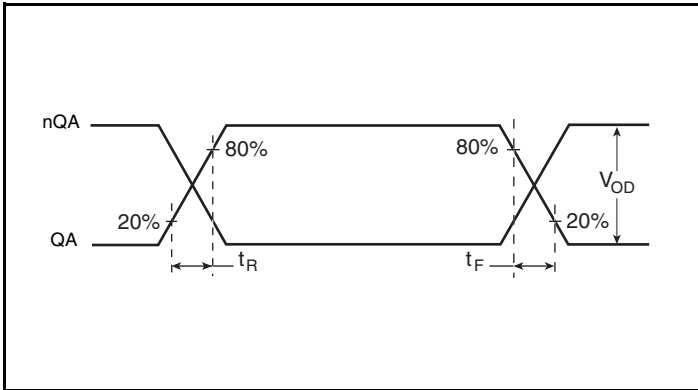


RMS Phase Jitter

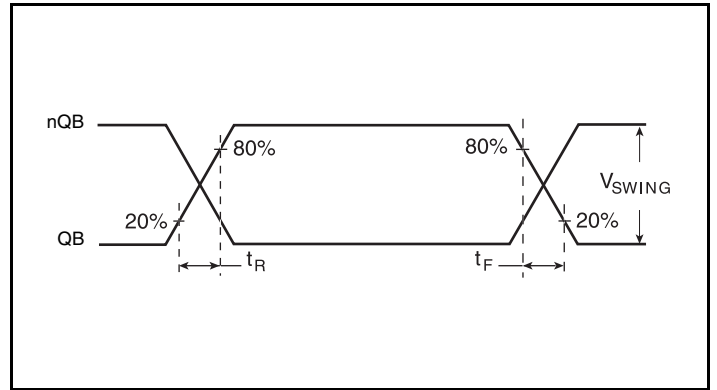


Output Duty Cycle/Pulse Width/Period

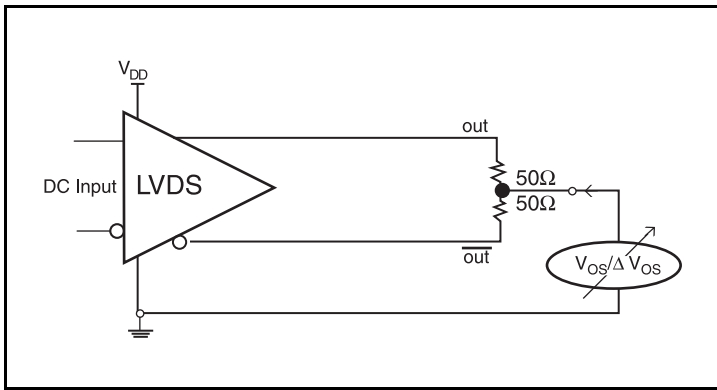
Parameter Measurement Information, continued



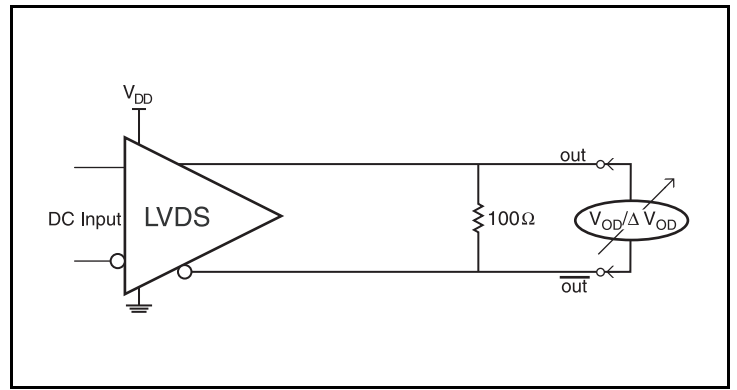
LVDS Output Rise/Fall Time



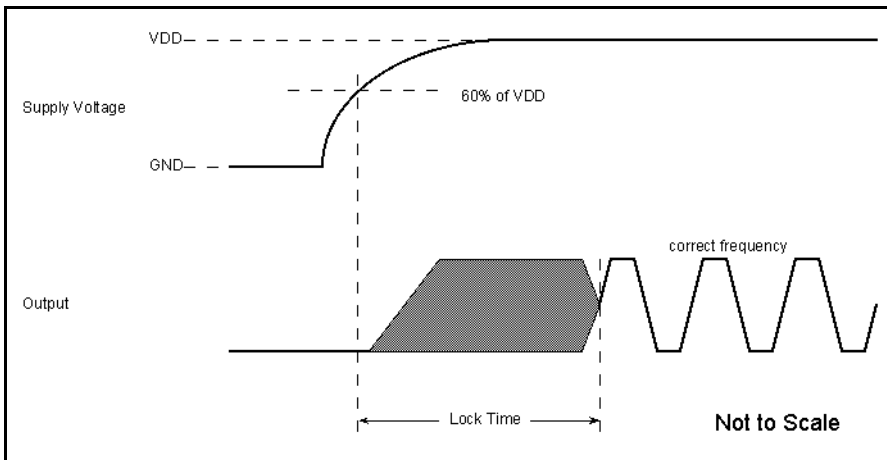
LVPECL Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup



VCXO & FemtoClock PLL Lock Time

## Applications Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 813N2521-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ ,  $V_{CCO}$  and  $V_{CCX}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin.

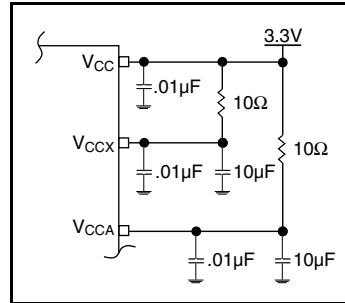


Figure 1. Power Supply Filtering

### Wiring the Differential Input to Accept Single-Ended Levels

*Figure 2* shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is  $2.5\text{V}$  and  $V_{CC} = 3.3\text{V}$ , R1 and R2 value should be adjusted to set  $V_1$  at  $1.25\text{V}$ . Similarly, if the input clock swing is  $1.8\text{V}$  and  $V_{CC} = 3.3\text{V}$ , R1 and R2 value should be adjusted to set  $V_1$  at  $0.9\text{V}$ . It is recommended to always use R1 and R2 to provide a known  $V_1$  voltage. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways.

First, R3 and R4 in parallel should equal the transmission line impedance. For most  $50\Omega$  applications, R3 and R4 can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3\text{V}$  and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3\text{V}$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

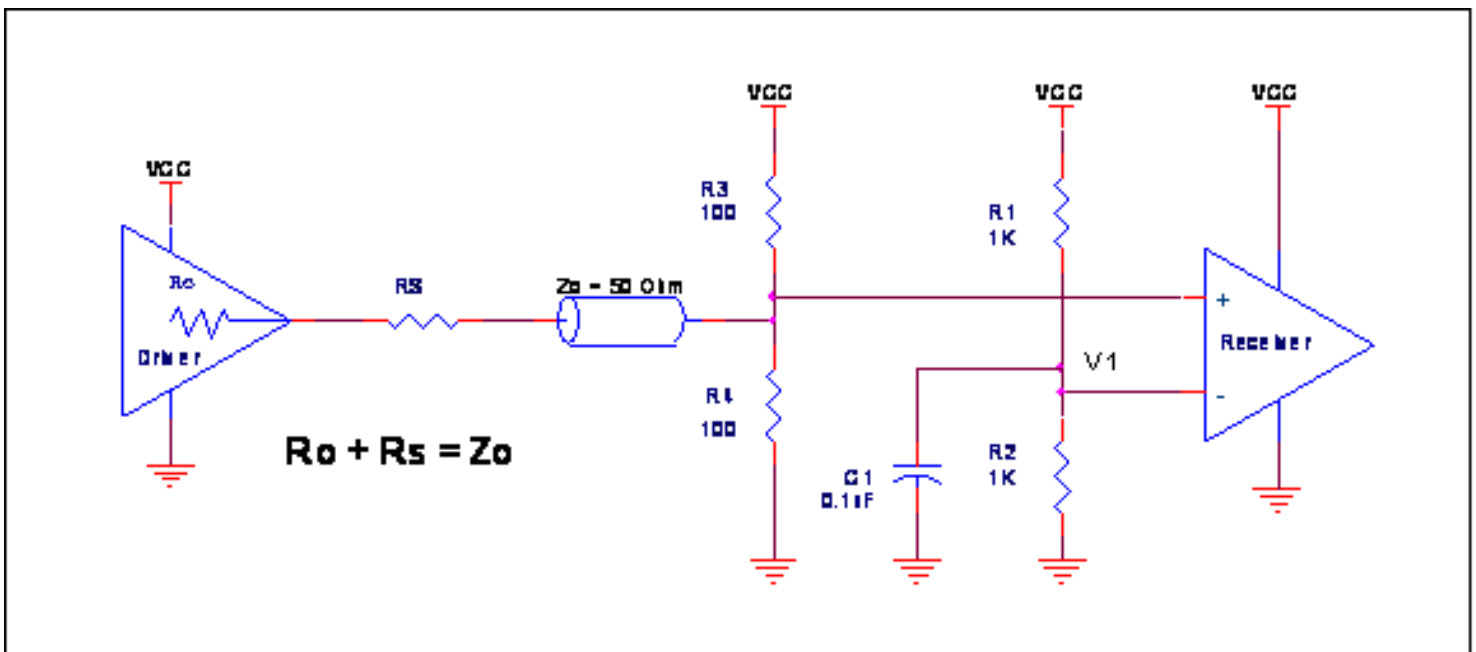


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

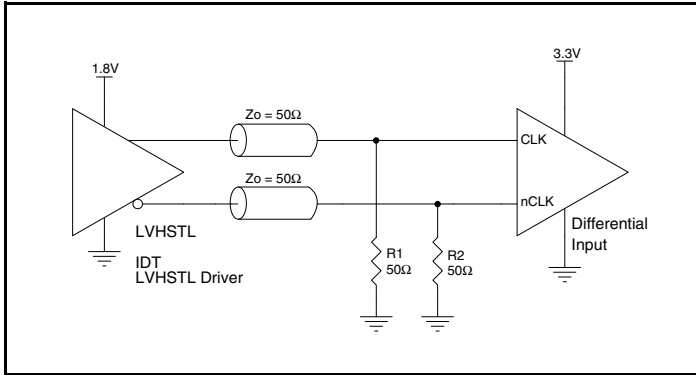


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

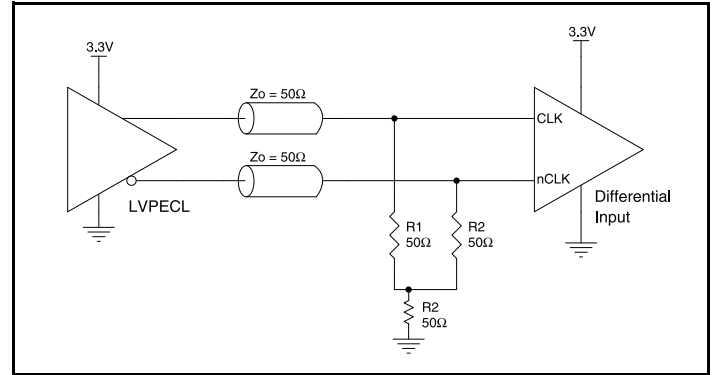


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

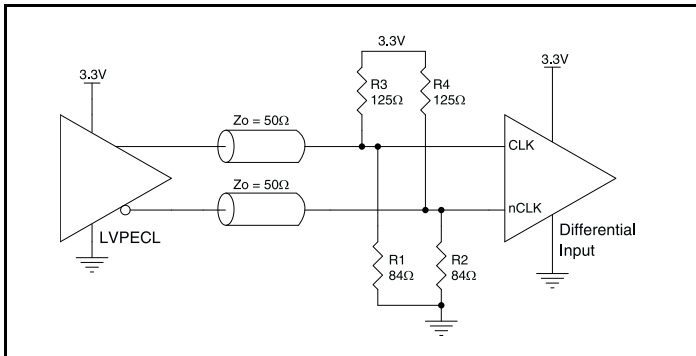


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

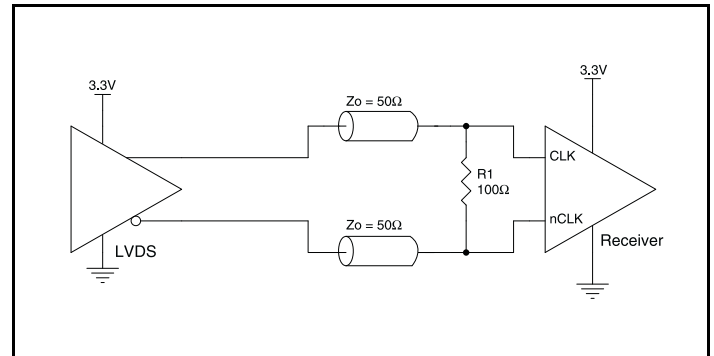


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

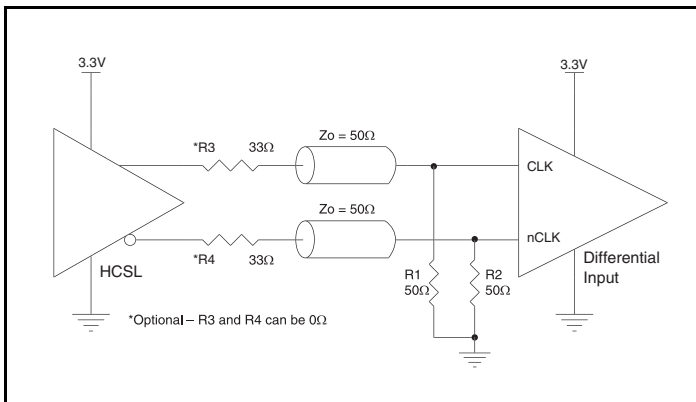


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

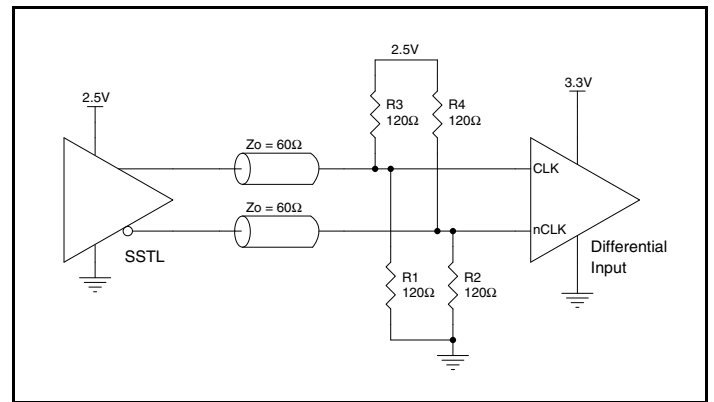


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

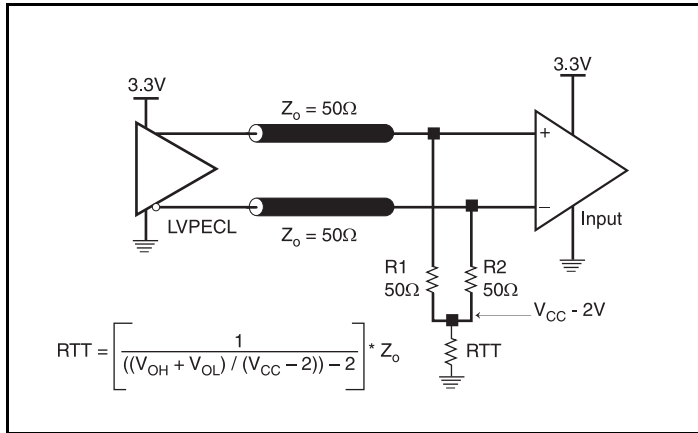


Figure 4A. 3.3V LVPECL Output Termination

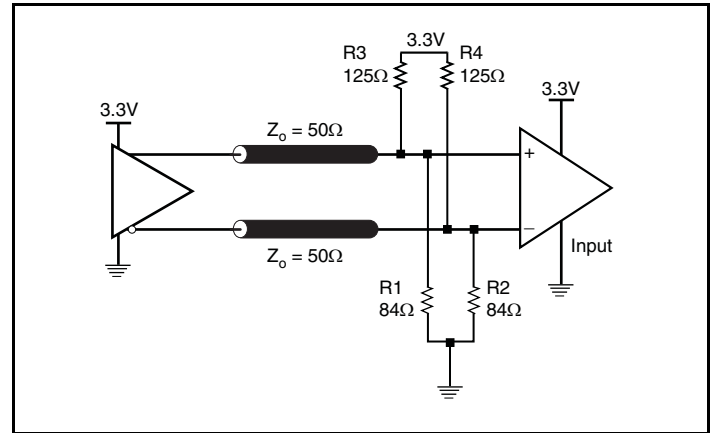
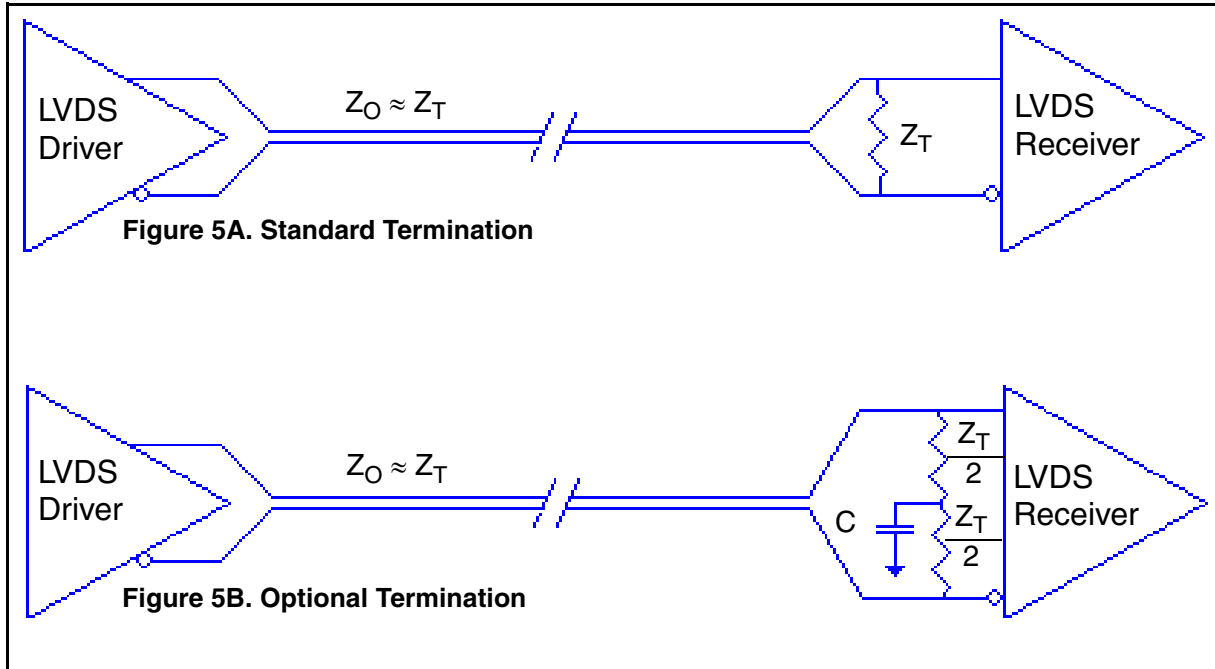


Figure 4B. 3.3V LVPECL Output Termination

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source type. The

standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



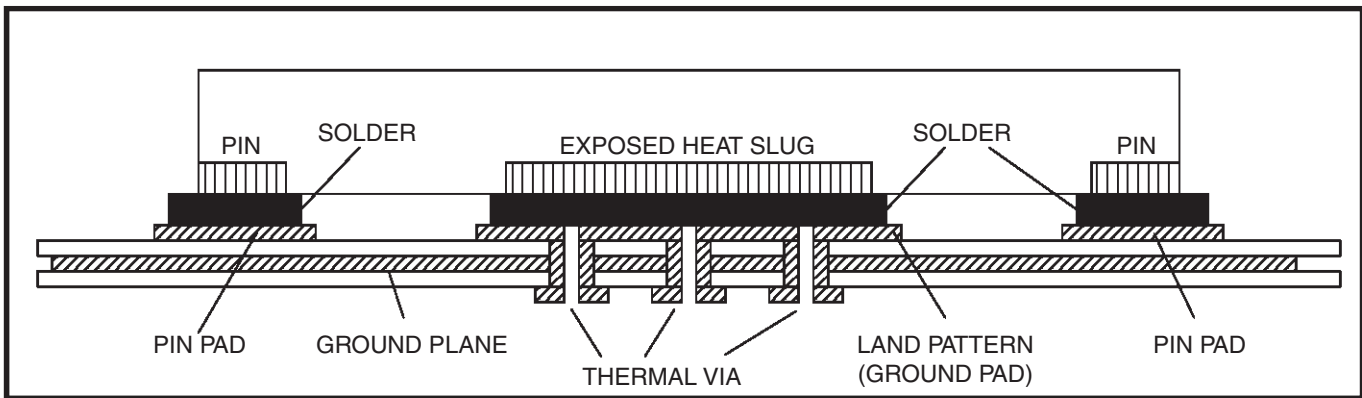
### LVDS Termination

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**



## Schematic Example

Figure 7 shows an example of 813N252I-04 application schematic. In this example, the device is operated at  $V_{CC} = V_{CCX} = V_{CCO} = 3.3V$ . The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. Two examples of LVPECL and one example of LVDS terminations are

shown in this schematic. An optional 3-pole filter can also be used for additional spur reduction. It is recommended that the loop filter components be laid out for the 3-pole option. This will also allow the 2-pole filter to be used.

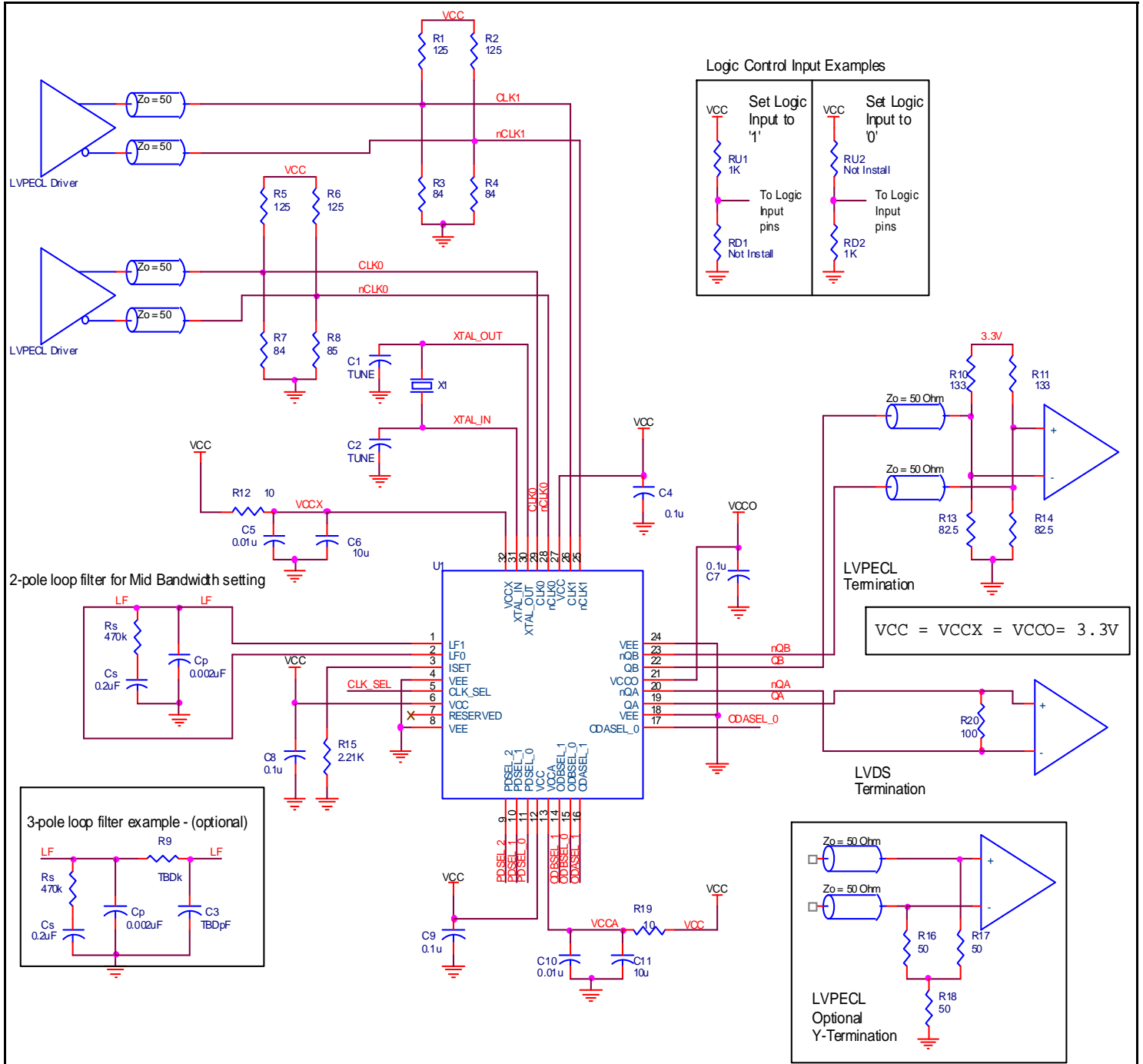


Figure 7. 813N252I-04 Schematic Example

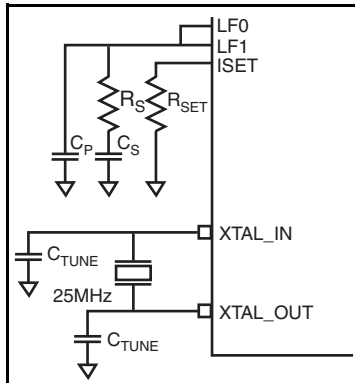
### VCXO-PLL EXTERNAL COMPONENTS

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance ( $C_L$ ). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note*.

The crystal's load capacitance ( $C_L$ ) characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors ( $C_{TUNE}$ ).

If the crystal  $C_L$  is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal ( $C_L$ ) is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of ( $C_L$ ) is dependant on the characteristics of the VCXO. The recommended ( $C_L$ ) in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The frequency of oscillation in the third overtone mode is not necessarily at exactly three times the fundamental frequency. The mechanical properties of the quartz element dictate the position of the overtones relative to the fundamental. The oscillator circuit may excite both the fundamental and overtone modes simultaneously. This will cause a nonlinearity in the tuning curve. This potential problem is why VCXO crystals are required to be tested for absence of any activity inside a  $\pm 200$  ppm window at three times the fundamental frequency. Refer to  $F_{L\_3OVT}$  and  $F_{L\_3OVT\_spurs}$  in the crystal Characteristics table.



The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.

### VCXO Characteristics Table

Symbol	Parameter	Typical	Units
$k_{VCXO}$	VCXO Gain	4.4	kHz/V
$C_{V\_LOW}$	Low Varactor Capacitance	8	pF
$C_{V\_HIGH}$	High Varactor Capacitance	16	pF

### VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	M	$R_S$ (k $\Omega$ )	$C_S$ ( $\mu$ F)	$C_P$ ( $\mu$ F)	$R_{SET}$ (k $\Omega$ )
8Hz (Low)	25	3125	680	0.20	0.002	22
20Hz (Mid)	25	3125	470	0.20	0.002	5
75Hz (High)	25	3125	680	0.02	0.0003	2.2

NOTE: When configuring the 813N252I-04 with PLL loop bandwidth less than 75Hz, it is recommended that CLK1, nCLK1 input be used as the only reference clock. In systems where both reference clocks are used, it is recommended to have PLL loop bandwidths of 75Hz or greater.

### Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation		Fundamental			
$f_N$	Frequency			25		MHz
$f_T$	Frequency Tolerance				±20	ppm
$f_S$	Frequency Stability				±20	ppm
	Operating Temperature Range		-40		85	°C
$C_L$	Load Capacitance			10		pF
$C_O$	Shunt Capacitance			4		pF
$C_O / C_1$	Pullability Ratio			220	240	
$F_{L\_3OVT}$	3 <sup>rd</sup> Overtone $F_L$		200			ppm
$F_{L\_3OVT\_spurs}$	3 <sup>rd</sup> Overtone $F_L$ Spurs		200			ppm
ESR	Equivalent Series Resistance				20	Ω
	Drive Level				1	mW
	Aging @ 25 °C	First Year			±3	ppm
		Ten Year			±10	ppm

## Power Considerations

This section provides information on power dissipation and junction temperature for the 813N252I-04. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 813N252I-04 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core\_LVDS)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 225mA = 779.625mW$
- Power (outputs)<sub>MAX</sub> = **31.55mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $779.625mW + 31.55mW = 811.175mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.811W * 37^\circ C/W = 115^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

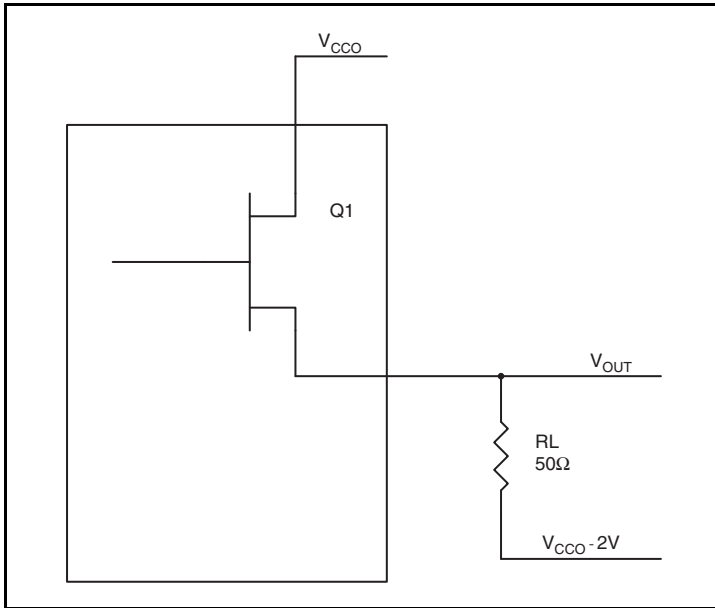
**Table 6. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 8*.



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V<sub>CCO</sub> - 2V.

- For logic high, V<sub>OUT</sub> = V<sub>OH\_MAX</sub> = V<sub>CCO\_MAX</sub> - 0.75V  
(V<sub>CCO\_MAX</sub> - V<sub>OH\_MAX</sub>) = 0.75V
- For logic low, V<sub>OUT</sub> = V<sub>OL\_MAX</sub> = V<sub>CCO\_MAX</sub> - 1.6V  
(V<sub>CCO\_MAX</sub> - V<sub>OL\_MAX</sub>) = 1.6V

Pd<sub>H</sub> is power dissipation when the output drives high.

Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.75V)/50\Omega] * 0.75V = \mathbf{18.75mW}$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.6V)/50\Omega] * 1.6V = \mathbf{12.80mW}$$

Total Power Dissipation per output pair = Pd<sub>H</sub> + Pd<sub>L</sub> = **31.55mW**

## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead VFQFN**

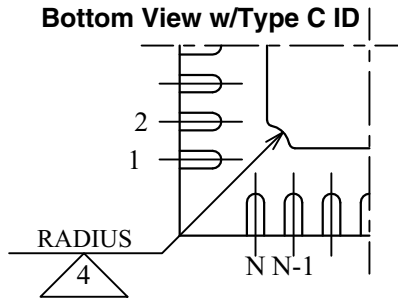
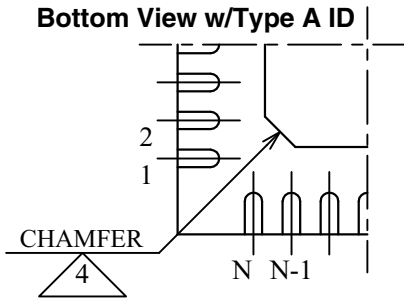
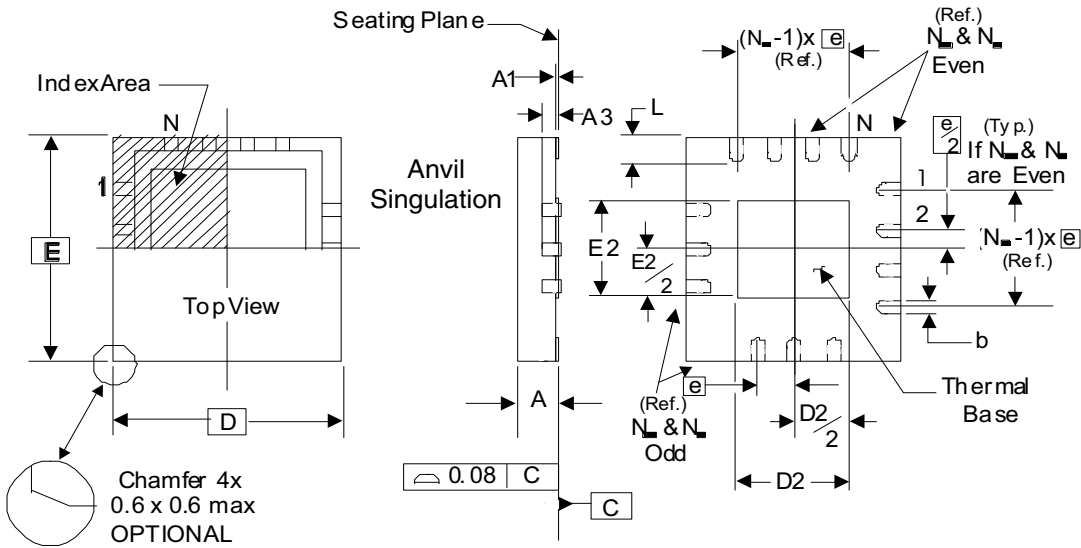
$\theta_{JA}$ vs. Air Flow			
Meters per Second	<b>0</b>	<b>1</b>	<b>2.5</b>
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29°C/W

## Transistor Count

The transistor count for 813N252I-04 is: 22,280

# Package Outline and Package Dimensions

## Package Outline - K Suffix for 32 Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:  
 1. Type A: Chamfer on the paddle (near pin 1)  
 2. Type C: Mouse bite on the paddle (near pin 1)

**Table 8. Package Dimensions**

JEDEC Variation: VHHD-2/-4			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A	0.80		1.00
A1	0		0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N <sub>D</sub> & N <sub>E</sub>			8
D & E	5.00 Basic		
D2 & E2	3.0		3.3
e	0.50 Basic		
L	0.30	0.40	0.50

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin out are shown on the front page. The package dimensions are in Table 8.

Reference Document: JEDEC Publication 95, MO-220

## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
813N252BKI-04LF	ICS252BI04L	"Lead-Free" 32 Lead VFQFN	Tray	-40°C to 85°C
813N252BKI-04LFT	ICS252BI04L	"Lead-Free" 32 Lead VFQFN	Tape & Reel	-40°C to 85°C



## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	4C	7	Differential DC Characteristics Table - redefined V <sub>CMR</sub> min. to standard levels as the crosspoint. Changed from 0.5V min. to V <sub>EE</sub> . Updated Notes.	3/18/10
	4D	7	LVPECL DC Characteristics Table - corrected V <sub>OH</sub> /V <sub>OL</sub> Parameter verbiage from Current to Voltage and corrected units to "V".	
		12	Updated "Wiring the Differential Input to Accept Single-ended Levels".	
A		6	Supply Voltage, V <sub>CC</sub> . Rating changed from 4.5V min. to 3.63V per Errata NEN-11-03.	5/24/11
B			Per PCN #N1210-01 changed revision marking from "A" to "B" in page footer and ordering information table.	1/18/13
		11	Parameter Measurement Information Section - added LockTime diagram.	
		12	Updated <i>Wiring the Differential Input to Accept Single-ended Levels</i> Application Note.	
		15	Updated <i>LVDS Driver Termination</i> Application Note.	
		18	VCXO-PLL External Components: VCXO-PLL Loop Bandwidth Selection Table - added note. Crystal Characteristics - added "Ten Year" spec to <i>Aging</i> row.	
		22	Updated Package Outline.	
	T9	23	Ordering Information Table - changed revision marking from "A" to "B"; deleted Tape & Reel Count; deleted note.	
C			Updated header/footer. Deleted "ICS" prefix from part number.	12/11/15



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