NSE11409-Q1

1CH, 90mΩ, 40V, Fully Protected Automotive Low-side Switch

Datasheet (EN) 1.0

Product Overview

NSE11409-Q1 is a 90mΩ low-side switch with 48V clamp voltage for automotive applications. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnostic function is built to indicate any faults when thermal shutdown and open-drain conditions through an open-drain status output pin. This device operates in ambient temperatures from –40°C to 125°C.

Key Features

- AEC-Q100 Qualified
- Drain current limitation: 8.5A
- 48V overvoltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block:
  - Thermal shutdown diagnosis
  - Open-drain diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection
- RoHS-compliant package

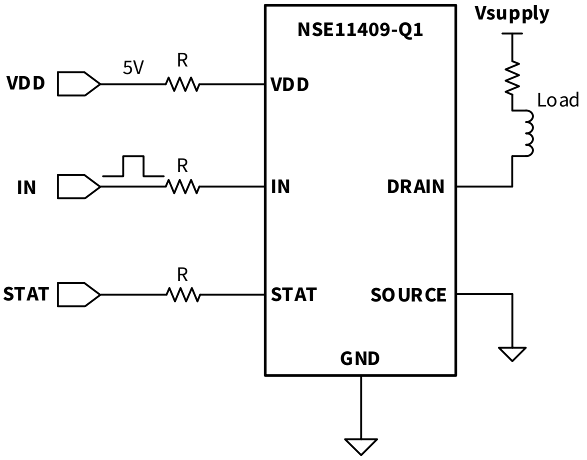
Applications

- Automotive Relays
- Solenoids
- Valves
- Lighting

Device Information

Part Number	*Package*	*Body Size*
NSE11409-QSPR	SOP8	4.9mm x 3.9mm
NSE11409-QSTBR	SOT223	6.48mm x 3.38mm

Typical Application



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1. Pin Configuration and Functions

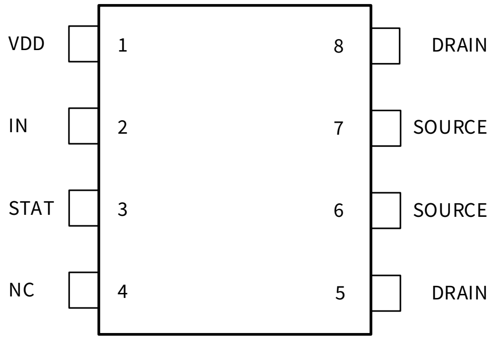


Figure 1 NSE11409-QSPR Pin-out

PIN NO.	SYMBOL	FUNCTION
1	VDD	Power supply pin.
2	IN	CMOS compatible, voltage controlled input pin.
3	STAT	Open drain digital diagnostic pin.
4	NC	Not connect.
5, 8	DRAIN	PowerMOS drain.
6, 7	SOURCE	PowerMOS source.

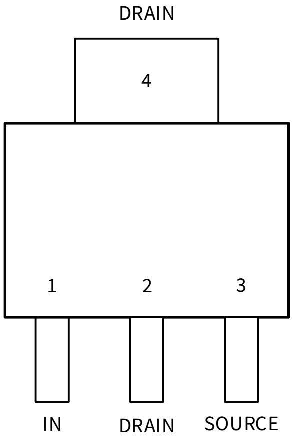


Figure 2 NSE11409-QSTBR Pin-out

PIN NO.	SYMBOL	FUNCTION
1	IN	CMOS compatible, voltage controlled input pin.
2, 4	DRAIN	PowerMOS drain.
3	SOURCE	PowerMOS source.

2. Block diagram

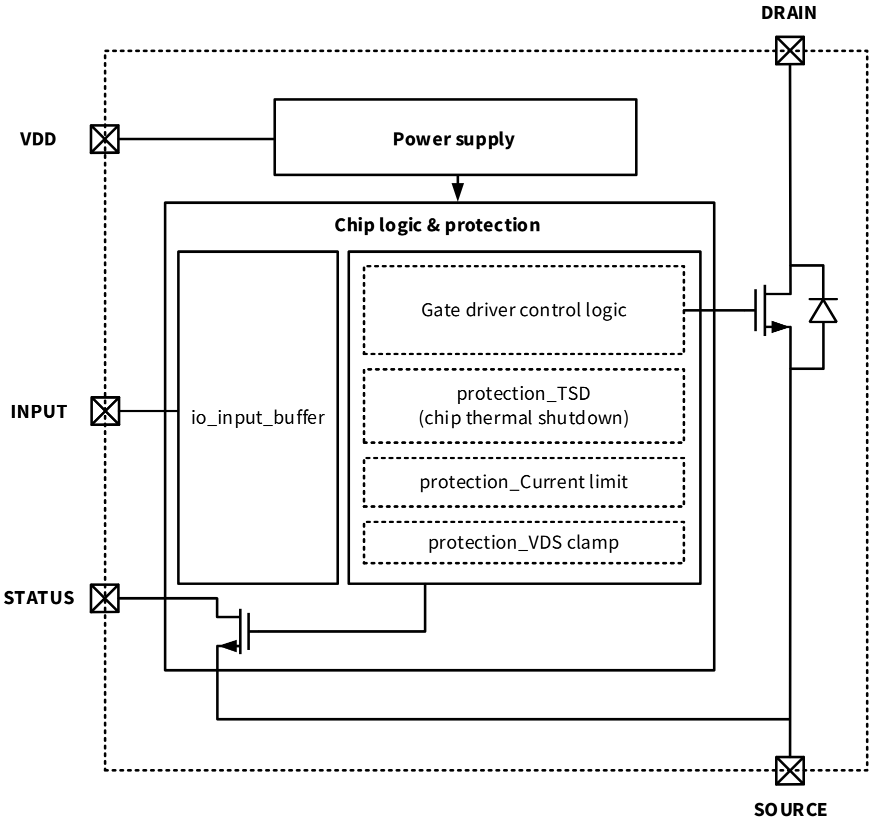


Figure 3 Block diagram

3. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Drain-to-Source Voltage	V_{DS}			Internally clamped	V
DC Drain Current	I_D			Thermal limited	A
Reverse DC drain current	$-I_D$			12.5	A
VDD Pin Current	I_{VDD}	-1		10	mA
INPUT Pin Current	I_{IN}	-1		10	mA
STATUS Pin Current	I_{STAT}	-1		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C
Single pulse avalanche energy (L=90mH, IDS=1.5A, VCC=13.5V)	E_{as}		73(1)		mJ

(1) Not subject to production test, bench evaluation.

4. ESD Ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002-RevD	±3000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	±2000	V

5. Thermal Information

Parameters	Symbol	SOP8	SOT223	Unit
IC Junction-to-ambient Thermal Resistance(1)	θ_{JA}	94.5	73	°C/W

(1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layer board.

6. Specifications

6.1. Electrical Characteristics

$V_{DD} = V_{IN} = 4.5$ V to 5.5 V, $T_A = -40$ °C to 125 °C. Unless otherwise noted, typical value is at $T_A = 25$ °C.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power MOSFET						
ON-state resistance	R_{ON}		90	180	mΩ	$I_D = 1.6$ A; $V_{DD} = V_{IN} = 5$ V
Drain-source clamp voltage	V_{CLAMP}	46	48	56	V	$V_{IN} = 0$V; $I_D = 1.6$ A
Drain-source clamp threshold voltage	V_{CLTH}	40			V	$V_{IN} = 0$V; $I_D = 2$ mA
OFF-state output current	I_{DSS}	0		3	µA	$V_{IN} = 0$ V; $V_{DS} = 13$ V; $T_j = 25$°C
		0		5	µA	$V_{IN} = 0$ V; $V_{DS} = 13$ V; $T_j = 125$°C
Bode diode forward voltage	V_{BD}		0.8		V	$I_D = 1.6$ A; $V_{IN} = 0$ V
VDD (NSE11409-QSTBR supplied by pin IN)						
Operating supply voltage	V_S	3.5	5	5.5	V	
Operating supply current	I_S		10	25	µA	OFF-state; $T_j = 25$°C; $V_{IN} = V_{DS} = 0$ V;
			25	65		ON-state; $V_{IN} = 5$ V; $V_{DS} = 0$ V
Supply clamp voltage	V_{SCL}	5.5		8	V	$I_{SCL} = 1$ mA
			-0.7			$I_{SCL} = -1$ mA
Logic Input (NSE11409-QSPR only)						
Low-level input voltage	V_{IL}			0.9	V	
Low-level input current	I_{IL}	1			µA	$V_{IN} = 0.9$ V
High-level input voltage	V_{IH}	2.1			V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
High-level input current	I_{IH}			10	µA	V_{IN} = 2.1 V
Input hysteresis voltage	$V_{I\,(hyst)}$	0.13			V	
Input clamp voltage	V_{ICL}	5.5		8		I_{IN} = 1 mA
			-0.7			I_{IN} = -1 mA
Status indicator (NSE11409-QSPR only)						
Status low output voltage	V_{STAT}			0.5	V	I_{STAT} = 1 mA
Status leakage current	I_{LSTAT}			10	µA	V_{STAT} = 5 V
Status pin input capacitance	C_{STAT}			100	pF	V_{STAT} = 5 V
Status clamp voltage	V_{STCT}	5.5		8	V	I_{STAT} = 1 mA
			-0.7			I_{STAT} = - 1 mA
Open load detection (NSE11409-QSPR only)						
Open load OFF-state voltage detection threshold	V_{OI}	1.1	1.2	1.3	V	V_{IN} = 0 V
Delay between INPUT falling edge and STATUS falling edge in open load condition	$t_{d\,(STAT)}$		225		µs	I_{OUT} = 0 A
Switching characteristics (Vsupply = VIN = 3.5V to 5.5 V, See Figure 4 for Switching timing characteristics)						
Turn-on delay time	$t_{d\,(ON)}$		8		µs	R_L = 8.2 Ω; V_{CC} = 13 V
Turn-off delay time	$t_{d\,(OFF)}$		18		µs	R_L = 8.2 Ω; V_{CC} = 13 V
Rise time	t_r		10		µs	R_L = 8.2 Ω; V_{CC} = 13 V
Fall time	t_f		10		µs	R_L = 8.2 Ω; V_{CC} = 13 V
Switching energy losses at turn-on	W_{ON}		57		uJ	R_L = 8.2 Ω; V_{CC} = 13 V
Switching energy losses at turn-off	W_{OFF}		55		uJ	R_L = 8.2 Ω; V_{CC} = 13 V
Protection and diagnostics						
DC short-circuit current	I_{limH}	5.5	8.5	11.5	A	V_{DS} = 13 V; V_S = V_{IN} = 5V
Shutdown temperature	T_{TSD}	150	175	200	°C	
Reset temperature	T_R	T_{RS} + 1	T_{RS} + 5		°C	
Thermal reset of STATUS	T_{RS}	135			°C	
Thermal hysteresis (TTSD - TR)	T_{HYST}		7		°C	

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Dynamic temperature	ΔT_j		40		K	T_j = -40°C; V_{CC} = 13V
Dynamic temperature hysteresis	$\Delta T_{j(HYS)}$		15		K	

6.2. Typical Performance Characteristics

6.2.1. True table

Conditions	*Input*	*Drain*	*Status*
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Over-temperature limitation	L	H	H
	H	H	L
V_{DD} under-voltage	L	H	X
	H	H	X
Open-drain detection	L	L	L
	H	L	H

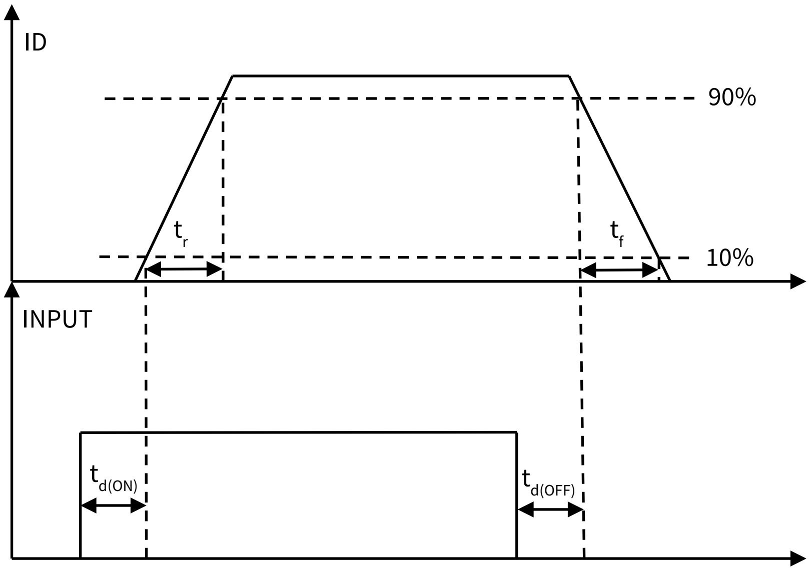


Figure 4 Switching characteristics

6.2.2. Electrical characteristics curves

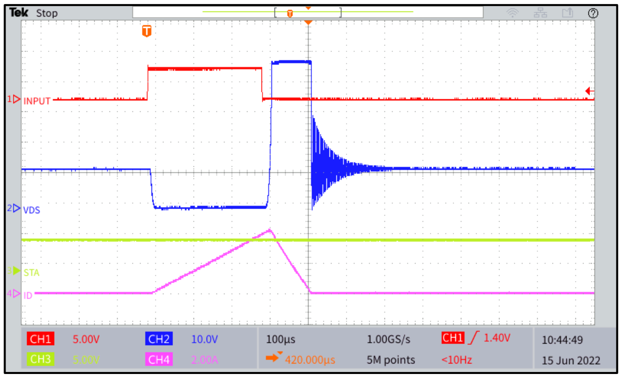


Figure 5 Inductive clamp voltage

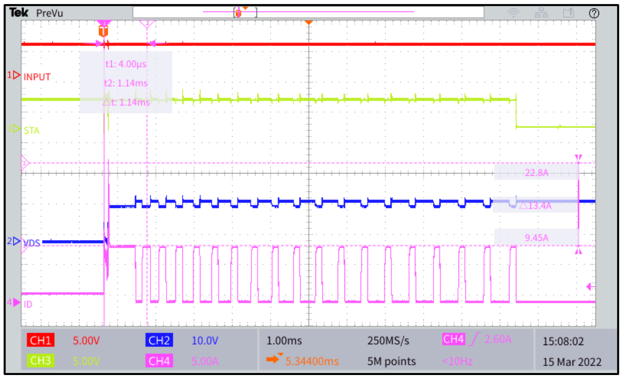


Figure 6 Thermal swing & current limitation

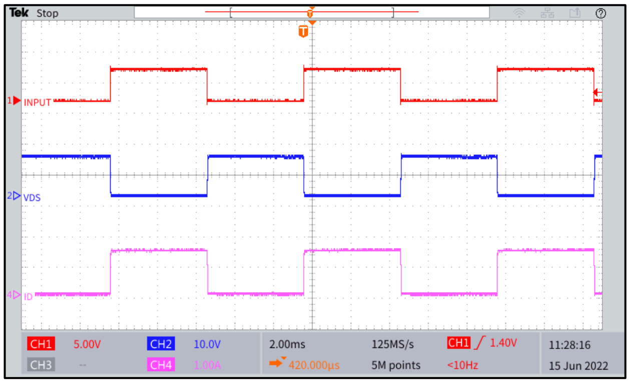


Figure 7 Normal load (1.5A, R_{load}, 25°C)

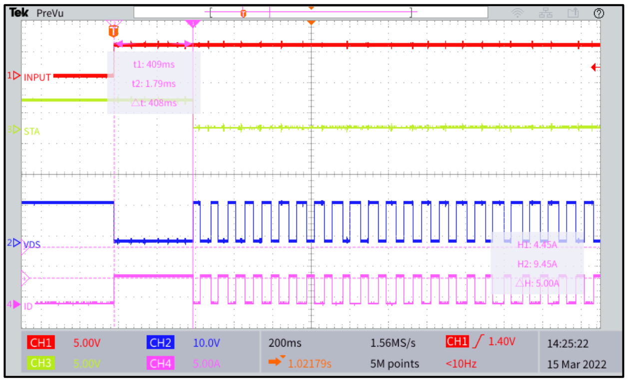


Figure 8 Thermal shutdown (5A, Rload, 85°C)

7. Protections

7.1. Current limitation

NSE11409-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to ground.

7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shutdown the MOSFET when the hottest junction temperature exceeds the T_{TSD}, and the dynamic temperature protection is also to shutdown the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔT_j.

8. Typical Application

8.1. Application Circuit

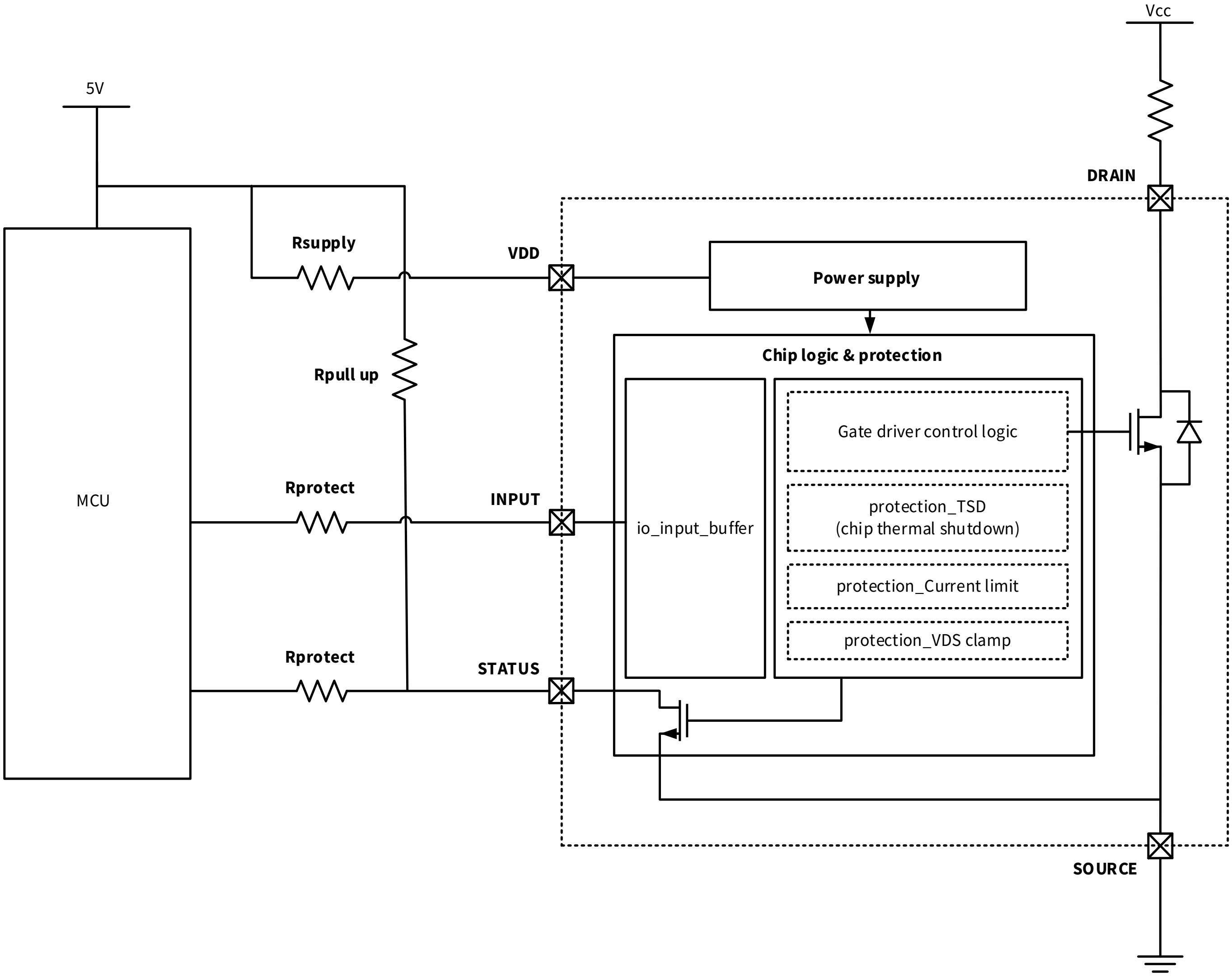


Figure 9 Typical application circuit of NSE11409-Q1

8.2. MCU I/O protection

NSE11409-Q1 has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

$$\frac{V_{ICL}}{I_{latchup}} \leq R_{prot} \leq \frac{V_{MCU\_OUT} - V_{IH}}{I_{IH\max}}$$

Where V_{ICL} is reverse clamp voltage of NSE11409-Q1, $I_{latchup}$ is the MCU I/O latch up current, V_{MCU_OUT} is the output voltage of MCU I/O, V_{IH} is the High-level input voltage of NSE11409-Q1, IIH is the high level input current.

Let:

$I_{latchup} \geq 20mA$; $V_{MCU\_OUT} \geq 4.5V$, so $35\Omega \leq R_{prot} \leq 100k\Omega$. The recommended value is 1kΩ. The supply resistor is the same.

8.3. The value of STATUS pull-up resistor

Because the STATUS pin is open drain output, a pull up resister is needed to fix the high voltage during normal operation. When the fault occurs, the voltage level of STATUS is pulled down by the internal MOSFET on. The value of pull-up resistor can be calculated by the formula as shown below:

$$\left(\frac{V_{pull-up}}{V_{OL}} - 1\right) R_{on} < R_{pull-up} < \frac{V_{pull-up} - V_{OH}}{I_{leak}}$$

Where $V_{pull\text{-}up}$ is the minimum of pull-up supply, V_{OL} is the maximum of MCU logic low, R_{on} is the on resistance of the MOSFET of STATUS pin, V_{OH} is the minimum of MCU logic high, I_{leak} is the maximum leakage current of STATUS pin.

Let:

$V_{pullup} = 4.5V$; $R_{on} = V_{STAT}/I_{STAT} = 500\Omega$; $V_{OL} = 0.9V$; $V_{OH} = 2.1V$; $I_{leak} = 10uA$, so $2k\Omega \leq R_{pull\text{-}up} \leq 240k\Omega$.

8.4. Inductive clamp

When the LSS is turned off while driving the inductive load, due to the energy stored on the inductor during the ON time, this energy needs to be dissipated through LSS without an external freewheeling diode. At this point, the inductor will pull the output voltage to a negative voltage. In order to prevent the drain and source terminals of the MOS from exceeding the breakdown voltage of MOS due to excessive voltage, V_{DS} clamps are needed to protect the MOS.

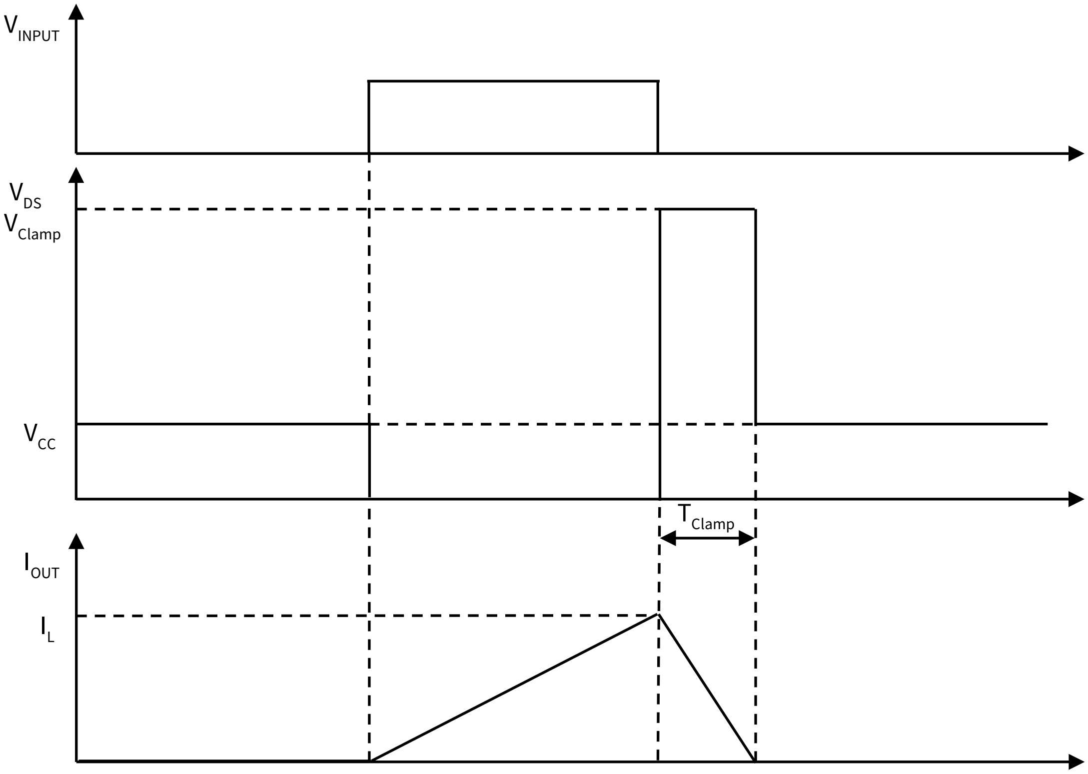


Figure 10 Switching characteristics of inductive load

The formula for calculating clamping energy is derived as follows, assuming that the inductance value is L, low side switch opens for a period of time, the current on L rises to I_L (less than inductance Saturation current), the energy stored on the inductor is:

$$E_L = \frac{1}{2} \cdot L \cdot {I_L}^2$$

$$Vclamp - VCC = -L\frac{di}{dt}$$

$$di = -\frac{Vclamp - VCC}{L}dt$$

$$i = I_L - (\frac{Vclamp - VCC}{L})t$$

$$E = \int_0^{tclamp} i \times Vclamp\ dt = \int_0^{tclamp} \left(I_L - \left(\frac{Vclamp - VCC}{L}\right)t\right) \times Vclamp\ dt = [I_L \times Vclamp \times t - \frac{1}{2}(\frac{V_{clamp} - VCC}{L}) \times Vclamp \times t{}^\wedge 2]_{0}^{tclamp}$$

Where,

$$tclamp = \frac{L \times I_L}{Vclamp - VCC}$$

So that:

$$E = \frac{1}{2} \cdot {I_L}^2 \cdot L \cdot \frac{V_{clamp}}{V_{clamp} - Vcc}$$

For better working reliability, a diode (e.g. 40V, 1A or 2A) could be placed in reverse parallel with the inductor according to the actual load current. Figure 11 shows the recommended application circuit for inductive loads of NSE11409.

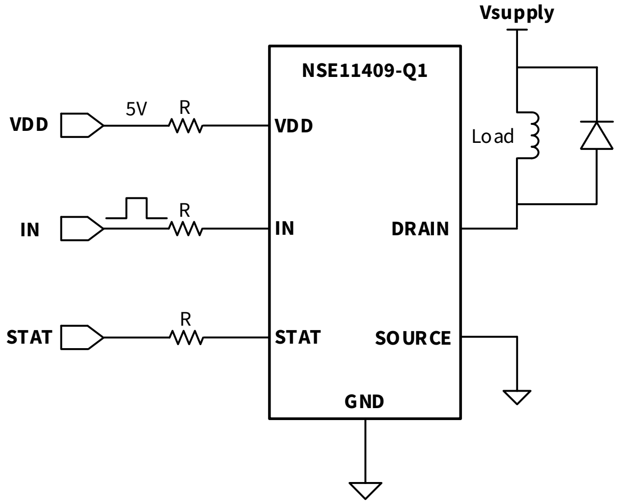


Figure 11 Recommended application circuit for inductive loads of NSE11409

9. Layout

9.1. Layout Guidelines

Both drain and source traces should be wide enough for better heat dissipation, via arrays are recommended to connect multiple layers to improve thermal performance.

9.2. Layout Example

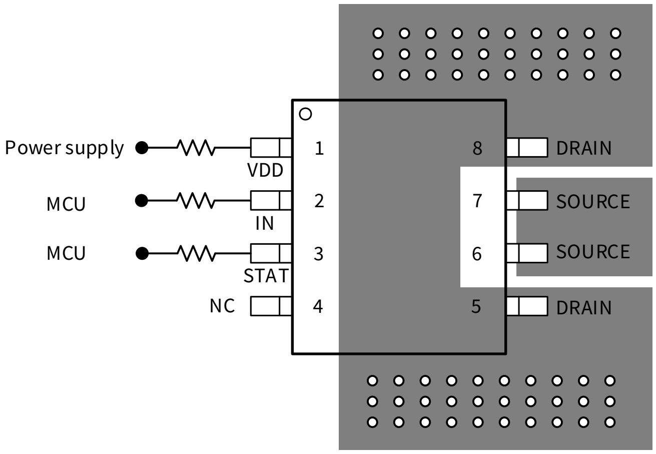


Figure 12 SOP8 Layout Example

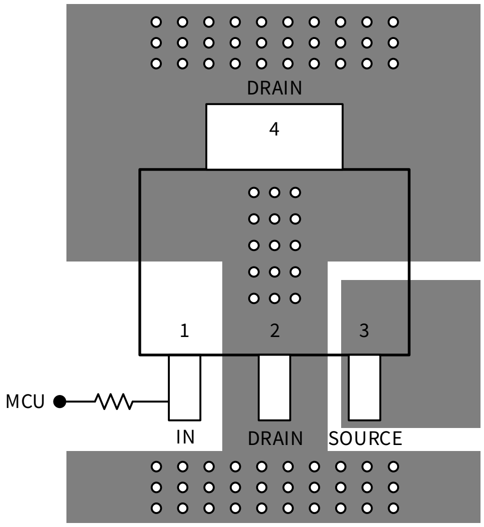
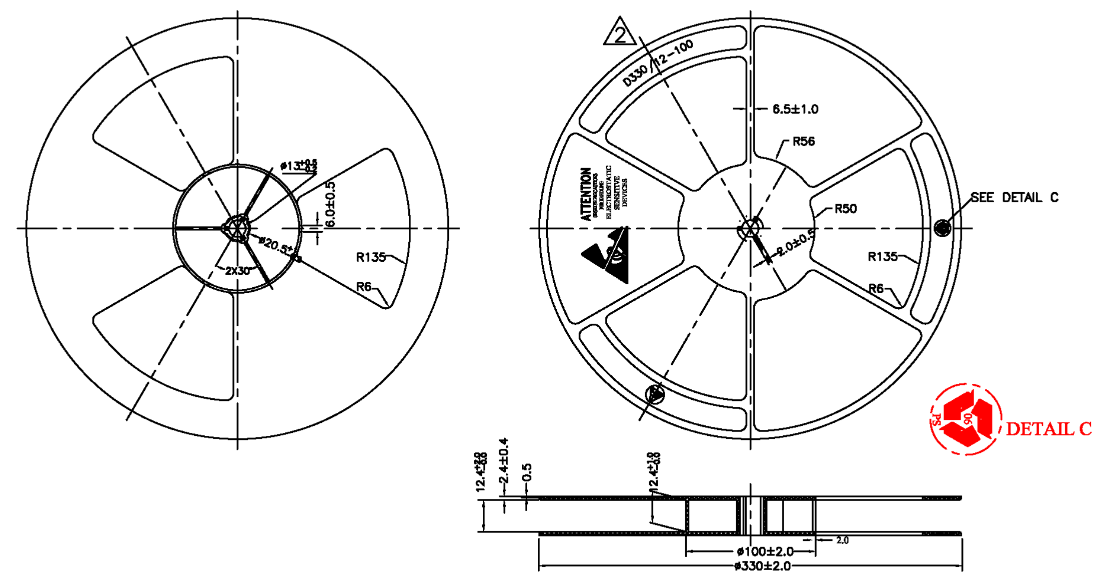


Figure 13 SOT223 Layout Example

10. Package Information

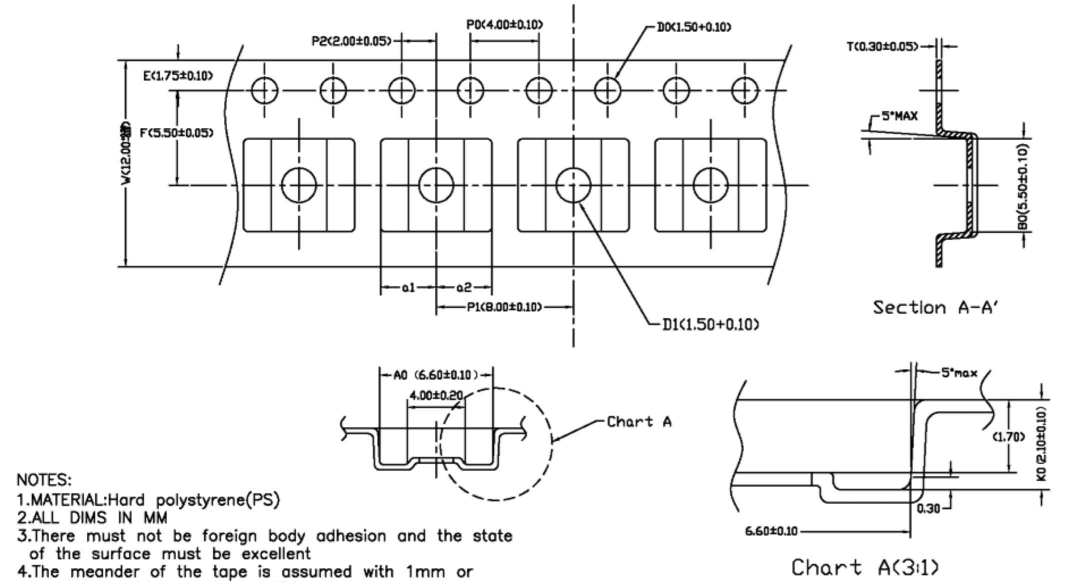
10.1. SOP8

10.1.1. Tape and Reel



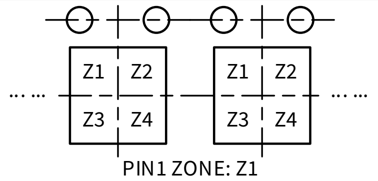
NOTES:

1. MATERIAL: POLYSTYRENE (BLACK).
2. ALL DIMENSIONS NOTED ARE IN MILLIMETERS.
3. TOLERANCE ON ALL DIMENSIONS (NOT OTHERWISE NOTED) IS ±0.25.



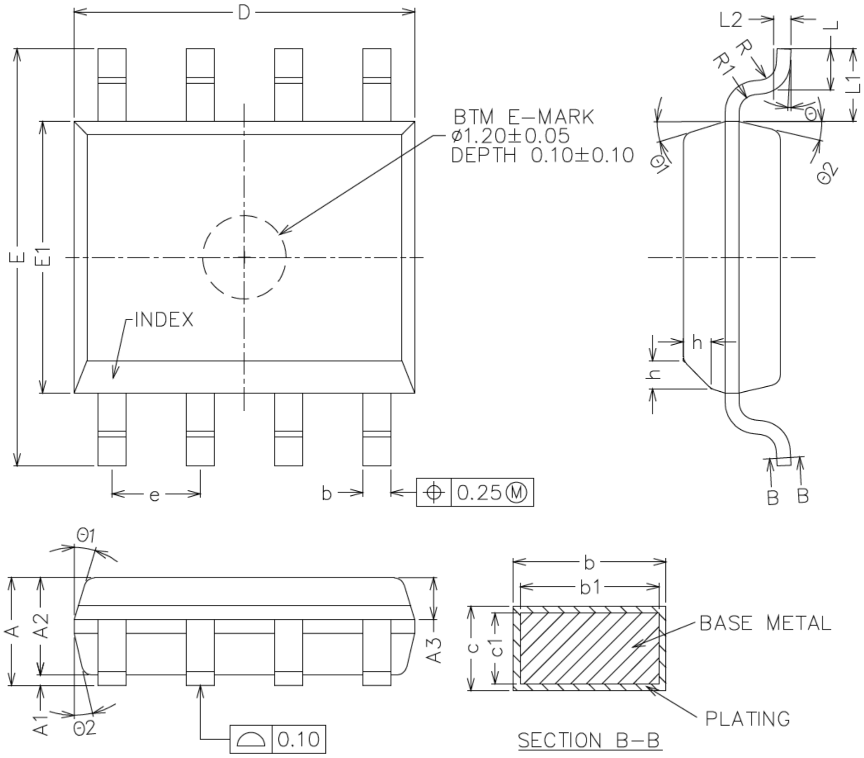
NOTES:

1.MATERIAL:Hard polystyrene(PS)
2.ALL DIMS IN MM
3.There must not be foreign body adhesion and the state of the surface must be excellent
4.The meander of the tape is assumed with 1mm or less every 100mm between 250mm
5.A permissible difference of the accumulation pitch of the sending hole is assumed to be ±0.3 up to 50 pitches
6.The dimension of A0 should be continuous measured at least by 7 pockets which should be embodied in COC; And a1,a2≥3.25mm, | a1−a2 | ≤0.15mm
3 7.ø560 Paper−Reel, EMB−X0084: 60000 pockets(480m)
EMB−X0084(H): 88750(710m)
8.Corner R=0.3max
4 9.Surface resistance 1X10E4≤Rs≤1X10E11 OHMS



PIN1 ZONE: Z1

10.1.2. Mechanical Data

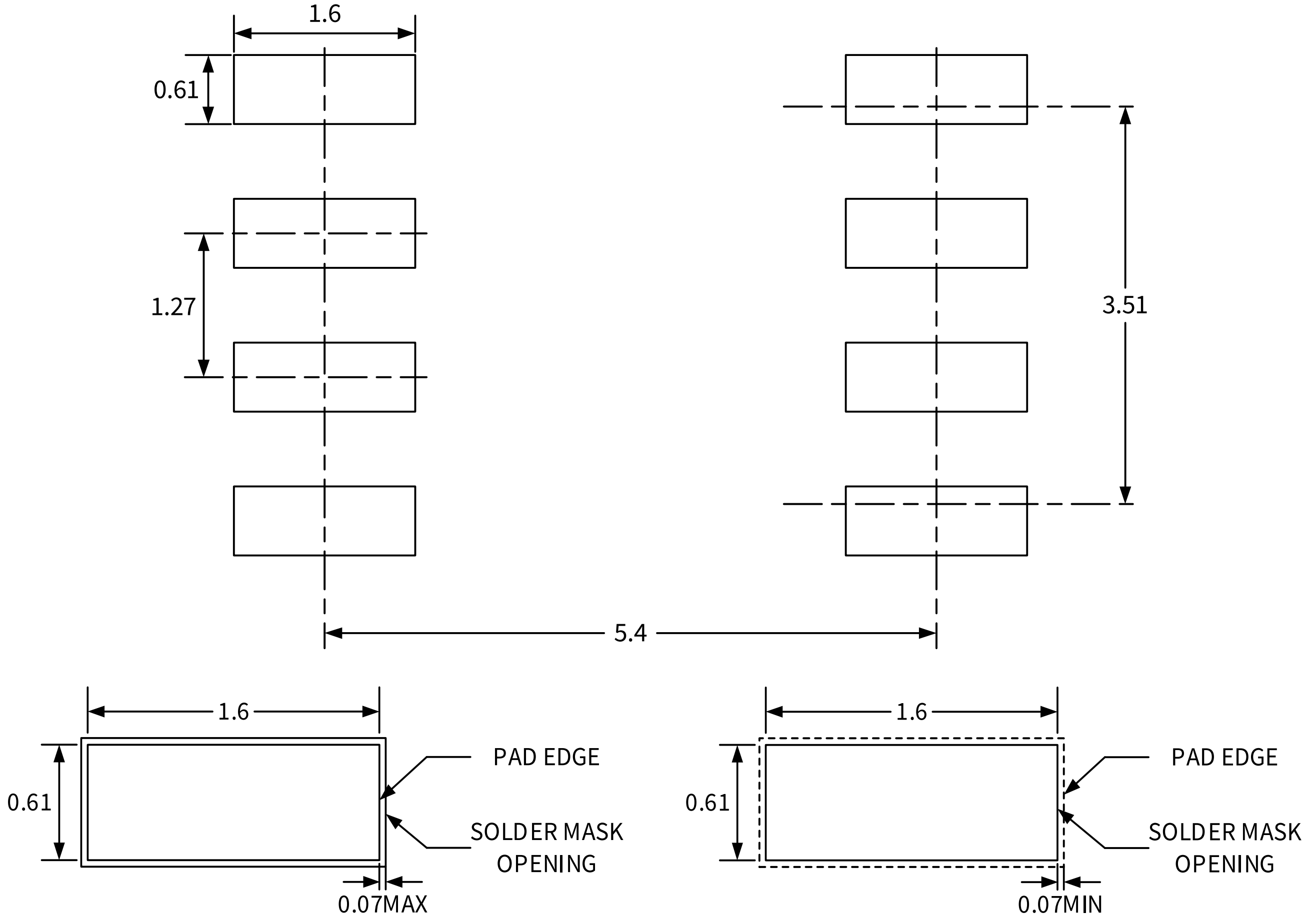


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

10.1.3. Recommended Land Pattern

LAND PATTERN EXAMPLE



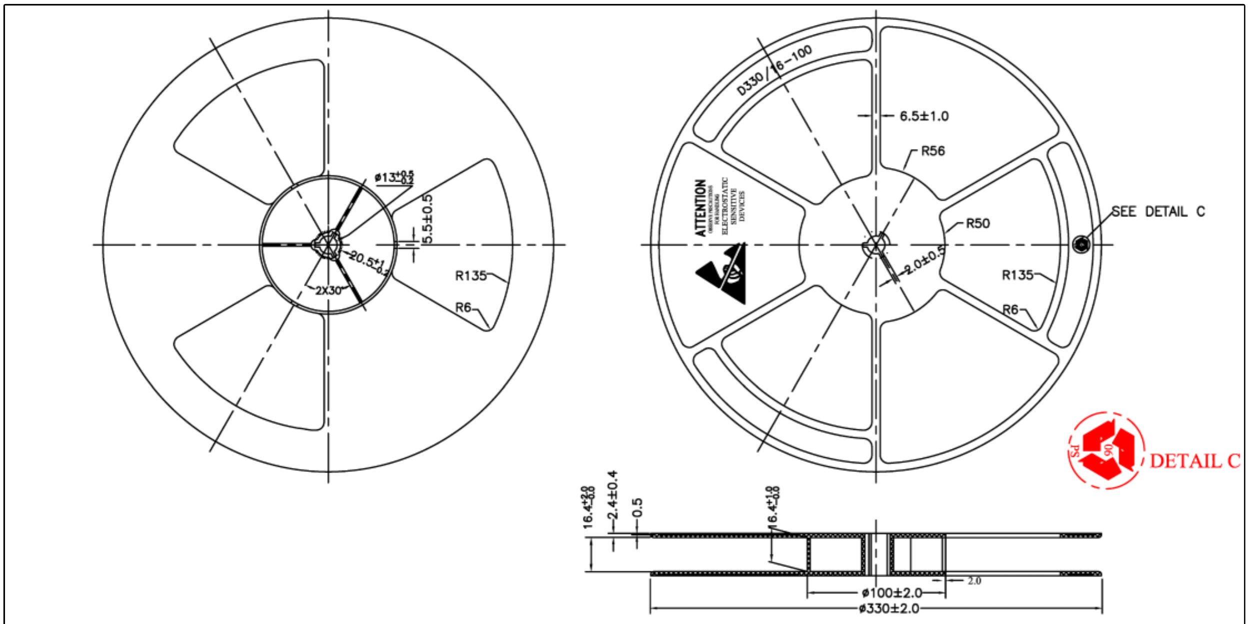
NON-SOLDER MASK
DEFINED PAD

SOLDER MASK
DEFINED PAD

NOTES: ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.

10.2. SOT223

10.2.1. Tape and Reel



NOTES:
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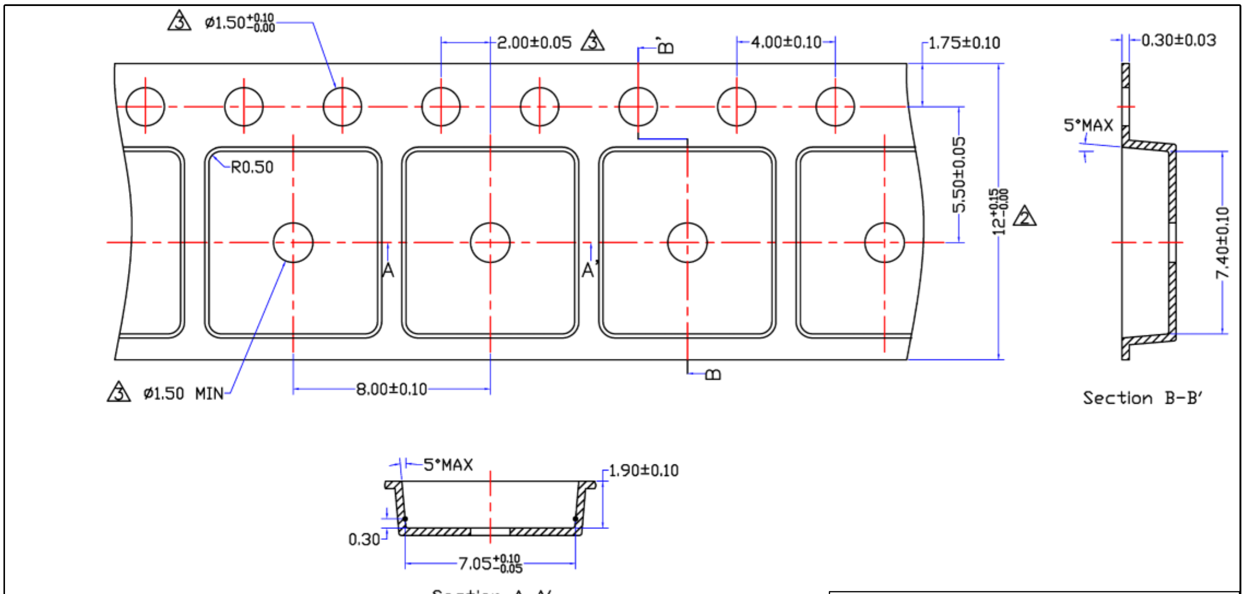
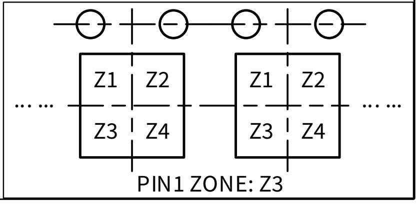
3. TOLERANCE ON ALL DIMENSIONS (NOT OTHERWISE NOTED) IS ±0.25.

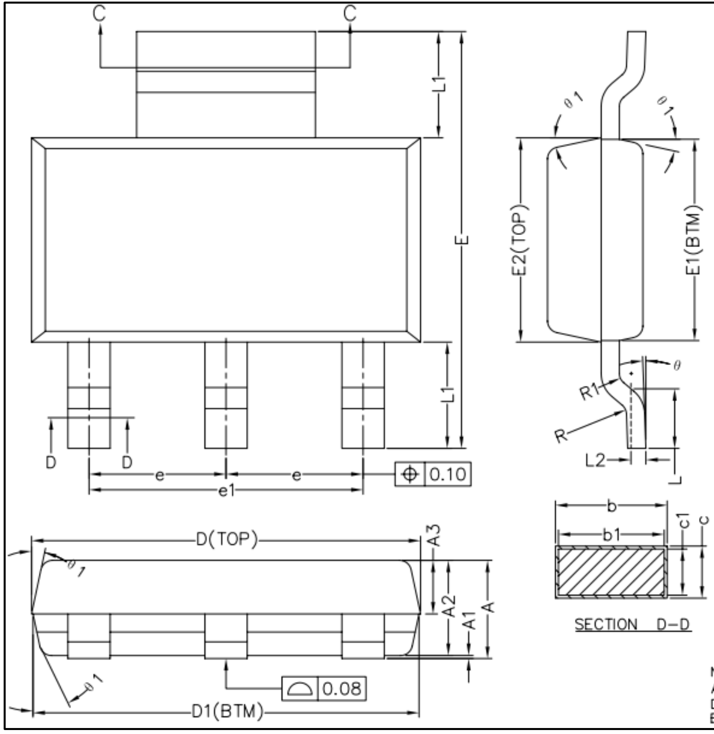


NOTES:
1.10 sprocket hole pitch cumulative tolerance ±0.2
2 2.Carrier camber is within 1mm in 250mm
3.MATERIAL:CONDUCTIVE POLYSTYRENE
4.ALL DIMS IN MM
5.There must not be foreign body adhesion and the state of the surface must be excellent
6.ø330 PLASTIC−Reel, 60625pockets(485m)
3 7.Surface resistance 1X10E5≤Rs≤1X10E9 OHMS/SQ



PIN1 ZONE: Z3

10.2.2. Mechanical Data



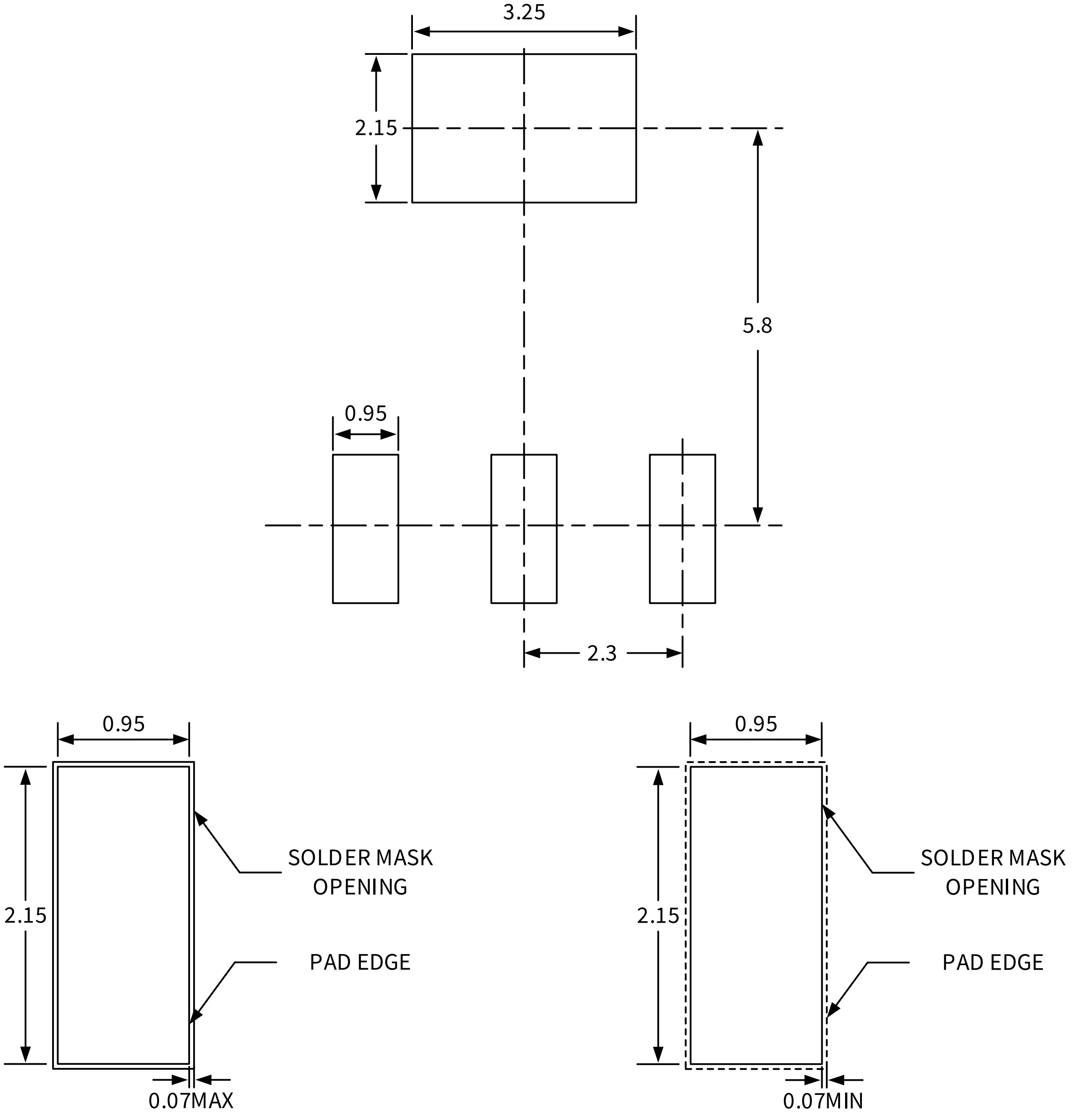
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.80
A1	0.02	–	0.10
A2	1.50	1.60	1.70
A3	0.80	0.90	1.00
b	0.67	–	0.80
b1	0.66	0.71	0.76
b2	2.96	–	3.09
b3	2.95	3.00	3.05
c	0.30	–	0.35
c1	0.29	0.30	0.31
D	6.48	6.53	6.58
D1	6.43	6.48	6.53
E	6.80	–	7.20
E1	3.30	3.38	3.48
E2	3.33	3.43	3.53
e	2.25	2.30	2.35
e1	4.50	4.60	4.70
L	0.80	1.00	1.20
L1	1.78REF		
L2	0.25BSC		
R	0.10	–	–
R1	0.10	–	–
θ	0°	–	8°
θ 1	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD T0261–AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS,
BODY LENGTH INCLUDING MOLD PROTRUSIONS SHALL NOT EXCEED 6.7mm.

10.2.3. Recommended Land Pattern

LAND PATTERN EXAMPLE



NON-SOLDER MASK DEFINED PAD

SOLDER MASK DEFINED PAD

NOTES: ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.

11. Order Information

Orderable Part Number	MSL	Package	SPQ	Marking
NSE11409-QSPR	3	SOP8	2500	NSE 11409Q1
NSE11409-QSTBR	3	SOT223	2500	NSE 11409Q1
NOTE: All packages are RoHS-compliant				

12. Revision history

Revision	Description	Date
1.0	Initial released version	2023/12

IMPORTANT NOTICE

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