

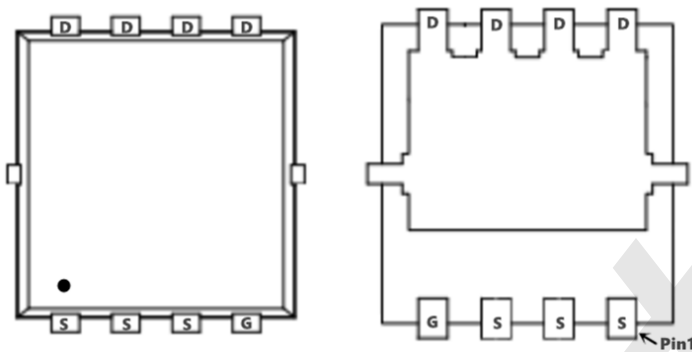
Product Summary

- ◆ $V_{DS} = 100V$ $I_D = 105A$
- ◆ $R_{DS(ON)} < 5.5 m\Omega$ @ $V_{GS}=10V$
- ◆ $R_{DS(ON)} < 8 m\Omega$ @ $V_{GS}=4.5V$

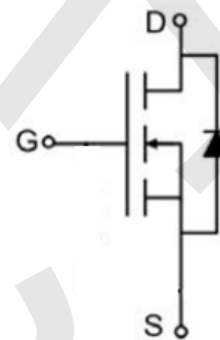
Application

- ◆ Load/Power switch
- ◆ Interfacing, logic switching
- ◆ Battery management for ultra portable electronics

Package and Pin Configuration



Circuit diagram



DFN5*6-8L

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter		N-Channel	Unit
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	
T_J	Maximum Junction Temperature		150	$^\circ C$
T_{STG}	Storage Temperature Range		-55 to 150	$^\circ C$
$I_{DM}^{(1)}$	Pulse Drain Current Tested	$T_c=25^\circ C$	142	A
I_D	Continuous Drain Current	$T_c=25^\circ C$	105	A
		$T_c=100^\circ C$	65	
P_D	Maximum Power Dissipation	$T_c=25^\circ C$	89	W
		$T_c=100^\circ C$	36	
$I_{AS}^{(2)}$	Avalanche Current, Single pulse	$L=0.1mH$	38	A
$E_{AS}^{(2)}$	Avalanche Energy, Single pulse	$L=0.1mH$	72	mJ

Electrical Characteristics (T =25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	100	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	2	3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	4.5	5.5	mΩ
		V _{GS} =4.5V, I _{DS} =10A	-	6.5	8.5	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =10A	-	30.2	-	S
Dynamic Characteristics ⑤						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	0.5	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, Freq.=1MHz	-	3358	-	pF
C _{oss}	Output Capacitance		-	924	-	
C _{rss}	Reverse Transfer Capacitance		-	42	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =25V, I _D =1A, R _{GEN} =3Ω	-	13.3	-	nS
t _r	Turn-on Rise Time		-	4.2	-	
t _{d(OFF)}	Turn-off Delay Time		-	2.9	-	
t _f	Turn-off Fall Time		-	101.4	-	
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =50V I _D =20A	-	32.9	-	nC
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =20A	-	64.3	-	
Q _{gs}	Gate-Source Charge		-	15.2	-	
Q _{gd}	Gate-Drain Charge		-	14.6	-	
Source-Drain Characteristics						
V _{SD} ④	Diode Forward Voltage	I _{SD} =10A, V _{GS} =0V	-	0.8	1.1	V
t _{rr}	Reverse Recovery Time	I _F =20A, V _R =50V	-	47.7	-	nS
Q _{rr}	Reverse Recovery Charge	dl _F /dt=100A/μs	-	59.4	-	nC

Typical Electrical and Thermal Characteristic Curves

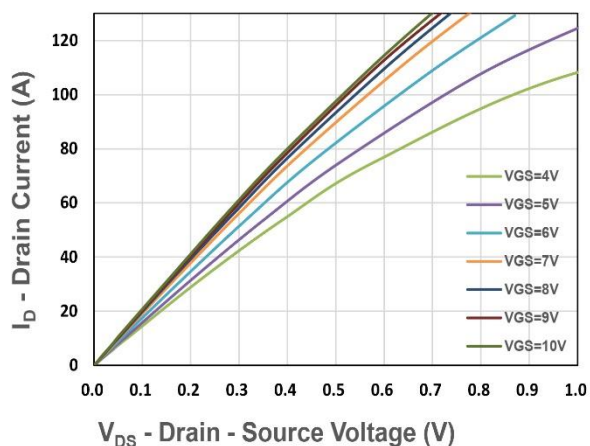


Figure 1. Output Characteristics

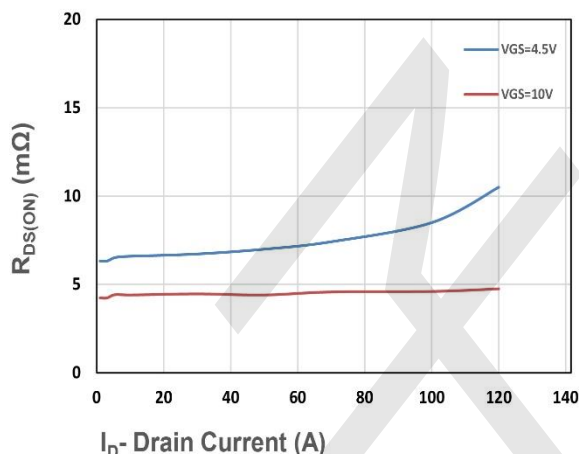


Figure 2. On-Resistance vs. I_D

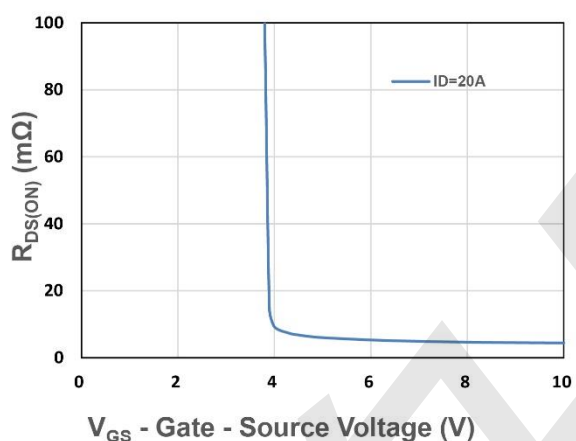


Figure 3. On-Resistance vs. V_{GS}

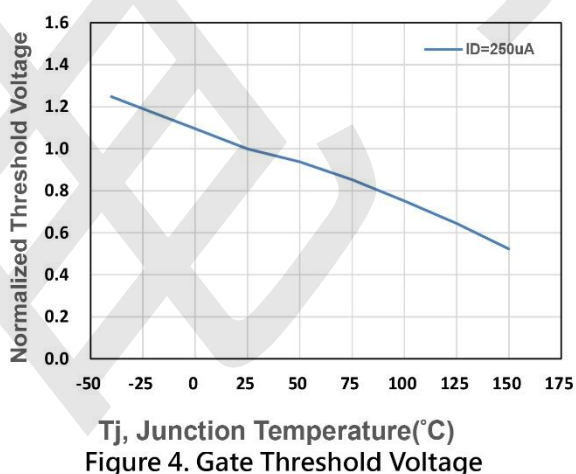


Figure 4. Gate Threshold Voltage

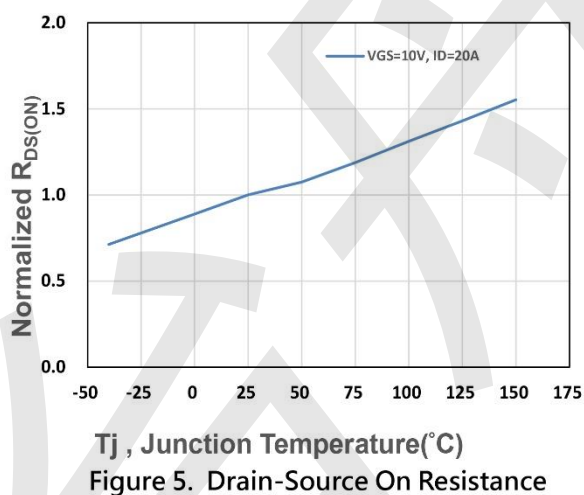


Figure 5. Drain-Source On Resistance

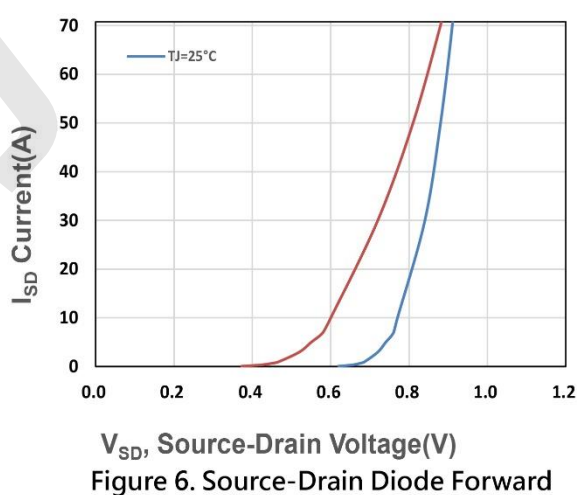
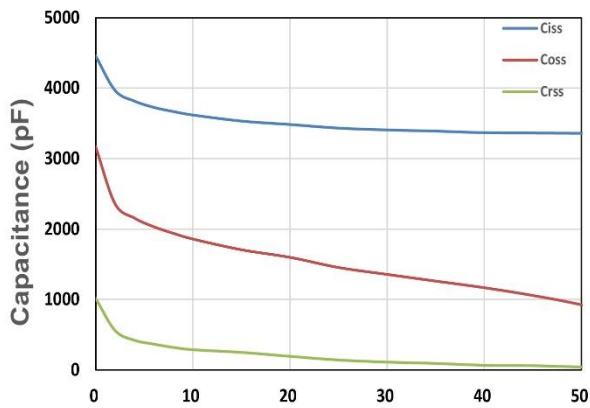
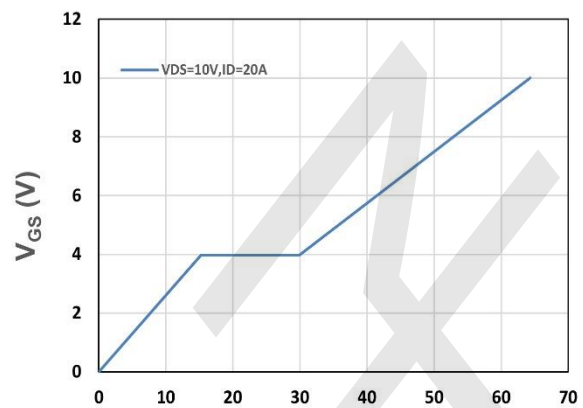


Figure 6. Source-Drain Diode Forward



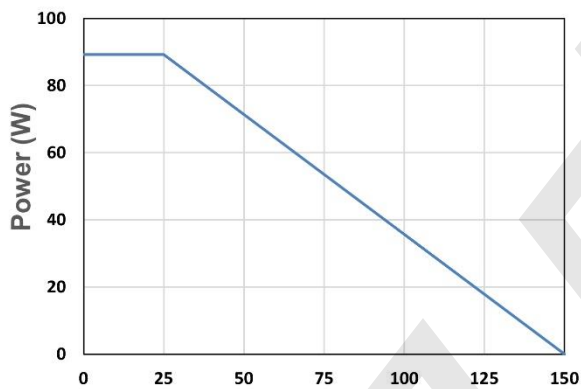
V_{DS} - Drain - Source Voltage (V)

Figure 7. Capacitance



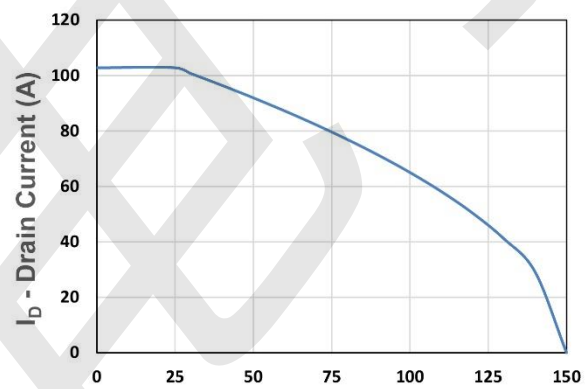
Q_g , Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics



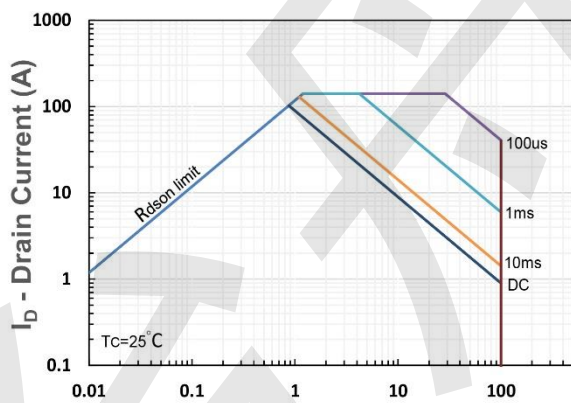
T_c - Case Temperature (°C)

Figure 9. Power Dissipation



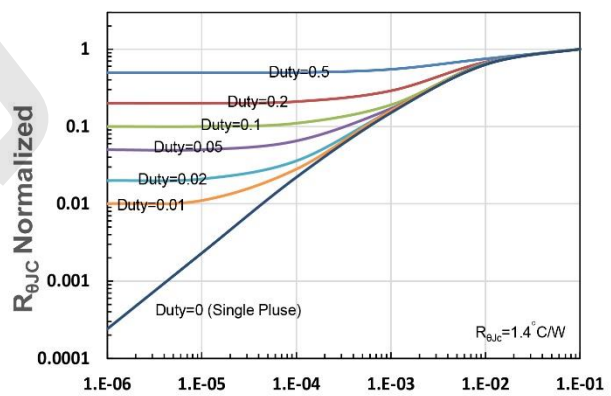
T_c - Case Temperature (°C)

Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)

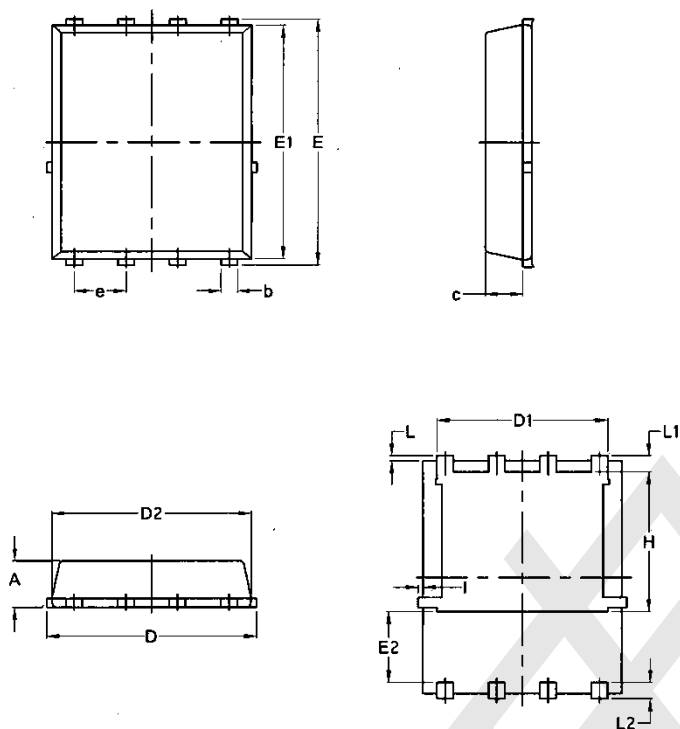
Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration (s)

Figure 12. $R_{\theta JC}$ Transient Thermal Impedance

Package Outline Dimensions DFN5*6-8L



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070