PCA9554A Remote 8-Bit I²C and SMBus I/O Expander With Interrupt Output and Configuration Registers

1 Features

- I²C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/Os
- 400-kHz Fast I²C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I²C/SMBus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Power-Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

This 8-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL), serial data (SDA)].

The PCA9554A consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs with a weak pullup to V_{CC}. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the PCA9554A in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I²C/SMBus state machine.

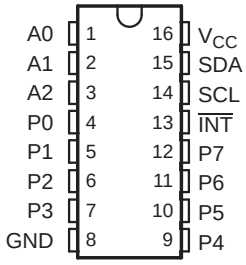
The PCA9554A open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

Device Information(1)

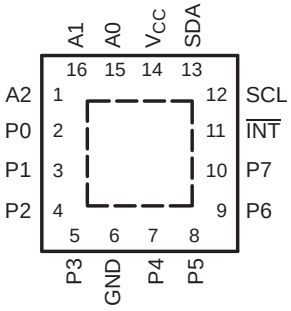
PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9554A	SSOP (16)	6.20 mm × 5.30 mm
	VQFN (16)	4.00 mm × 4.00 mm
	QFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

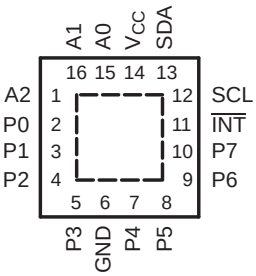
DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



RGV PACKAGE (TOP VIEW)



RGT PACKAGE (TOP VIEW)



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3 Revision History

Changes from Revision D (August 2008) to Revision E **Page**

- Added Interrupt Errata section. ... 15
- Added Power-On Reset Errata section. ... 23

4 Description (Continued)

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the PCA9554A can remain a simple slave device.

The device's outputs (latched) have high-current drive capability for directly driving LEDs and low current consumption.

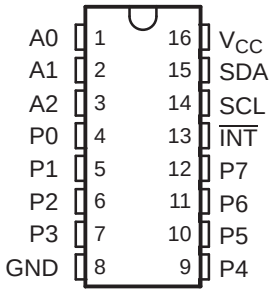
Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C address and allow up to eight devices to share the same I^2C bus or SMBus.

The PCA9554A is pin-to-pin and I^2C address compatible with the PCF8574A. However, software changes are required, due to the enhancements in the PCA9554A over the PCF8574A.

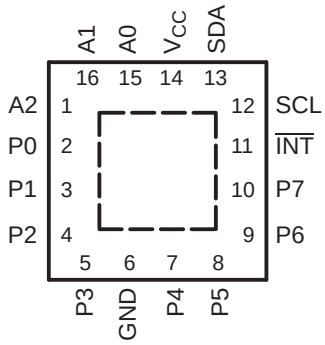
The PCA9554A and PCA9554 are identical except for their fixed I^2C address. This allows for up to 16 of these devices (8 of each) on the same I^2C/SMBus.

5 Pin Configuration And Functions

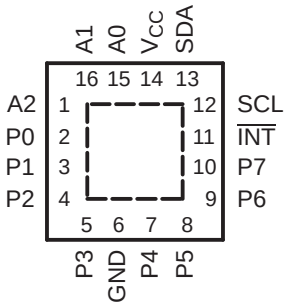
DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



RGV PACKAGE (TOP VIEW)



RGT PACKAGE (TOP VIEW)



Pin Functions

PIN			DESCRIPTION
NAME	QSOP (DBQ) SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT AND RGV)	
A0	1	15	Address input. Connect directly to V_{CC} or ground.
A1	2	16	Address input. Connect directly to V_{CC} or ground.
A2	3	1	Address input. Connect directly to V_{CC} or ground.
P0	4	2	P-port input/output. Push-pull design structure.
P1	5	3	P-port input/output. Push-pull design structure.
P2	6	4	P-port input/output. Push-pull design structure.
P3	7	5	P-port input/output. Push-pull design structure.
GND	8	6	Ground
P4	9	7	P-port input/output. Push-pull design structure.
P5	10	8	P-port input/output. Push-pull design structure.
P6	11	9	P-port input/output. Push-pull design structure.
P7	12	10	P-port input/output. Push-pull design structure.
$\overline{INT}$	13	11	Interrupt output. Connect to V_{CC} through a pullup resistor.
SCL	14	12	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	15	13	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	16	14	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance(3)	DB package		82	°C/W
		DBQ package		90	
		DGV package		120	
		DW package		57	
		PW package		108	
		RGT package		TBD	
		RGV package		51	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	5.5	V
		A2–A0, P7–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A2–A0, P7–P0	–0.5	0.8	
I_{OH}	High-level output current	P7–P0		–10	mA
I_{OL}	Low-level output current	P7–P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, I_O = 0	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	3.1			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	3			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	8		mA
	P port(3)	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	$\overline{INT}$	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	10		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	2.3 V to 5.5 V			–100	µA
I_{CC}	Operating mode	$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 400 kHz, No load	5.5 V		104	175	µA
			3.6 V		50	90	
			2.7 V		20	65	
		$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 100 kHz, No load	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz, No load	5.5 V		450	700	
			3.6 V		300	600	
			2.7 V		225	500	
		$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 0 kHz, No load	5.5 V		0.25	1	
			3.6 V		0.2	0.9	
			2.7 V		0.1	0.8	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		Every LED I/O at V_I = 4.3 V; f_{scl} = 0 kHz	5.5 V			1	
C_I	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5.5	6.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P0 to P7) must be limited to a maximum current of 200 mA.

6.5 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 14)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start		4.7		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		4.7		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		4		0.6		µs
t_{sps}	I²C Stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	µs
C_b	I²C bus capacitive load			400		400	ns

(1) C_b = Total capacitive load of one bus in pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 15 and Figure 16)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{pv}	Output data valid	SCL	P7–P0		200		200	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		µs

6.7 Typical Characteristics

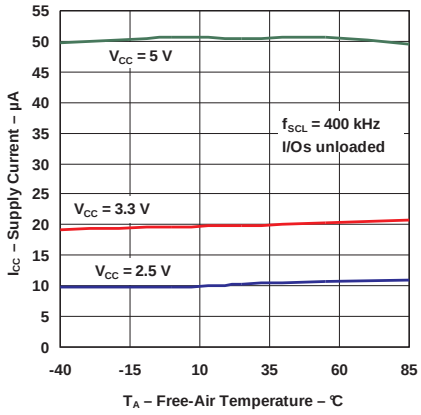


Figure 1. Supply Current vs Temperature

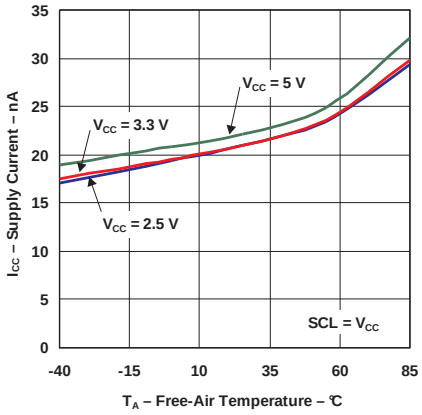


Figure 2. Quiescent Supply Current vs Temperature

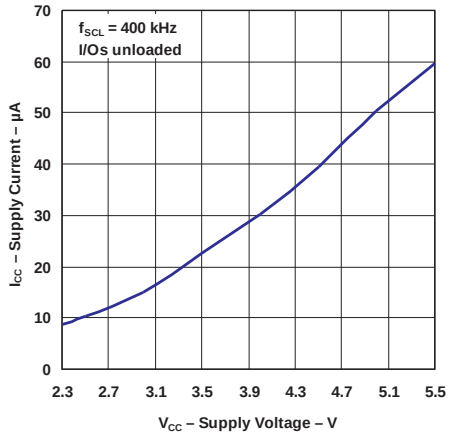


Figure 3. Supply Current vs Supply Voltage

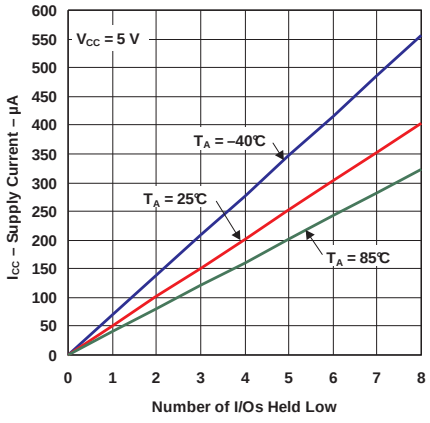


Figure 4. Supply Current vs Number Of I/Os Held Low

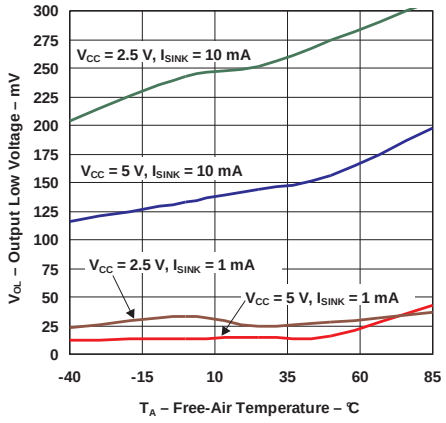


Figure 5. I/O Output Low Voltage vs Temperature

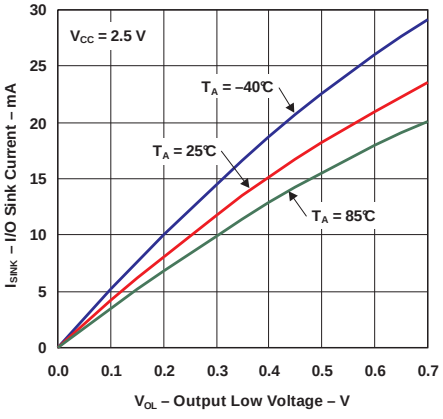


Figure 6. I/O Sink Current vs Output Low Voltage

Typical Characteristics (continued)

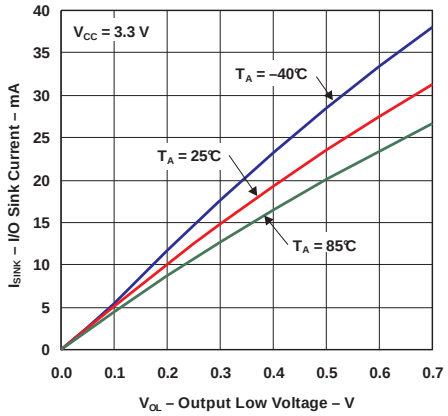


Figure 7. I/O Sink Current vs Output Low Voltage

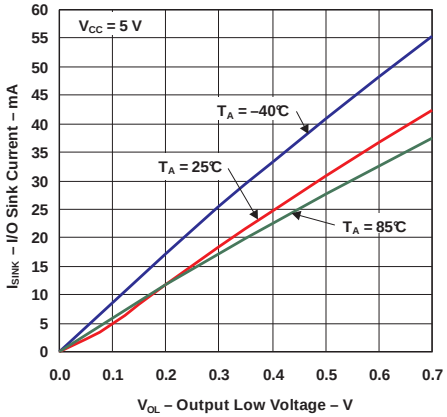


Figure 8. I/O Sink Current vs Output Low Voltage

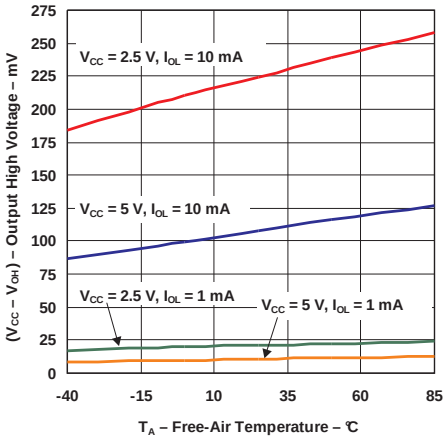


Figure 9. I/O Output High Voltage vs Temperature

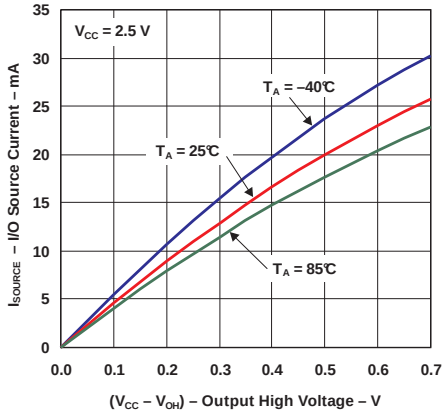


Figure 10. I/O Source Current vs Output High Voltage

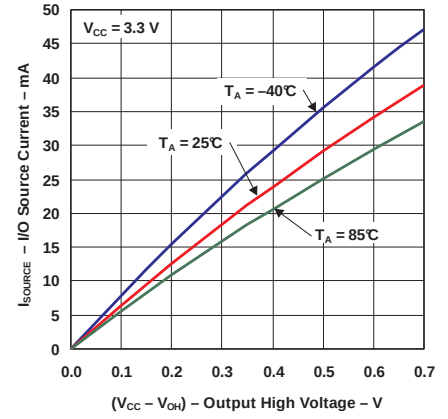


Figure 11. I/O Source Current vs Output High Voltage

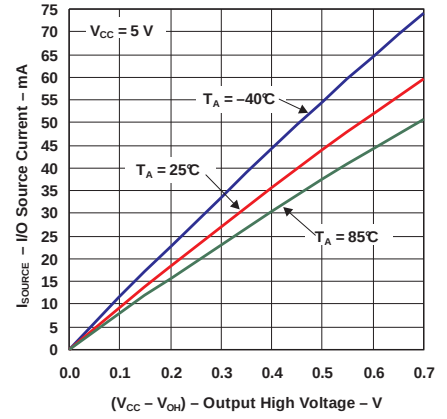


Figure 12. I/O Source Current vs Output High Voltage

Typical Characteristics (continued)

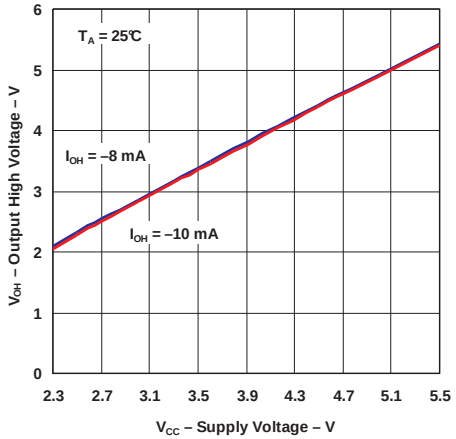
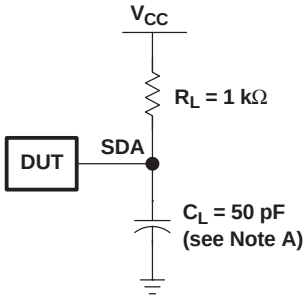
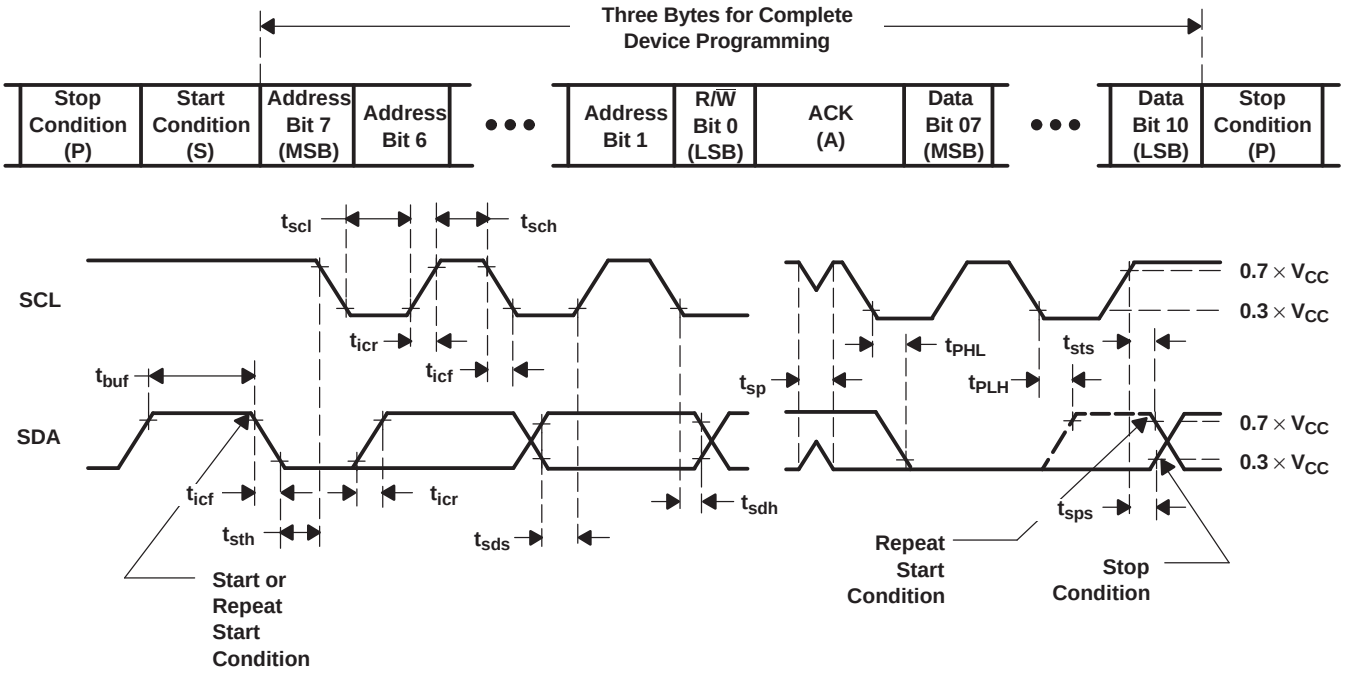


Figure 13. Output High Voltage vs Supply Voltage

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

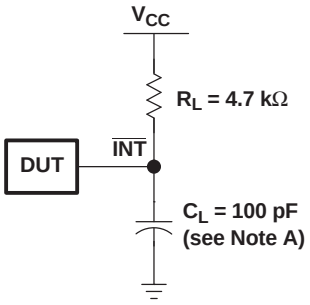
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

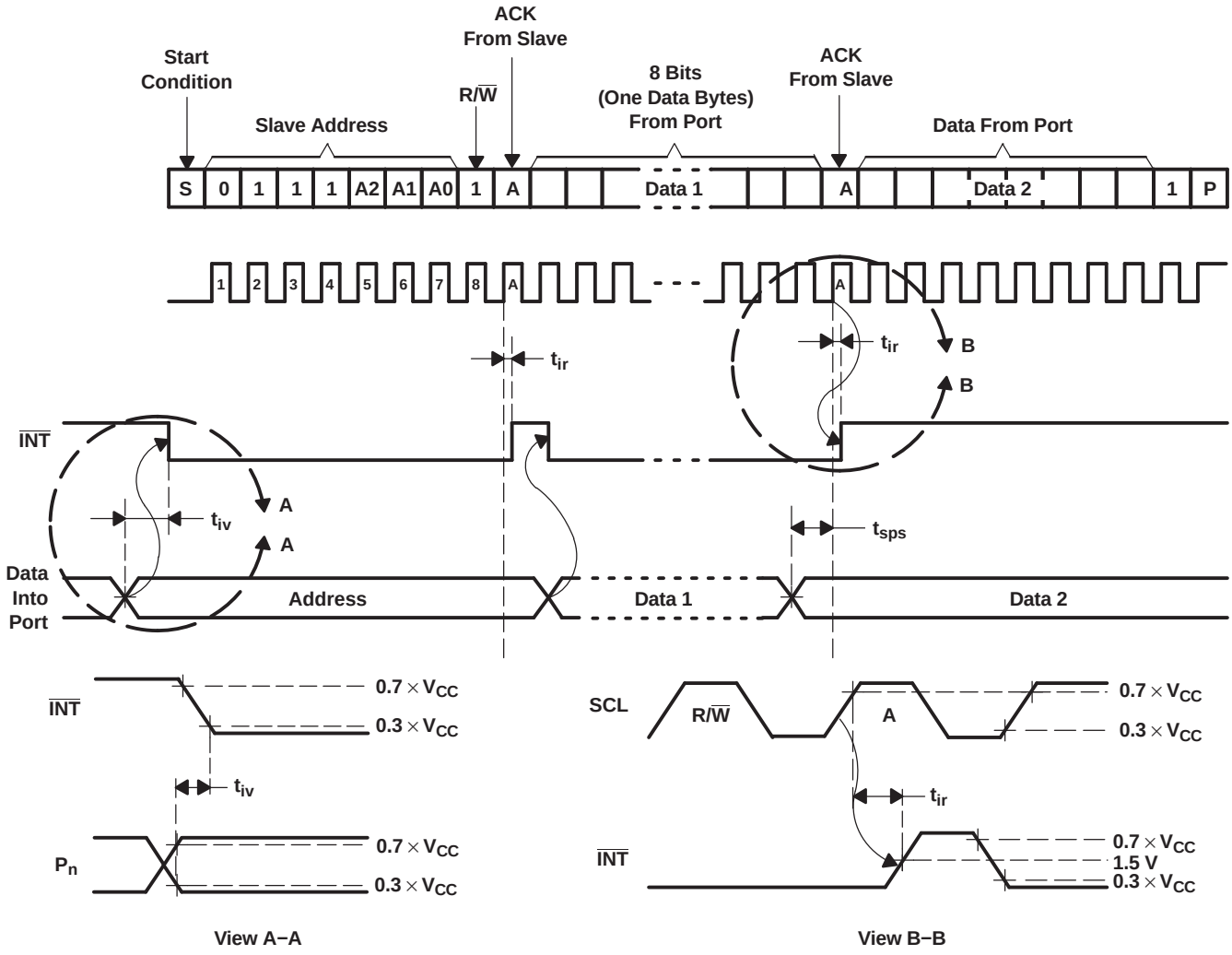
C. All parameters and waveforms are not applicable to all devices.

Figure 14. I^2C Interface Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION



View A–A View B–B

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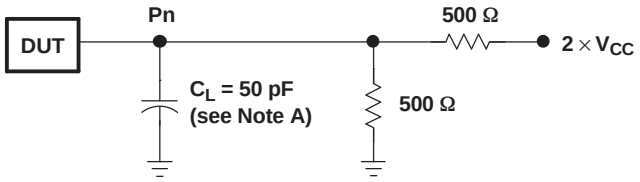
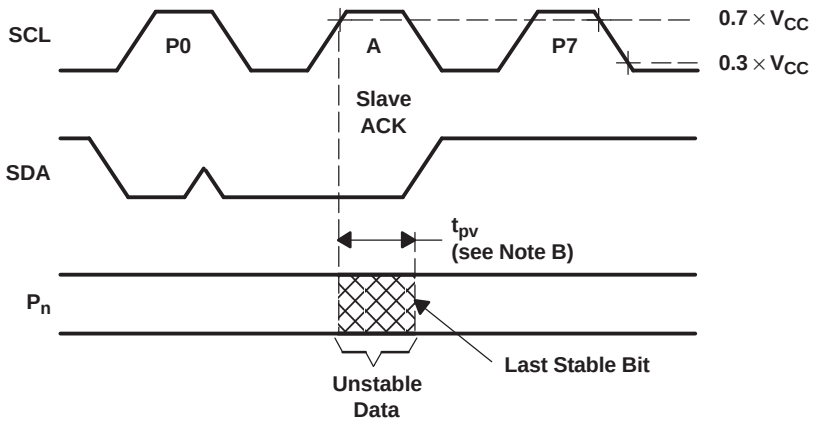
Figure 15. Interrupt Load Circuit And Voltage Waveforms

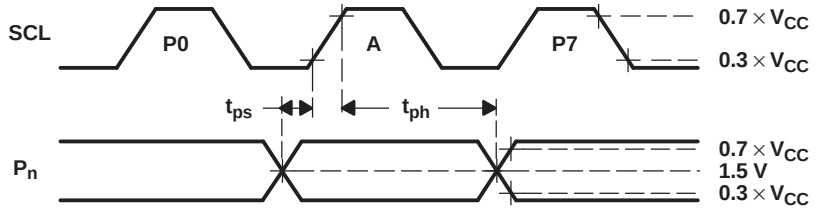
Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O pin output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

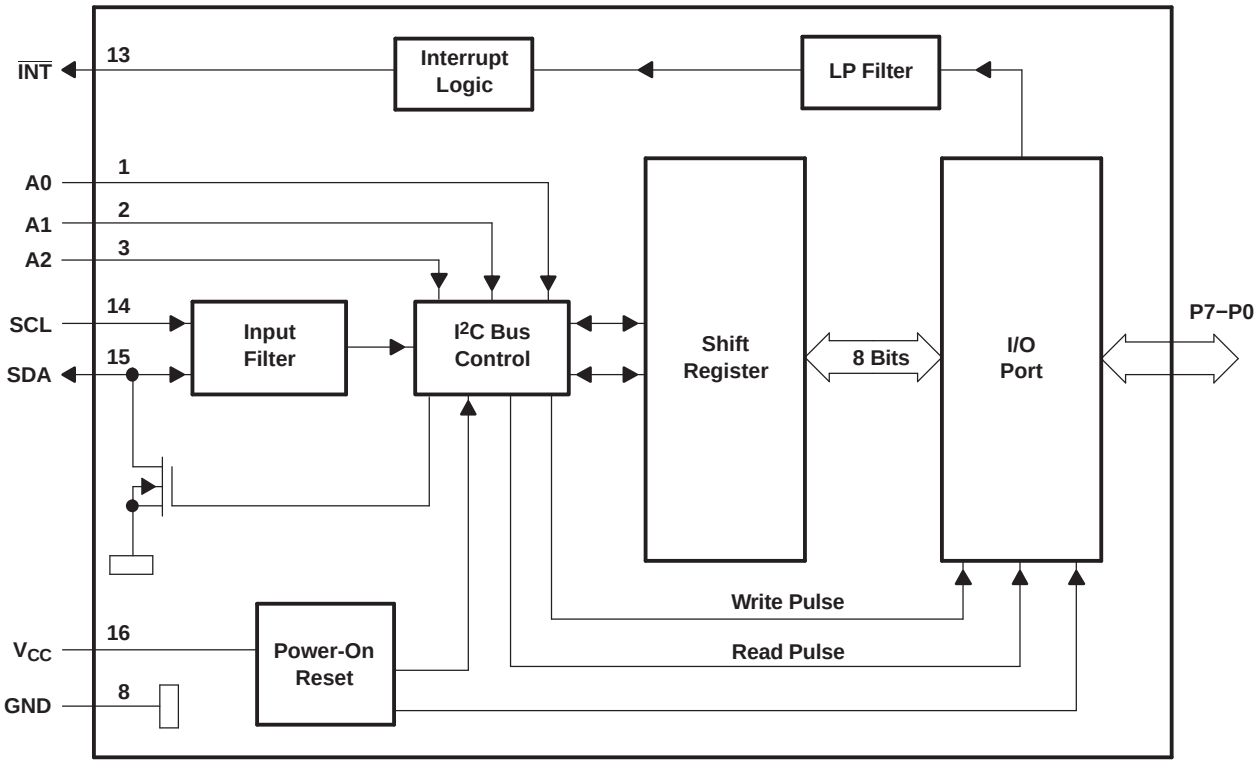
D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 16. P-Port Load Circuit And Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

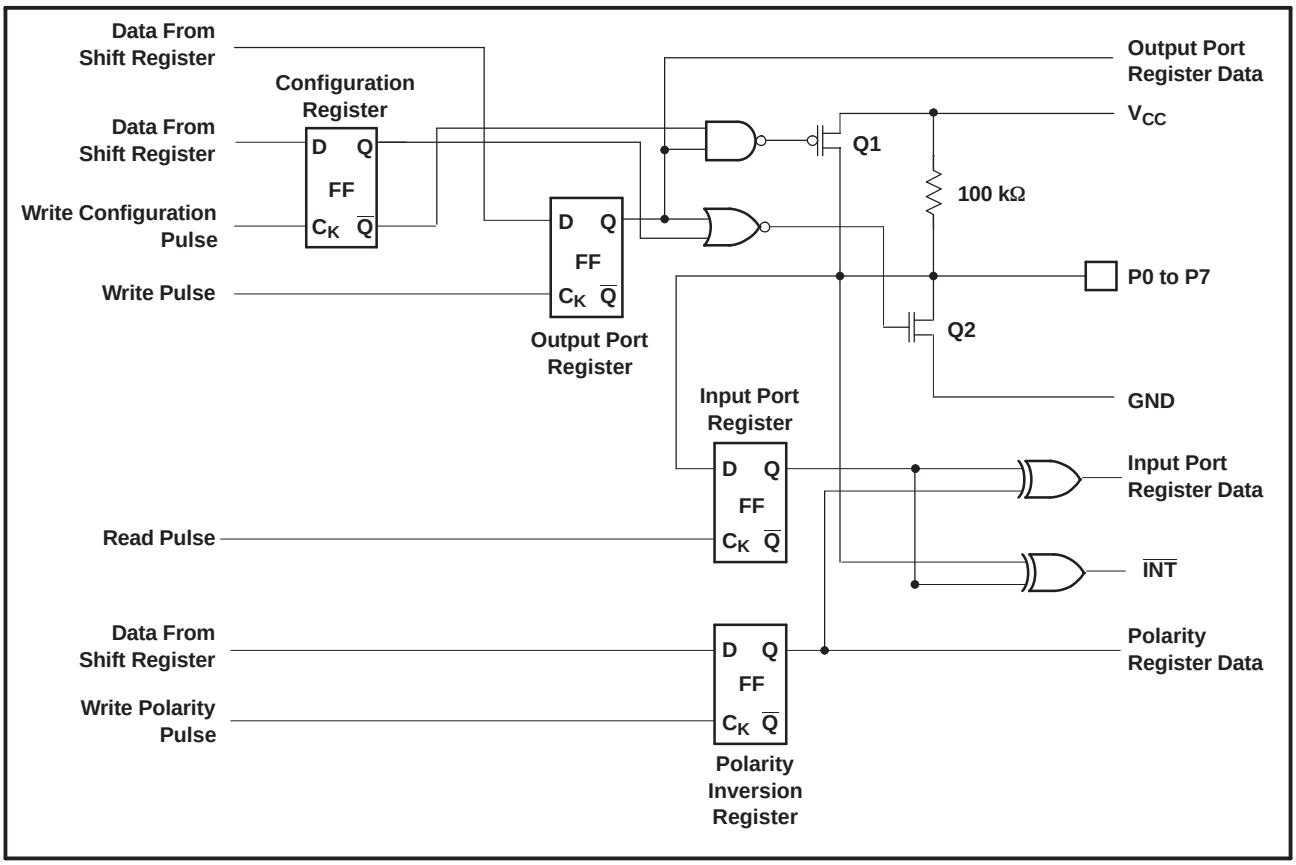


A. Pin numbers shown are for the DB, DBQ, DGV, DW, or PW package.

B. All I/Os are set to inputs at reset.

Figure 17. Logic Diagram

Functional Block Diagram (continued)



A. At power-on reset, all registers return to default values.

Figure 18. Simplified Schematic Of P0 To P7

8.2 Device Functional Modes

8.2.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9554A in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9554A registers and I^2C/SMBus state machine will initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Refer to the *Power-On Reset Errata* section.

8.2.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in Figure 18) are off, which creates a high impedance input with a weak pullup (100 kΩ typ) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.2.3 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Device Functional Modes (continued)

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

8.2.3.1 Interrupt Errata

Description

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I^2C command byte (register pointer) written to the device was 00h.

> **NOTE**
> This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I^2C bus acknowledges an address byte with the R/W bit set high

System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9554A device or before reading from another slave device.

> **NOTE**
> Software change will be compatible with other versions (competition and TI redesigns) of this device.

8.3 Programming

8.3.1 I^2C Interface

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 19). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit ($R/\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and Stop conditions.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 20).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 19).

Programming (continued)

Any number of data bytes can be transferred from the transmitter to receiver between the Start and Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 21). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

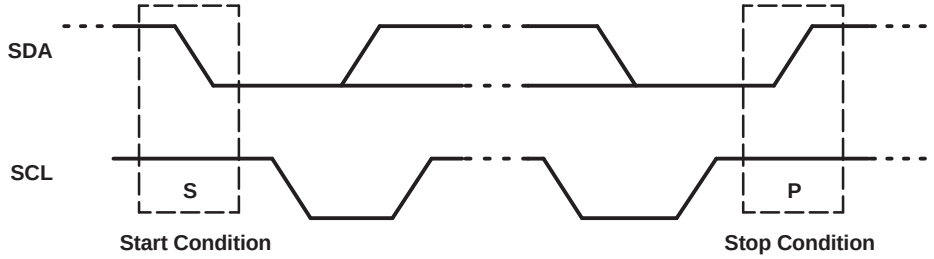


Figure 19. Definition Of Start And Stop Conditions

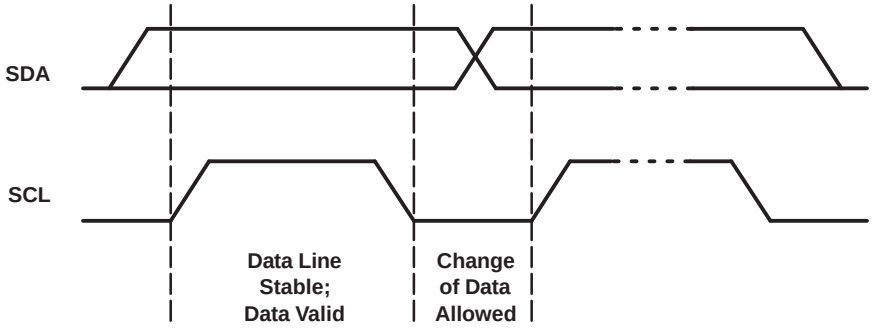


Figure 20. Bit Transfer

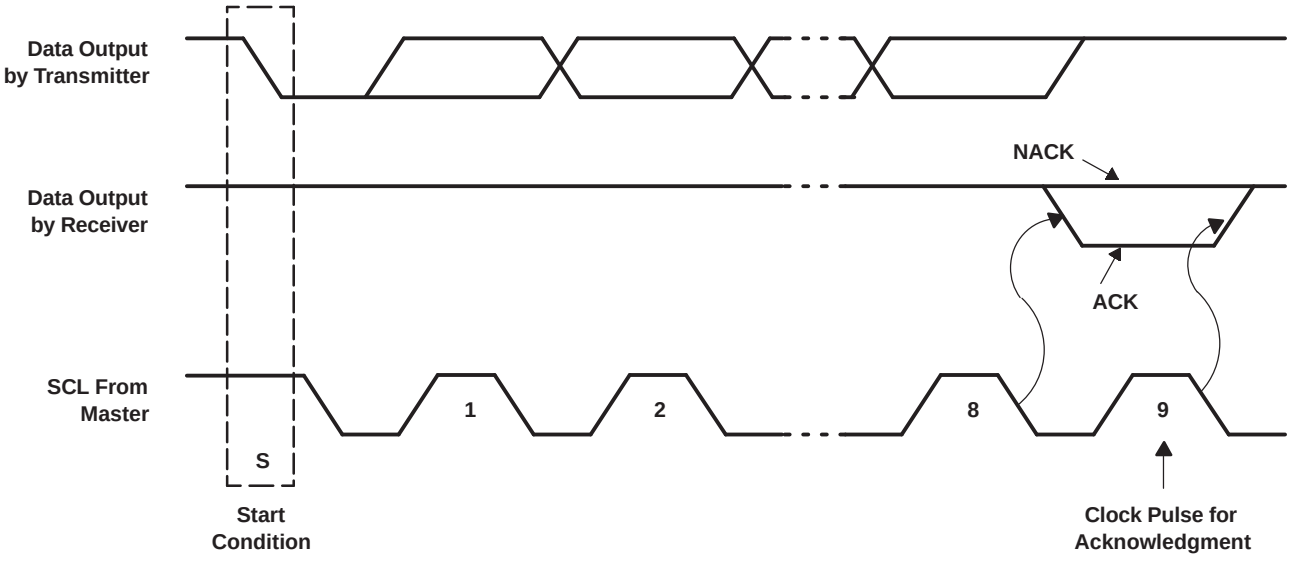


Figure 21. Acknowledgment On The I^2C Bus

Programming (continued)

8.3.2 Register Map

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	L	H	H	H	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.3.2.1 Device Address

Figure 22 shows the address byte for the PCA9554A.

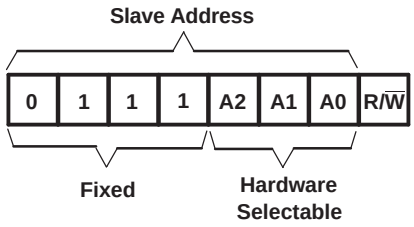


Figure 22. Pca9554a Address

Table 2. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	H	57 (decimal), 39 (hexadecimal)
L	H	L	58 (decimal), 3A (hexadecimal)
L	H	H	59 (decimal), 3B (hexadecimal)
H	L	L	60 (decimal), 3C (hexadecimal)
H	L	H	61 (decimal), 3D (hexadecimal)
H	H	L	62 (decimal), 3E (hexadecimal)
H	H	H	63 (decimal), 3F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected. A low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9554A. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

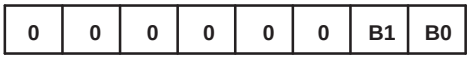


Figure 23. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	XXXX XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

8.3.2.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the Input Port register will be accessed next.

Table 4. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

Table 6. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

8.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9554A through write and read commands.

8.3.2.4.1 Writes

Data is transmitted to the PCA9554A by sending the device address and setting the least-significant bit to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 24 and Figure 25). There is no limitation on the number of data bytes sent in one write transmission.

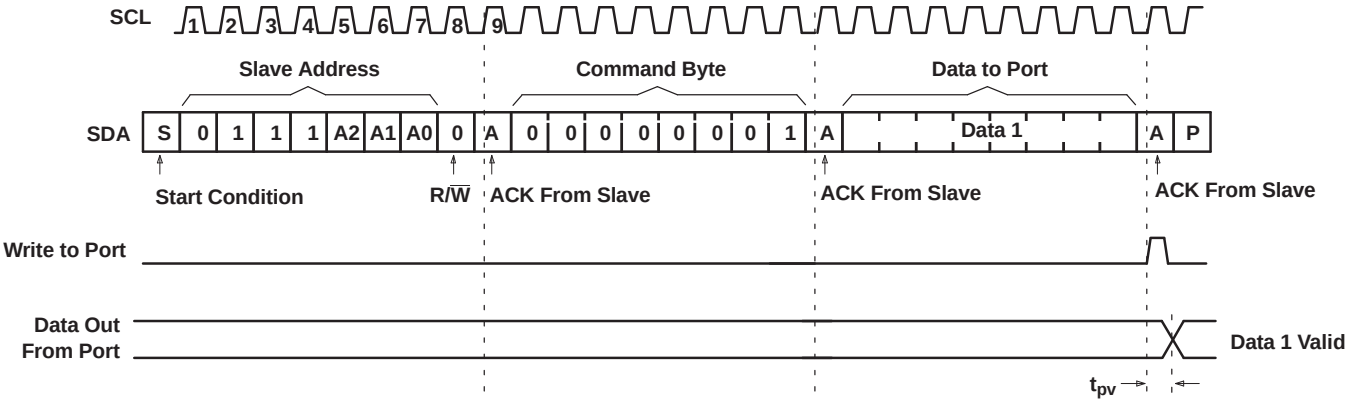


Figure 24. Write To Output Port Register

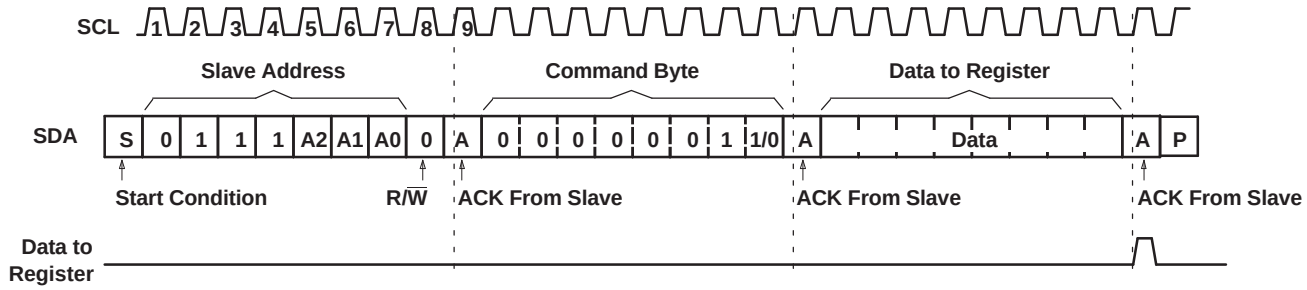


Figure 25. Write To Configuration Or Polarity Inversion Registers

8.3.2.4.2 Reads

The bus master first must send the PCA9554A address with the least significant bit (LSB) set to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9554A (see Figure 26 and Figure 27). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

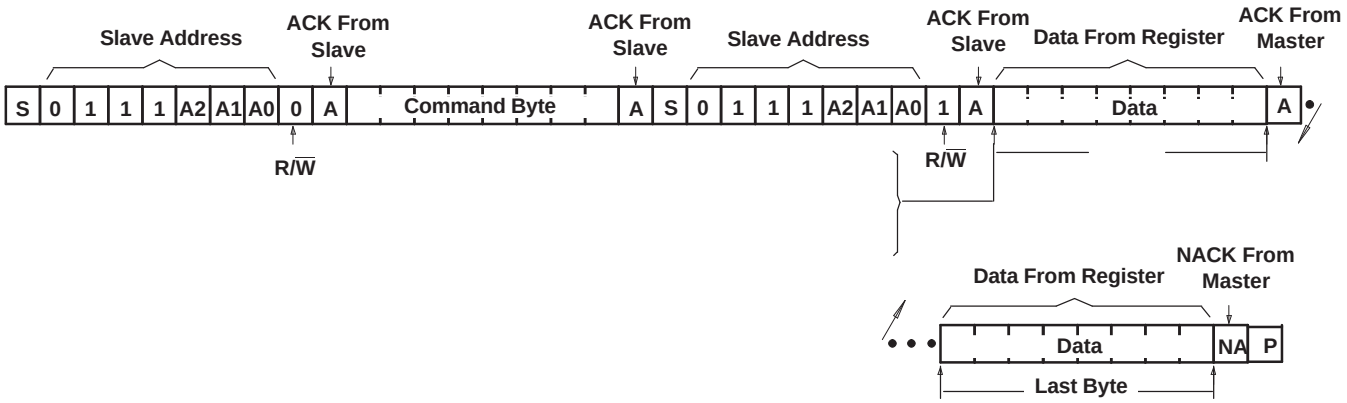
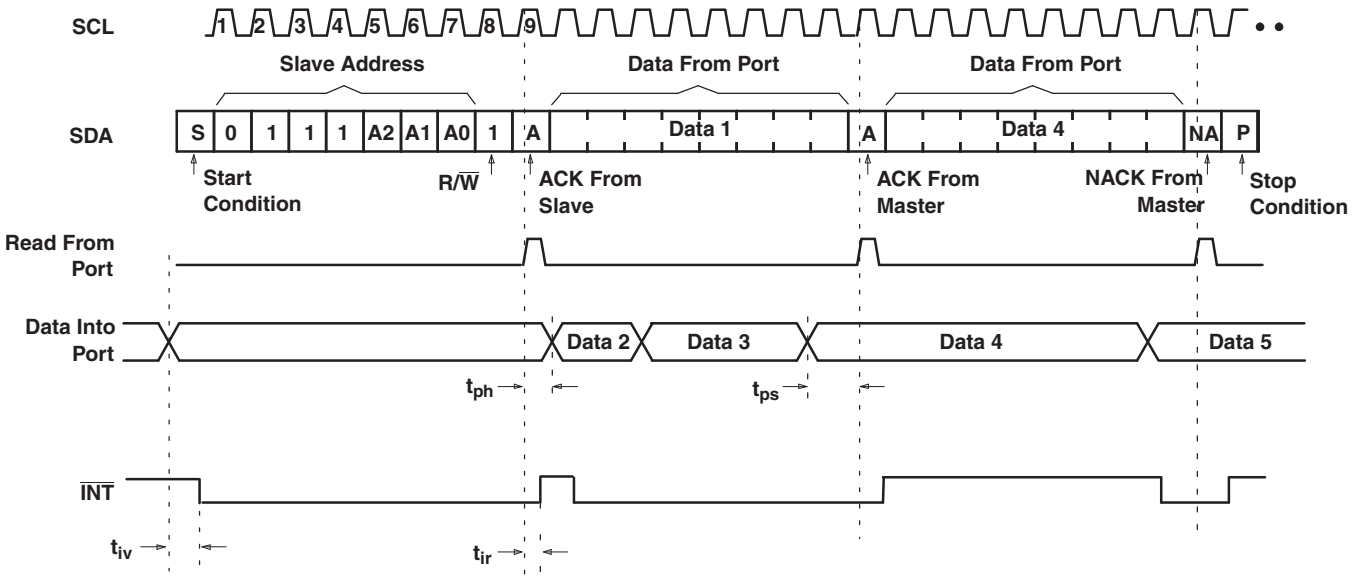


Figure 26. Read From Register



A. This figure assumes the command byte has previously been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

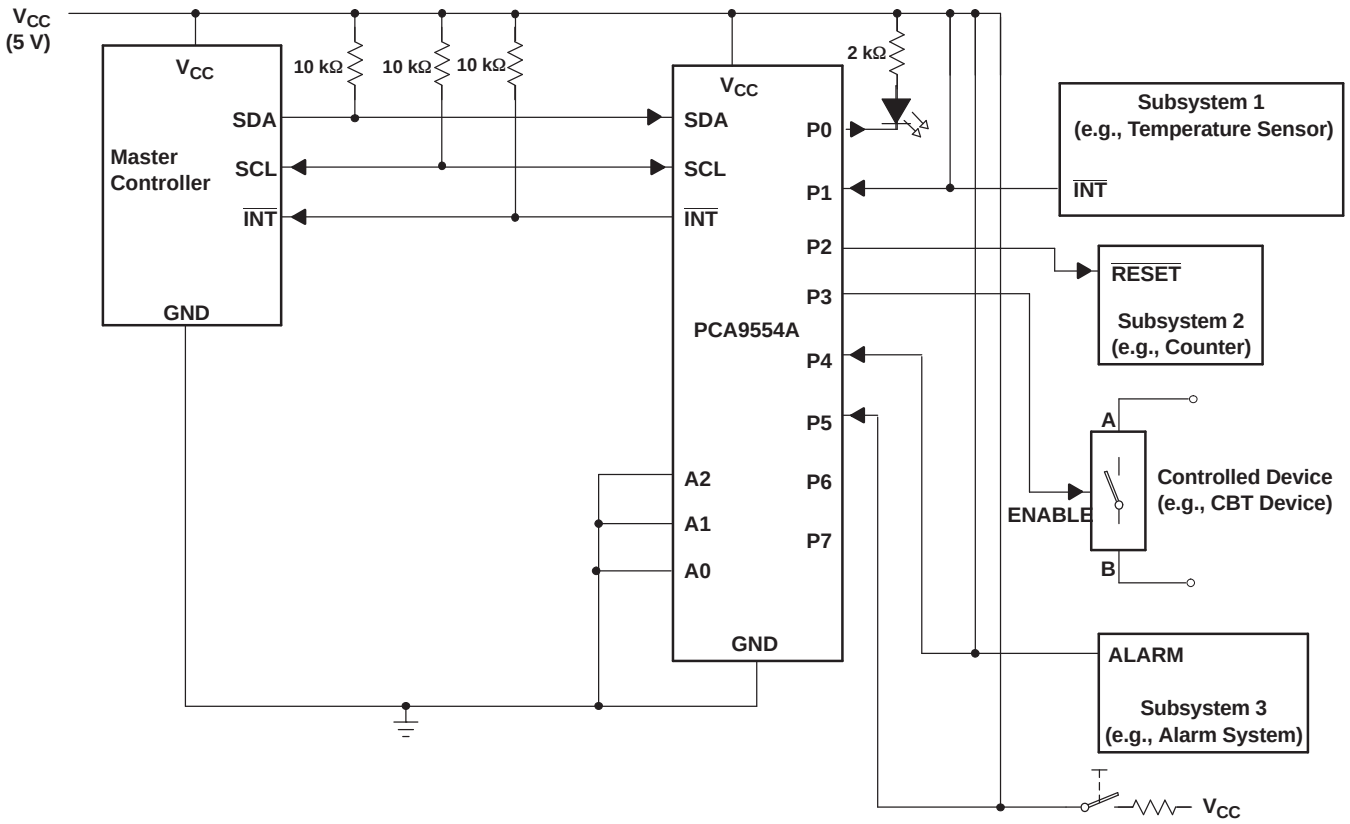
C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See Figure 26 for these details.

Figure 27. Read From Input Port Register

9 Application And Implementation

9.1 Typical Application

Figure 28 shows an application in which the PCA9554A can be used.



A. Device address is configured as 0111000 for this example.
B. P0, P2, and P3 are configured as outputs.
C. P1, P4, and P5 are configured as inputs.
D. P6 and P7 are not used and have internal 100-kΩ pullup resistors to protect them from floating.

Figure 28. Typical Application

Typical Application (continued)

9.1.1 Detailed Design Procedure

9.1.1.1 Minimizing I_{CC} When I/Os Control Leds

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in Figure 28. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. Figure 29 shows a high-value resistor in parallel with the LED. Figure 30 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.

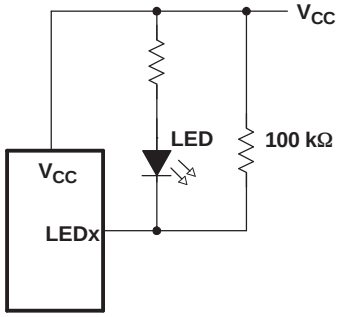


Figure 29. High-Value Resistor In Parallel With The Led

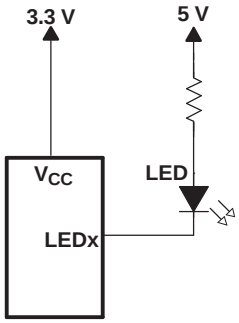
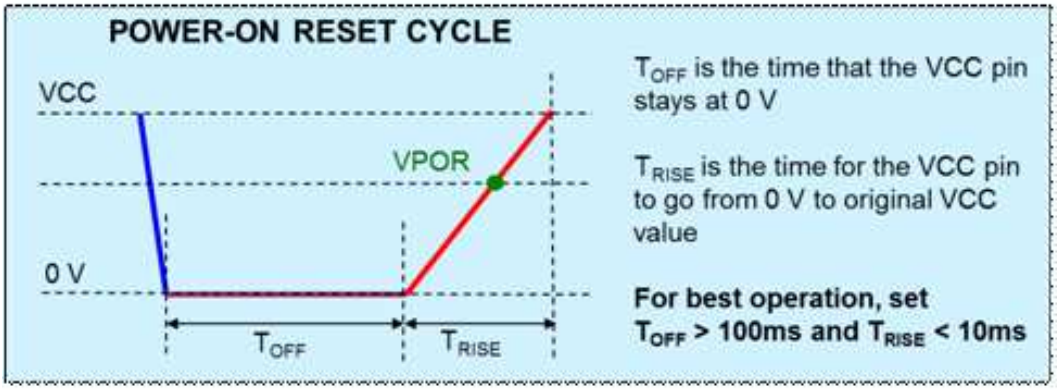


Figure 30. Device Supplied By A Lower Voltage

10 Power Supply Recommendations

10.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9554ADB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	Samples
PCA9554ADBQR	NRND	SSOP	DBQ	16		TBD	Call TI	Call TI	-40 to 85		
PCA9554ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	Samples
PCA9554ADGV	NRND	TVSOP	DGV	16		TBD	Call TI	Call TI	-40 to 85		
PCA9554ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	Samples
PCA9554ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	Samples
PCA9554ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9554A	Samples
PCA9554ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9554A	Samples
PCA9554ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9554A	Samples
PCA9554APW	NRND	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	
PCA9554APWG4	NRND	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	
PCA9554APWR	NRND	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	
PCA9554APWRG4	NRND	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A	
PCA9554ARGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVH	Samples
PCA9554ARGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD554A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

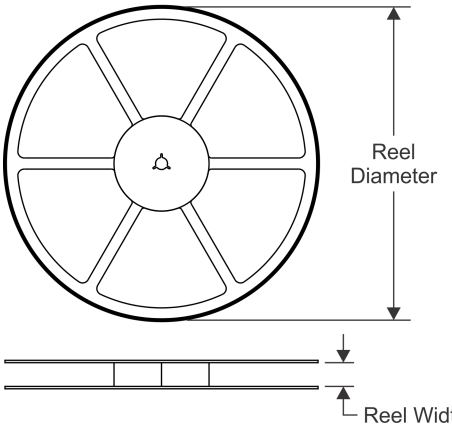
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

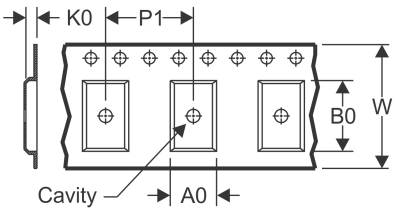
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

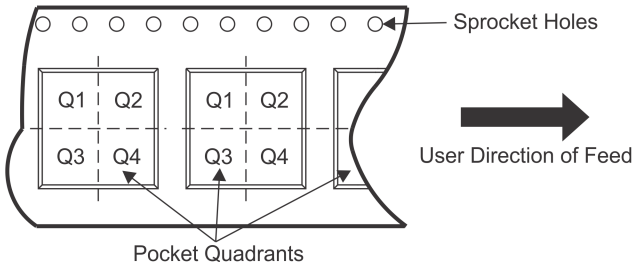


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

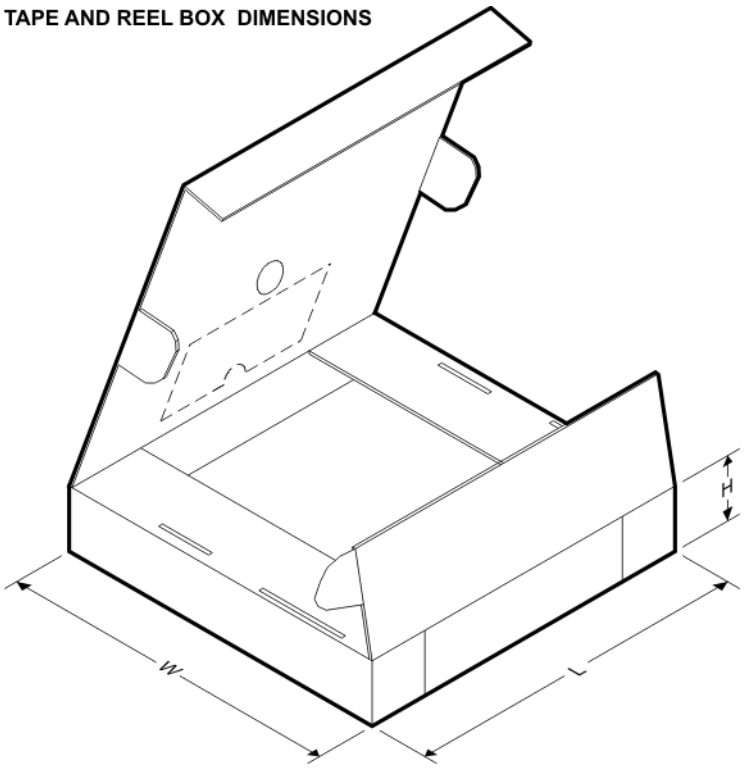
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9554ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
PCA9554ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9554ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9554APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9554ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PCA9554ARGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

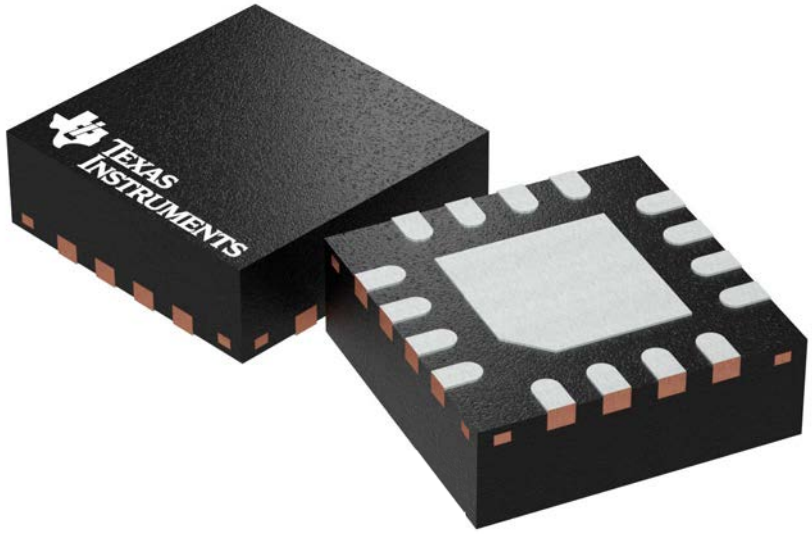


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9554ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
PCA9554ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
PCA9554ADWR	SOIC	DW	16	2000	367.0	367.0	38.0
PCA9554APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
PCA9554ARGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
PCA9554ARGVR	VQFN	RGV	16	2500	367.0	367.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



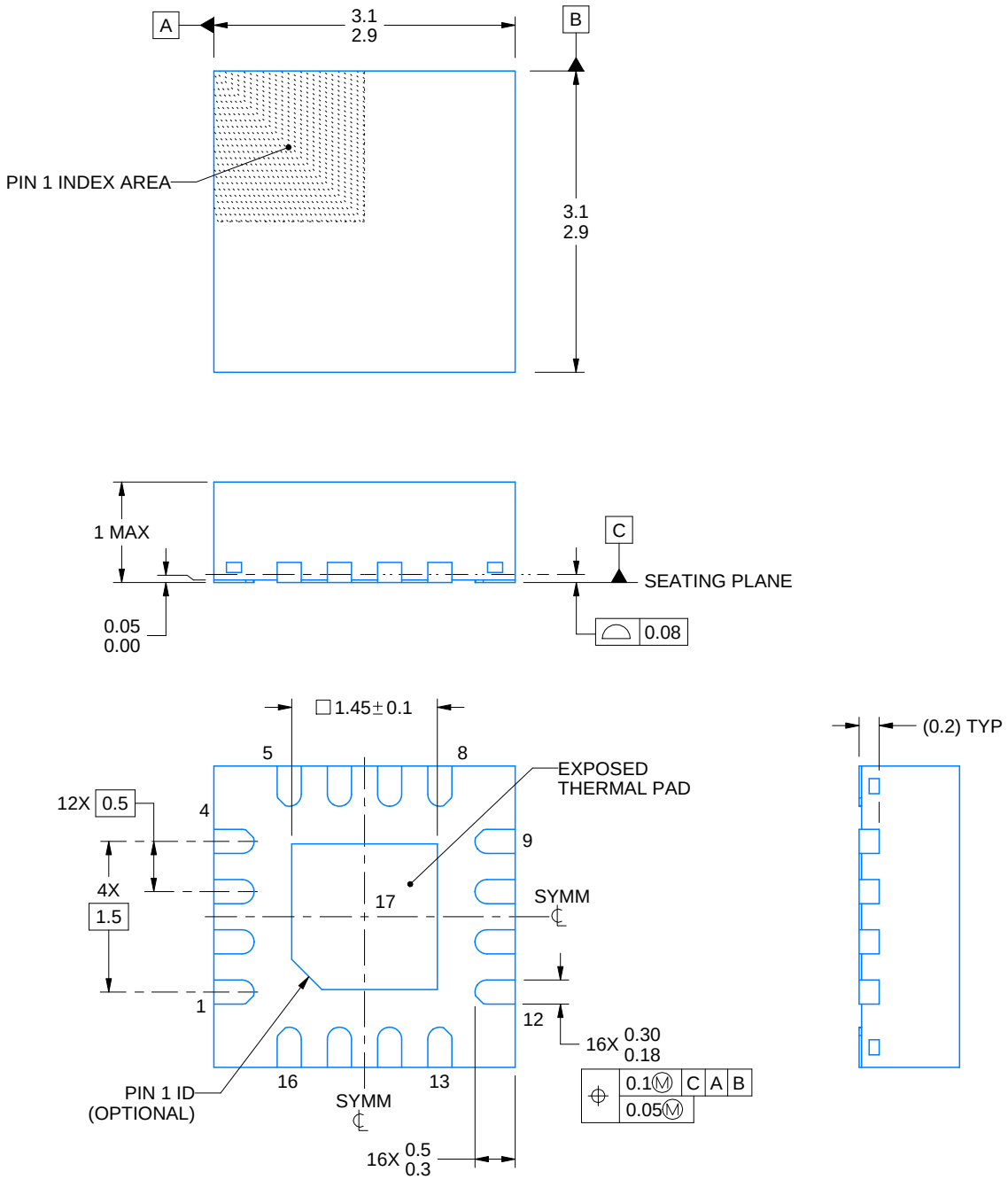
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

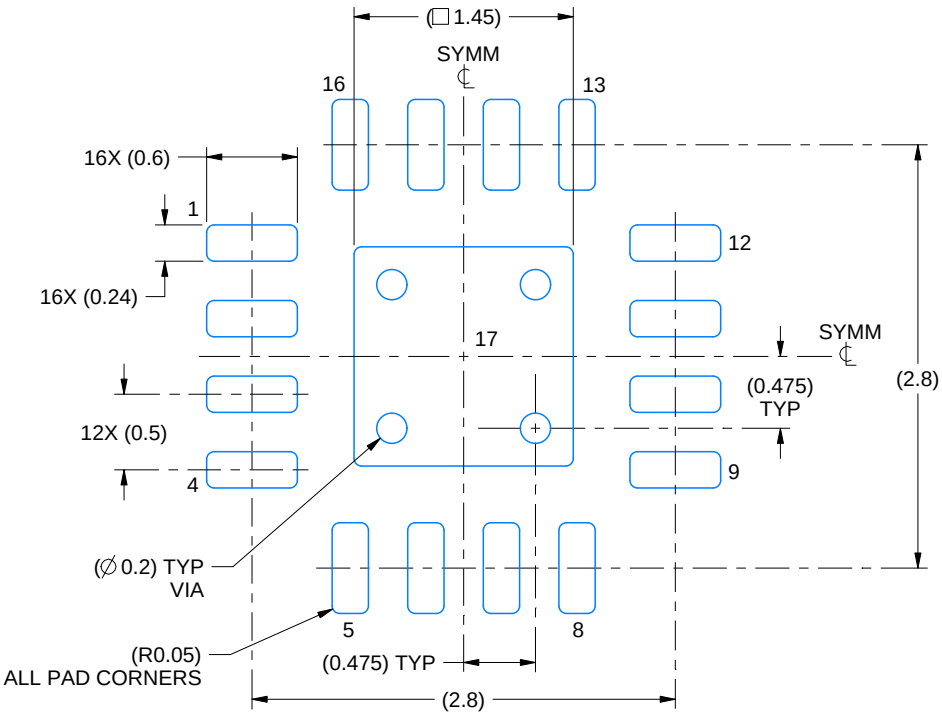
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

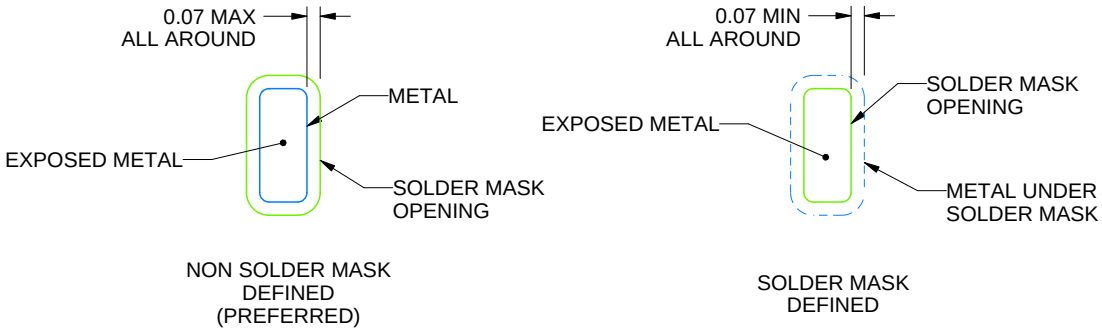


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

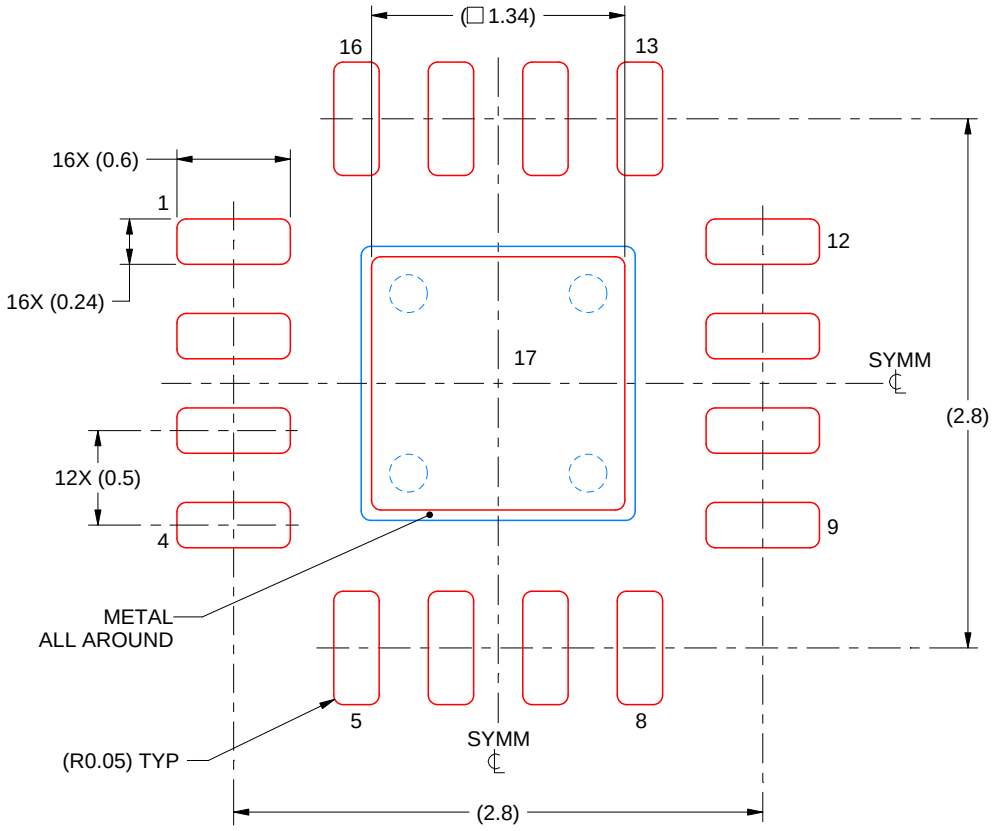


SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

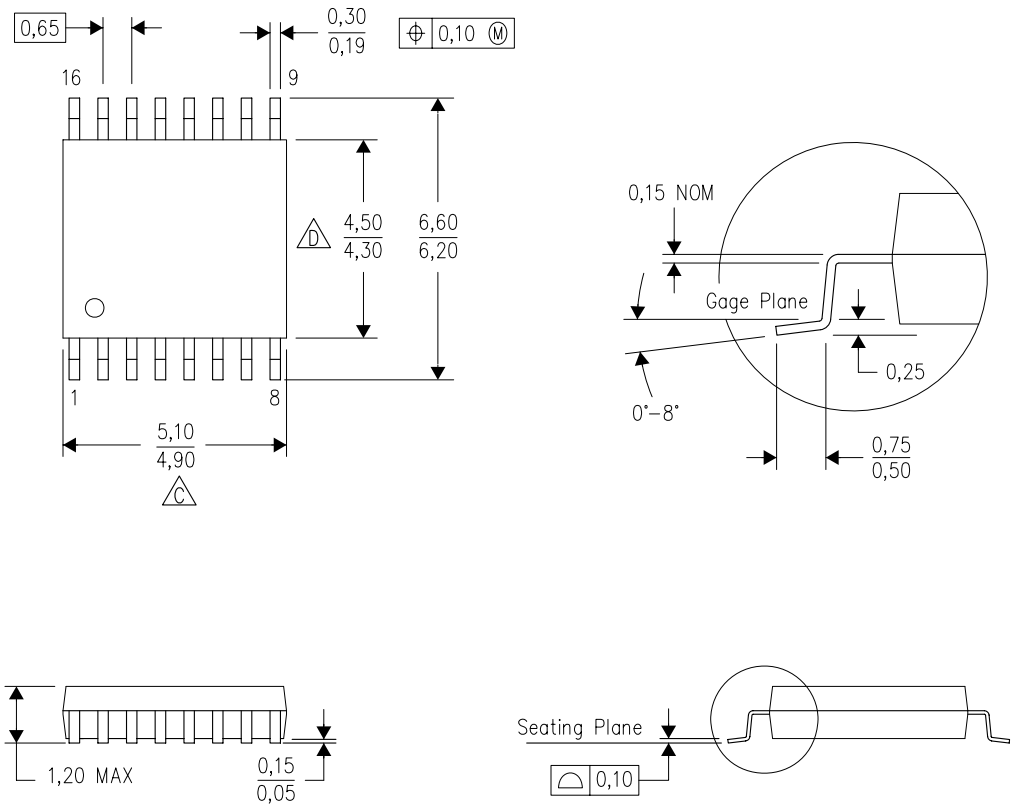
EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

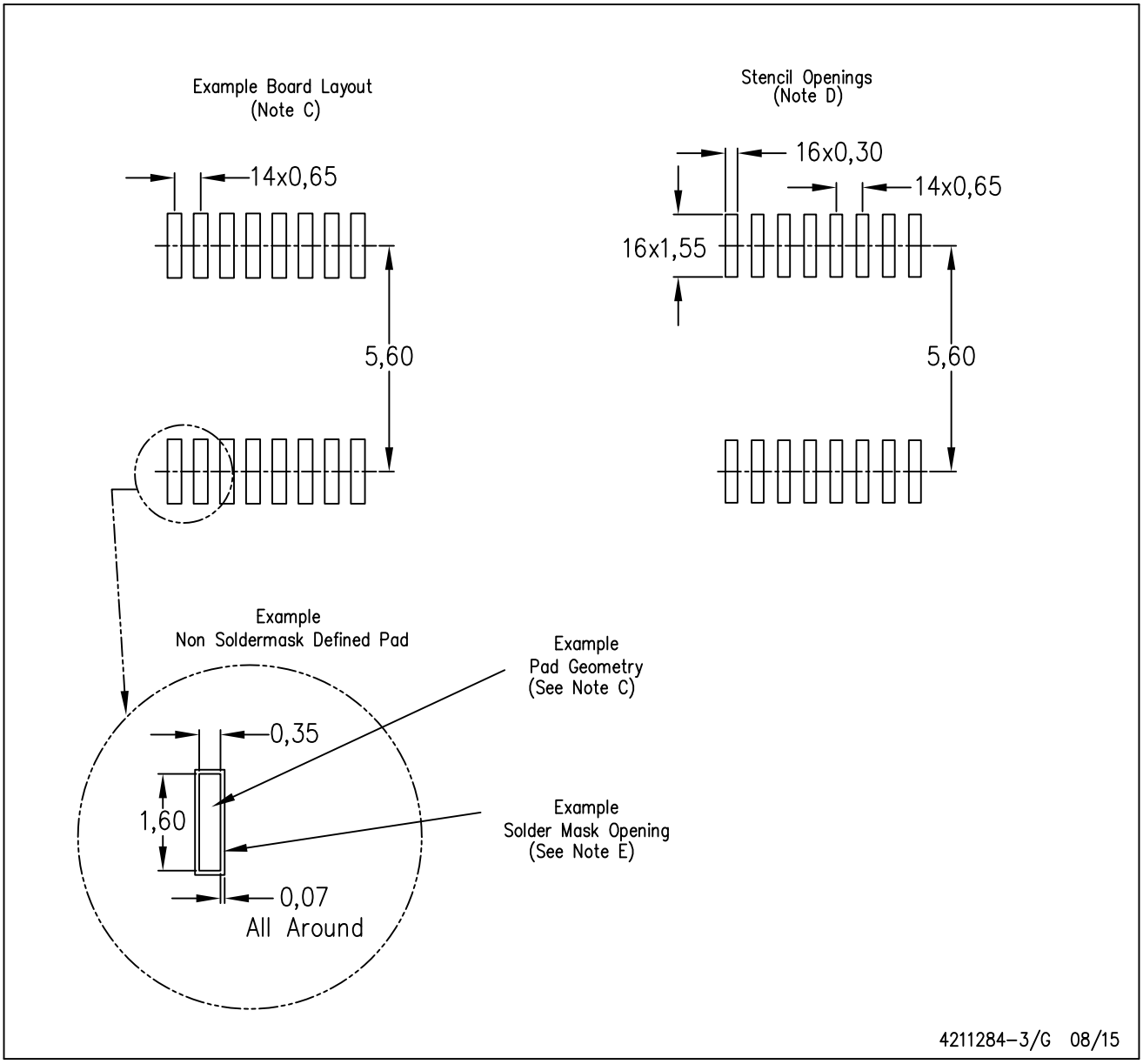
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

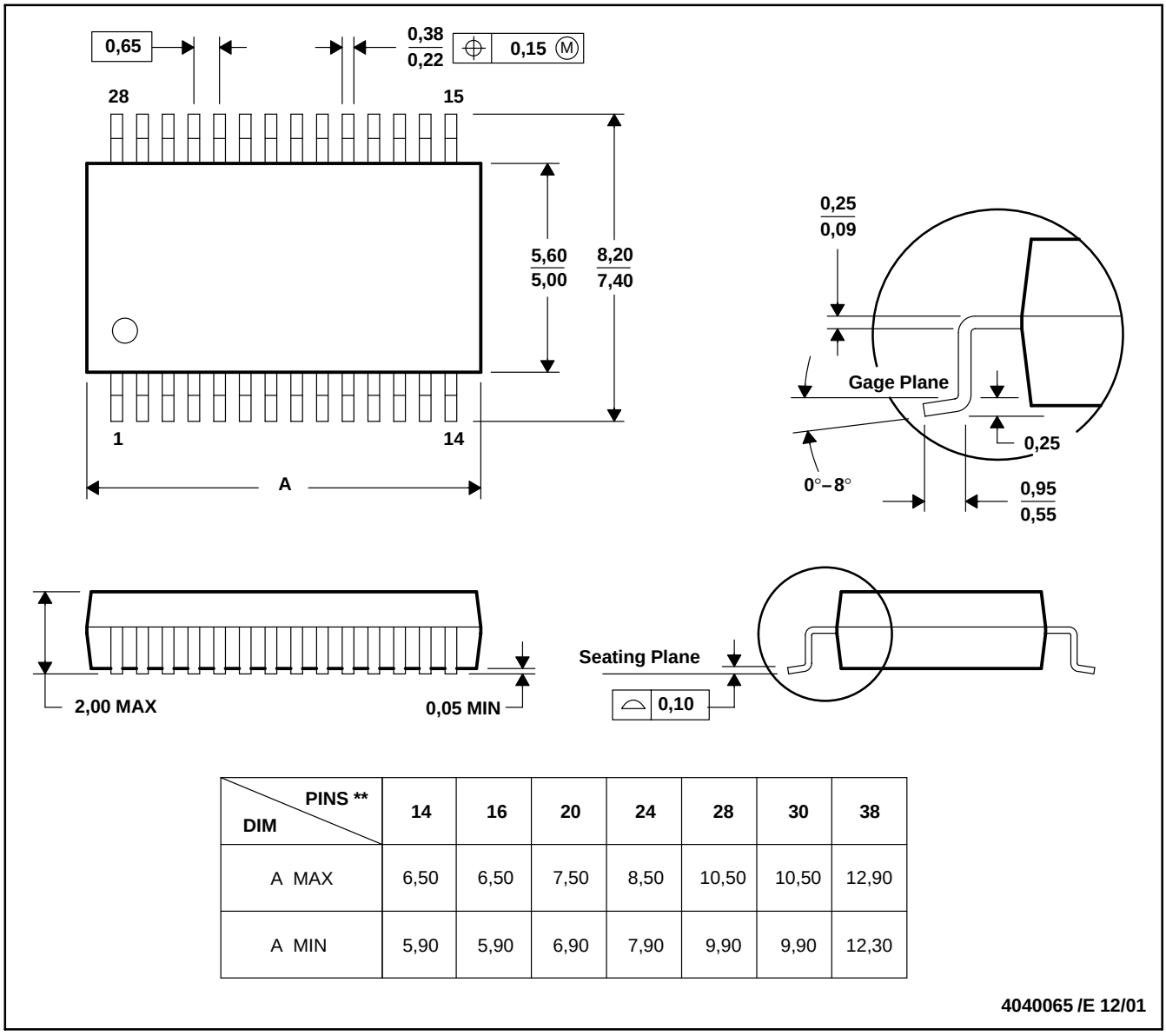


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

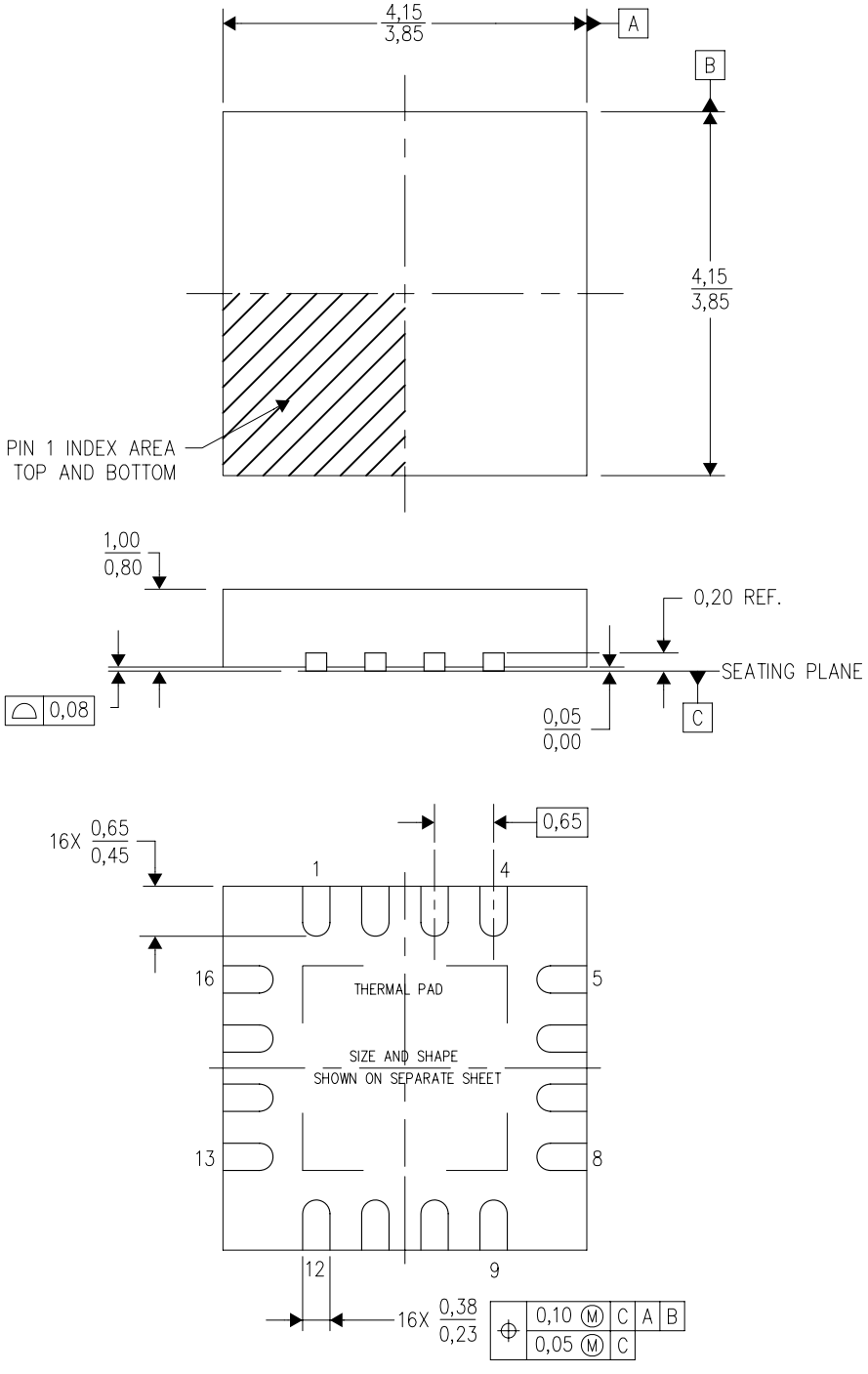


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

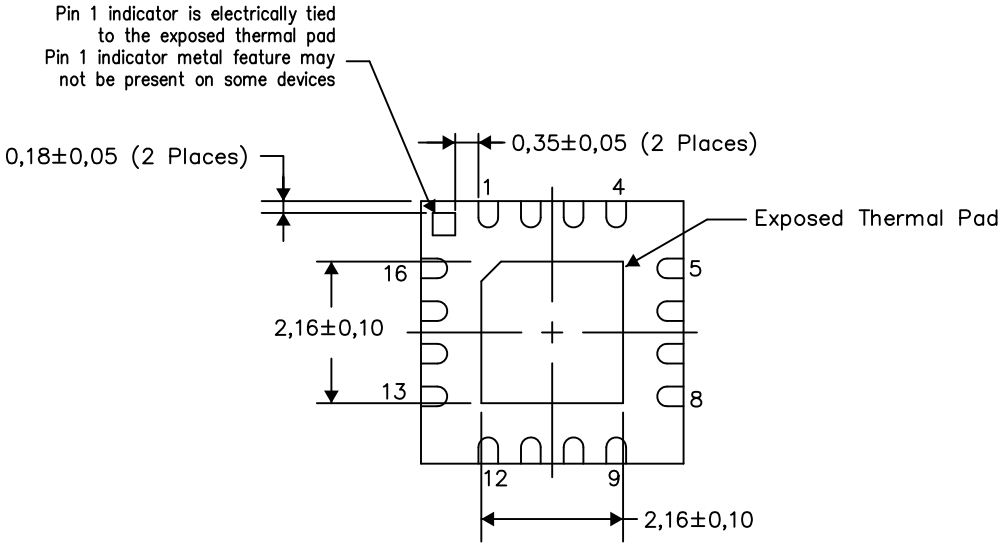
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



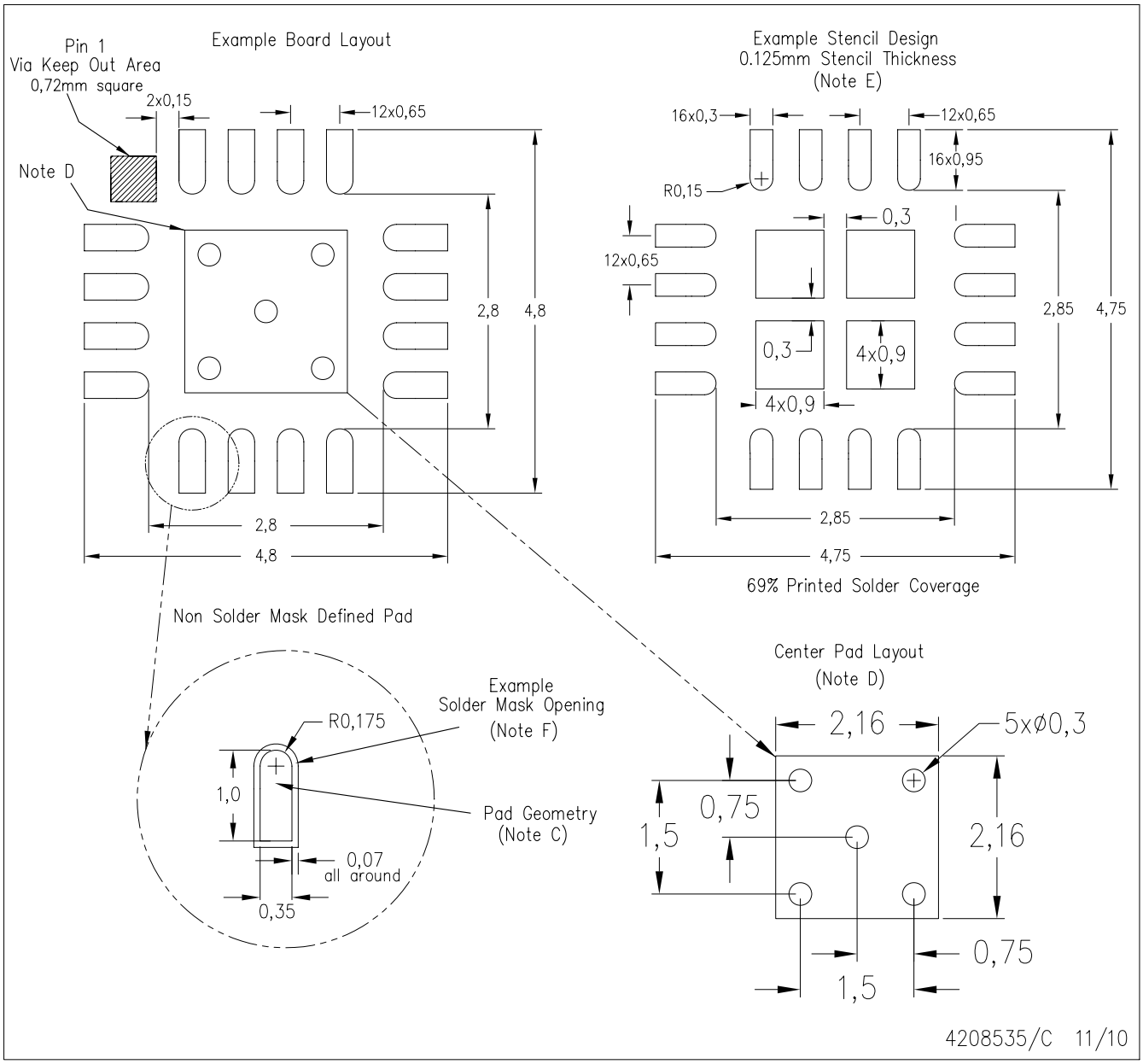
Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

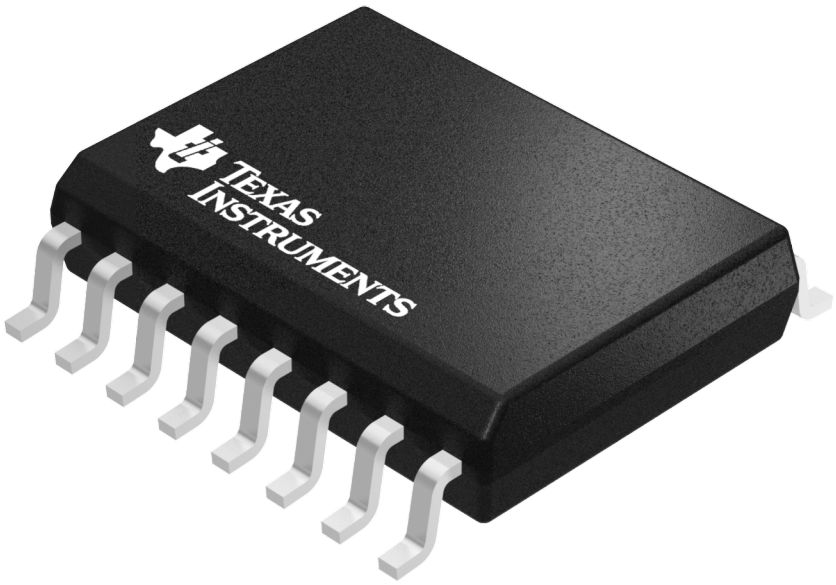


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

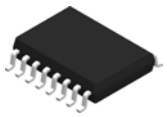
GENERIC PACKAGE VIEW

DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

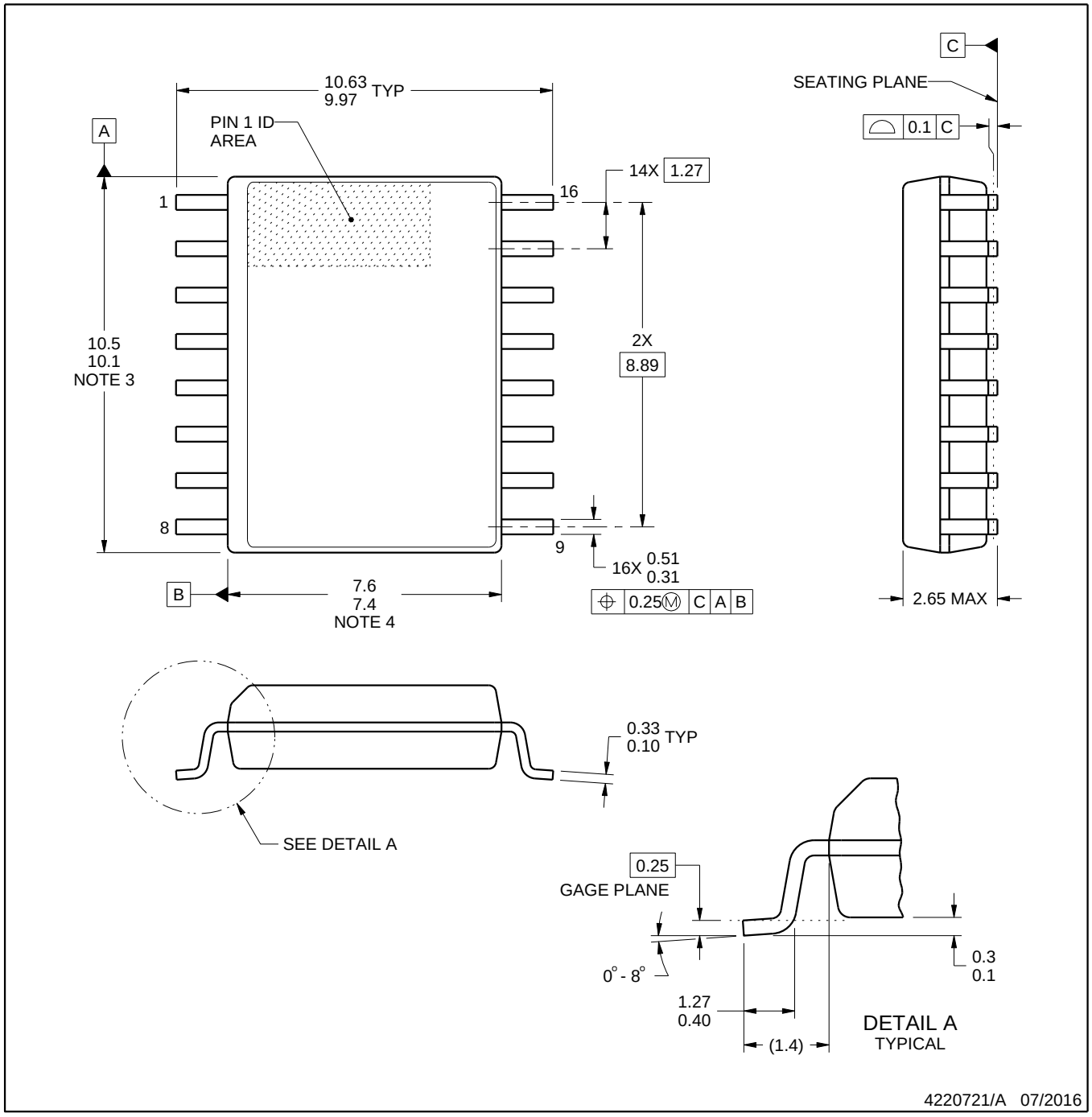


PACKAGE OUTLINE

DW0016A

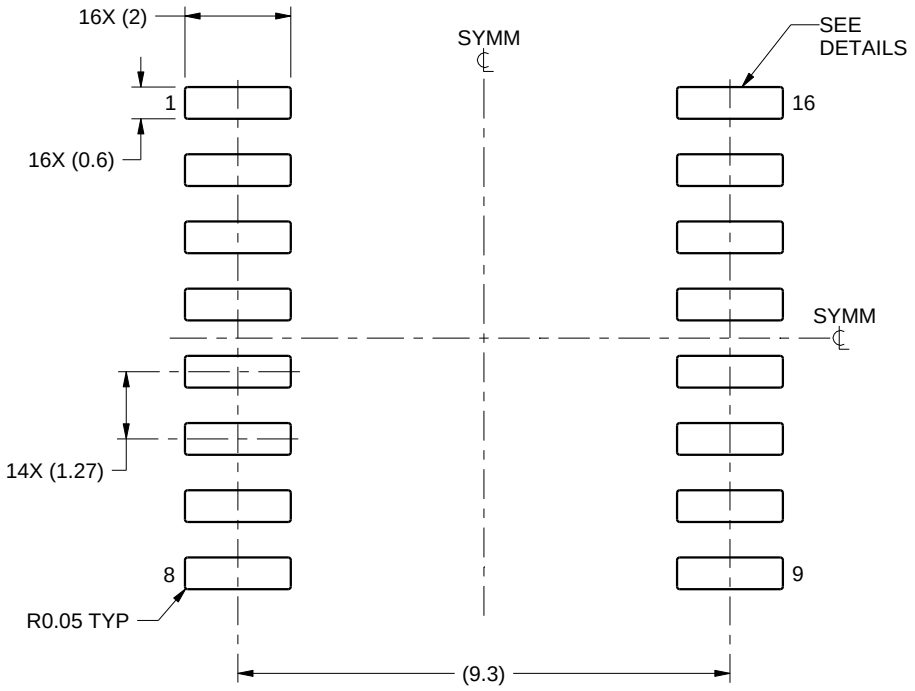
SOIC - 2.65 mm max height

SOIC

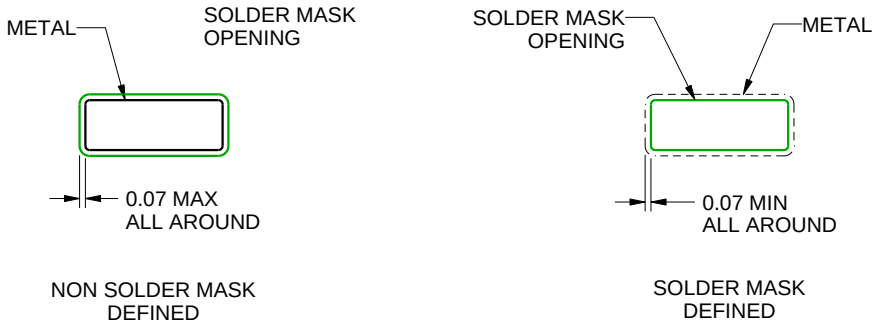


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

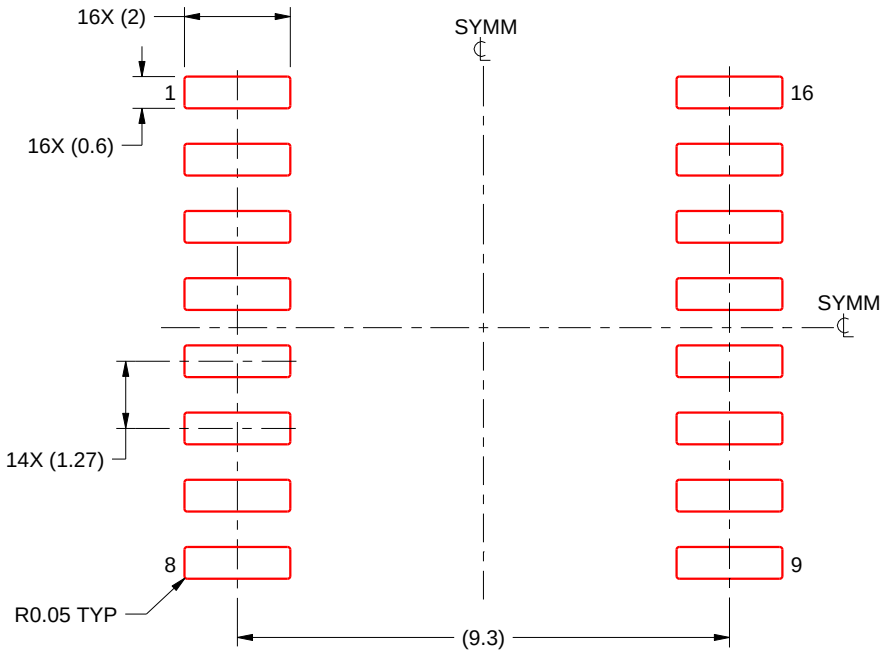


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

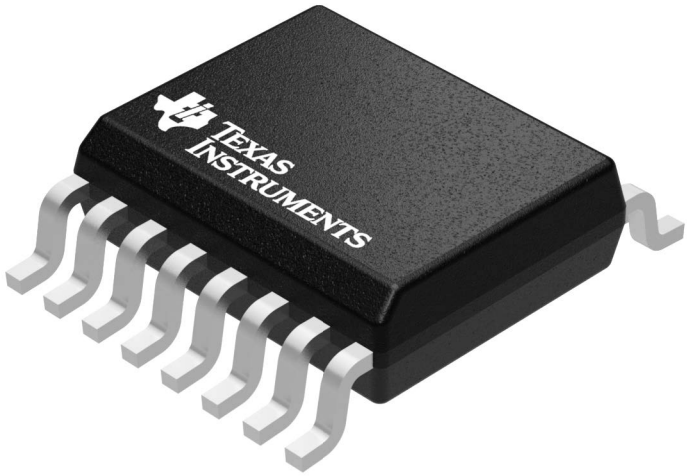
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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