TPS7A4001 100-V Input Voltage, 50-mA, Very High Voltage Linear Regulator

1 Features

- Very High Maximum Input Voltage: 100 V
- Wide Input Voltage Range: 7 to 100 V
- Accuracy:
  - Nominal: 1%
  - Over Line, Load, and Temperature: 2.5%
- Low Quiescent Current: 25 µA
- Quiescent Current at Shutdown: 4.1 µA
- Maximum Output Current: 50 mA
- CMOS Logic-Level-Compatible Enable Pin
- Adjustable Output Voltage from about 1.175 to 90 V
- Stable With Ceramic Capacitors:
  - Input Capacitance: ≥1 µF
  - Output Capacitance: ≥4.7 µF
- Dropout Voltage: 290 mV
- Built-In Current Limit and Thermal Shutdown Protection
- Package: High Thermal Performance HVSSOP PowerPAD™
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Microprocessors, Microcontrollers Powered by Industrial Busses With High Voltage Transients
- Industrial Automation
- Telecom Infrastructure
- Automotive
- Power over Ethernet (PoE)
- LED Lighting
- Bias Power Supplies

3 Description

The TPS7A4001 device is a very high voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (HVSSOP), and is able to withstand continuous DC or transient input voltages of up to 100 V.

The TPS7A4001 device is stable with any output capacitance greater than 4.7 µF and any input capacitance greater than 1 µF (over temperature and tolerance). Therefore, implementations of this device require minimal board space because of its miniaturized packaging (HVSSOP) and a potentially small output capacitor. In addition, the TPS7A4001 device offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode.

The TPS7A4001 device has an internal thermal shutdown and current limiting to protect the system during fault conditions. The HVSSOP packages has an operating temperature range of T_J = –40°C to 125°C.

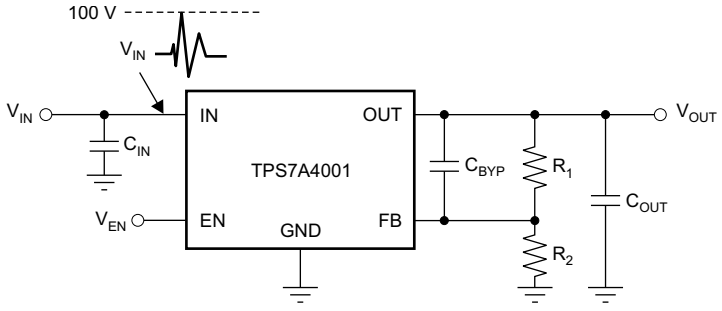
In addition, the TPS7A4001 device is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications; not only can it supply a well-regulated voltage rail, but it can also withstand and maintain regulation during very high and fast voltage transients. These features translate to simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications, including PoE, bias supply, and LED lighting.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A4001	HVSSOP (8)	3.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 9
8 Application and Implementation ... 10
8.1 Application Information ... 10
8.2 Typical Application ... 11
9 Power Supply Recommendations ... 12
10 Layout ... 13
10.1 Layout Guidelines ... 13
10.2 Layout Example ... 13
10.3 Thermal Considerations ... 13
10.4 Power Dissipation ... 14
11 Device and Documentation Support ... 15
11.1 Community Resources ... 15
11.2 Trademarks ... 15
11.3 Electrostatic Discharge Caution ... 15
11.4 Glossary ... 15
12 Mechanical, Packaging, and Orderable Information ... 15

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2011) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed Package from MSOP-8 to HVSSOP. ... 1
- Changed T_J value for disabled mode operating mode from 165 to 170°C ... 9
- Changed value from 35 to 45°C ... 14

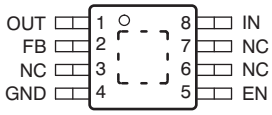
Changes from Original (March 2011) to Revision A — **Page**

- Changed all 105 V to 100 V on page 1 ... 1

Copyright © 2011–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Regulator output. A capacitor > 4.7 µF must be tied from this pin to ground to assure stability.
FB	2	O	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
NC	3	—	Not internally connected. This pin must either be left open or tied to GND.
	6		
	7		
GND	4	—	Ground
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_HI}$ the regulator is enabled. If $V_{EN} \leq V_{EN_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
IN	8	I	Input supply
PowerPAD	—	—	Solder to printed-circuit-board (PCB) to enhance thermal performance. **NOTE: The PowerPAD is internally connected to GND.** Although it can be left floating, TI highly recommends connecting the PowerPAD to the GND plane.

Copyright © 2011–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	105	V
	OUT pin to GND pin	–0.3	105	
	OUT pin to IN pin	–105	0.3	
	FB pin to GND pin	–0.3	2	
	FB pin to IN pin	–105	0.3	
	EN pin to IN pin	–105	0.3	
	EN pin to GND pin	–0.3	105	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN	7		100	V
VOUT	1.161		90	V
VEN	0		100	V
IOUT	0		50	mA

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A4001 DGN (HVVSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2011–2015, Texas Instruments Incorporated

6.5 Electrical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 7 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		7		100	V
V_{REF}	Internal reference	T_J = 25°C, V_{FB} = V_{REF}, V_{IN} = 9 V, I_{OUT} = 25 mA	1.161	1.173	1.185	V
V_{OUT}	Output voltage range(1)	V_{IN} ≥ $V_{OUT(NOM)}$ + 2 V	V_{REF}		90	V
	Nominal accuracy	T_J = 25°C, V_{IN} = 9 V, I_{OUT} = 25 mA	–1		1	$\%V_{OUT}$
	Overall accuracy	$V_{OUT(NOM)}$ + 2 V ≤ V_{IN} ≤ 24 V(2) 100 µA ≤ I_{OUT} ≤ 50 mA	–2.5		2.5	$\%V_{OUT}$
$\frac{\Delta\%V_{OUT}}{\Delta V_{IN}}$	Line regulation	7 V ≤ V_{IN} ≤ 100 V		0.03		$\%V_{OUT}$
$\frac{\Delta\%V_{OUT}}{\Delta I_{OUT}}$	Load regulation	100 µA ≤ I_{OUT} ≤ 50 mA		0.31		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 20 mA		290		mV
		V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 50mA		0.78	1.3	V
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 7 V, T_J ≤ 85°C	51	117	200	mA
		V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 9 V	51	128	200	mA
I_{GND}	Ground current	7 V ≤ V_{IN} ≤ 100 V, I_{OUT} = 0 mA		25	65	µA
		I_{OUT} = 50 mA		25		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		4.1	20	µA
I_{FB}	Feedback current(3)		–0.1	0.01	0.1	µA
I_{EN}	Enable current	7 V ≤ V_{IN} ≤ 100 V, V_{IN} = V_{EN}		0.02	1	µA
V_{EN_HI}	Enable high-level voltage		1.5		V_{IN}	V
V_{EN_LO}	Enable low- level voltage		0		0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = 12 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10 µF, BW = 10 Hz to 100 kHz		58		μV_{RMS}
		V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, BW = 10 Hz to 100 kHz		73		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, f = 100 Hz		65		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_J	Operating junction temperature		–40		125	°C

(1) To ensure stability at no-load conditions, a current from the feedback resistive network greater than or equal to 10µA is required.
(2) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT}$ = (24 V – V_{REF}) × 50 mA ≈ 1.14 W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
(3) I_{FB} > 0 flows out of the device.
(4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

Copyright © 2011–2015, Texas Instruments Incorporated

6.6 Typical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 9 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

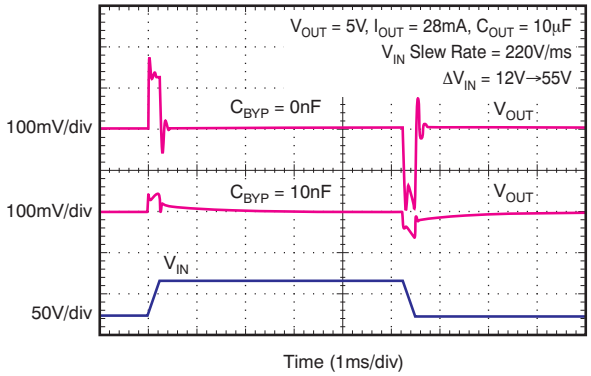


Figure 1. Line Transient Response vs C_{BYP}

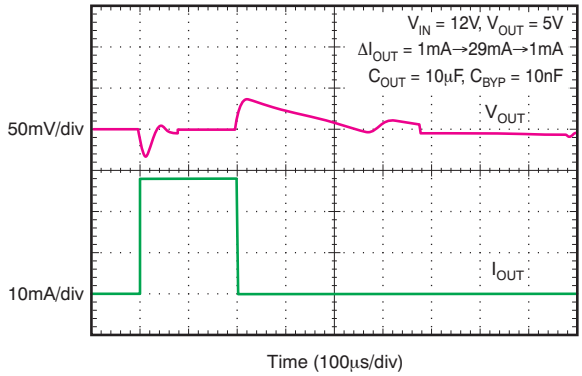


Figure 2. Load Transient Response

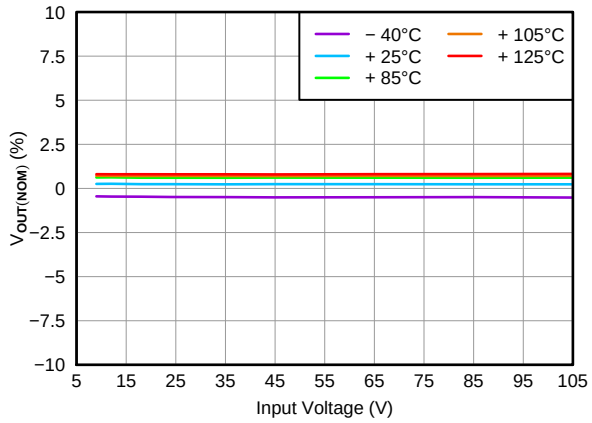


Figure 3. Line Regulation

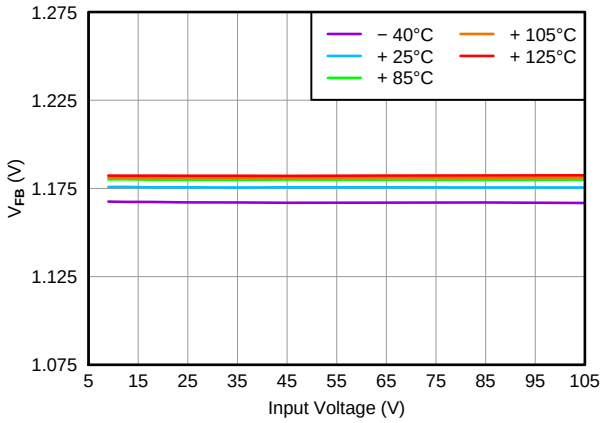


Figure 4. Feedback Voltage

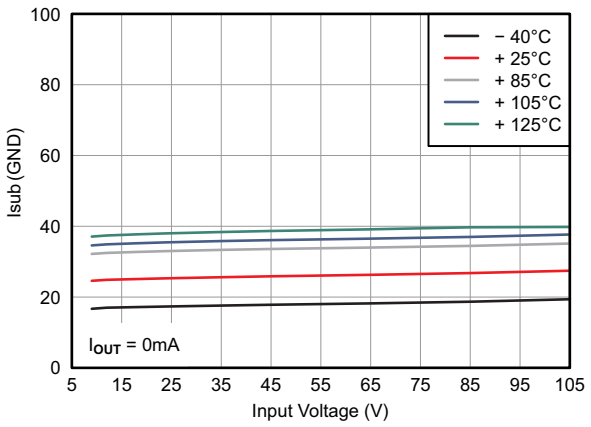


Figure 5. Ground Current vs Input Voltage

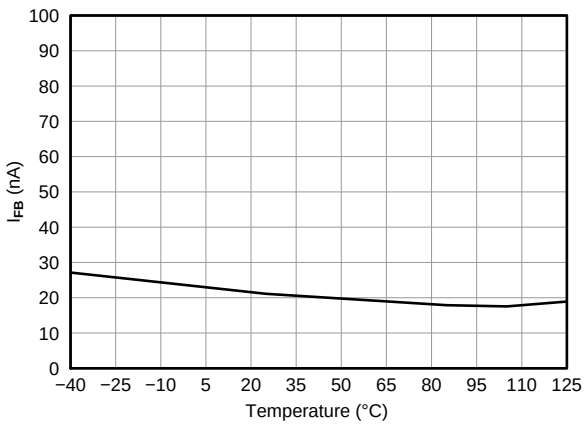


Figure 6. Feedback Current

Copyright © 2011–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 9 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

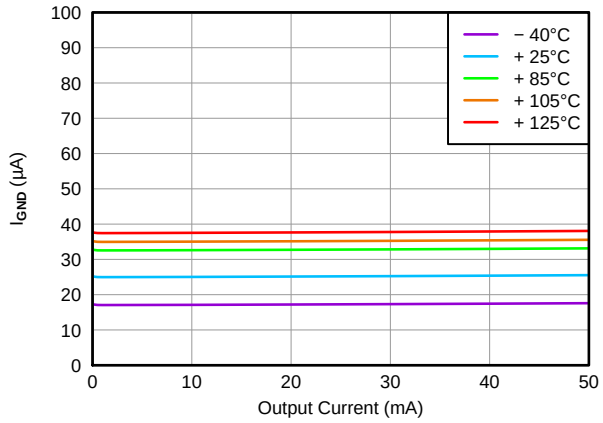


Figure 7. Ground Current vs Output Voltage

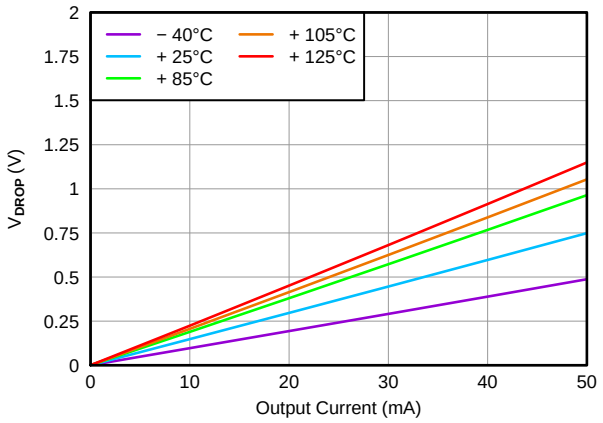


Figure 8. Dropout Voltage

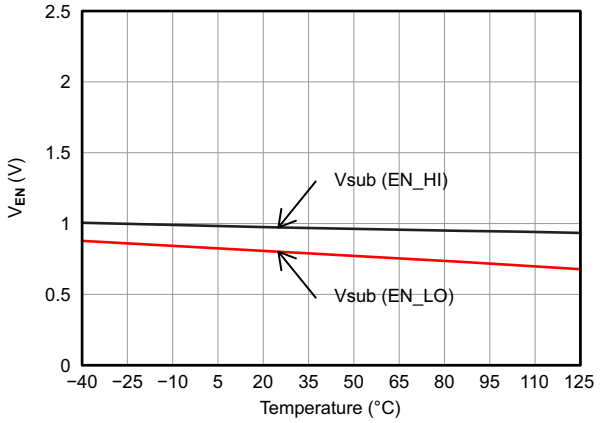


Figure 9. Enable Threshold Voltage

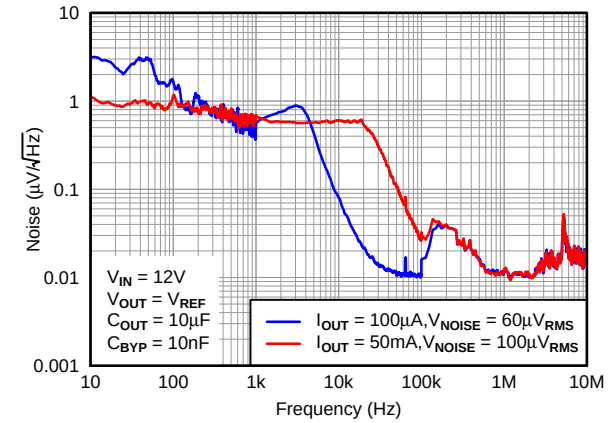


Figure 10. Output Spectral Noise Density

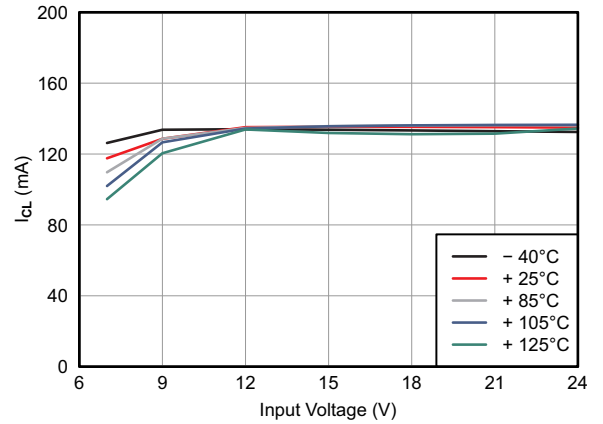


Figure 11. Current Limit

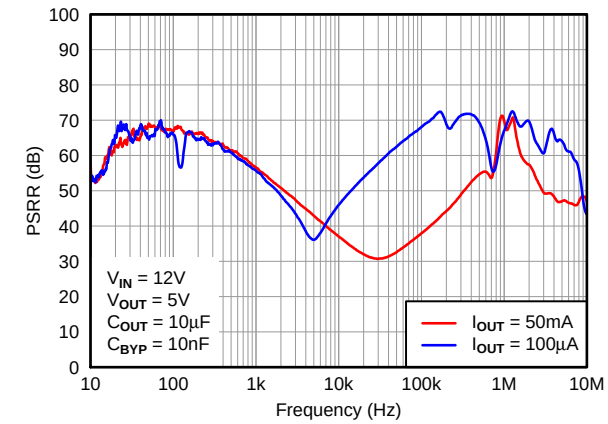


Figure 12. Power-Supply Rejection Ratio

Copyright © 2011–2015, Texas Instruments Incorporated

7 Detailed Description

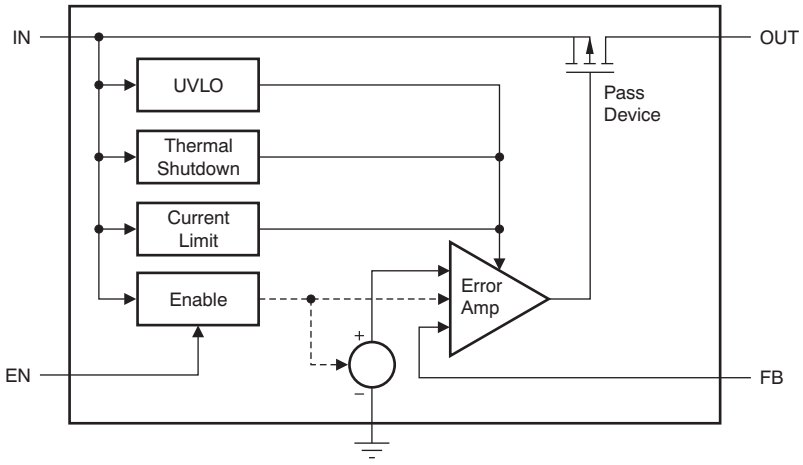
7.1 Overview

The TPS7A4001 device belongs to a new generation of linear regulators that use an innovative BiCMOS process technology to achieve very high maximum input and output voltages.

This process not only allows the TPS7A4001 device to maintain regulation during very fast high-voltage transients up to 105 V, but it also allows the TPS7A4001 device to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the ground current of the TPS7A4001 device is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance HVSSOP PowerPAD package, make this device ideal for industrial and telecom applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A4001 device helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (309 mA, typical), and is largely independent of output voltage. For reliable operation, the device does not operate in current limit for extended periods of time.

7.3.2 Enable Pin Operation

The TPS7A4001 device provides an enable pin (EN) feature that turns on the regulator when $V_{EN} > V_{EN_HI}$, and disables the regulator when $V_{EN} < V_{EN_LO}$.

7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

Copyright © 2011–2015, Texas Instruments Incorporated

Feature Description (continued)

The internal protection circuitry of the TPS7A4001 device has been designed to protect against overload conditions. The protection circuitry was not intended to replace proper heatsinking. Continuously running the TPS7A4001 device into thermal shutdown degrades device reliability.

7.3.4 Undervoltage Lockout (UVLO)

The TPS7A4001 contains an Undervoltage Lockout comparator that ensures the error amplifier is disabled when the input voltage is below the required minimum operational voltage. The minimum recommended operational voltage is 7 V.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN_HI}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN_HI}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN_LO}$	—	$T_J > 170°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

One of the primary applications of the TPS7A4001 device is to provide transient voltage protection to sensitive circuitry that may be damaged in the presence of high-voltage spikes.

This transient voltage protection can be more cost-effective and compact compared to topologies that use a transient voltage suppression (TVS) block.

8.1.1 Adjustable Operation

The TPS7A4001 device has an output voltage range of about 1.175 to 90 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 13.

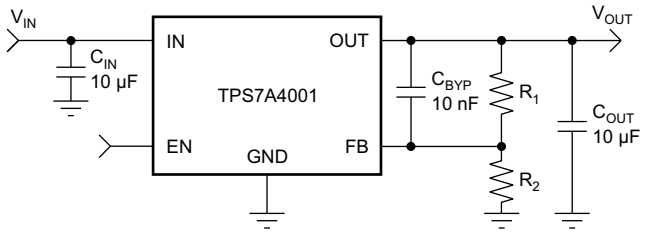


Figure 13. Adjustable Operation for Maximum AC Performance

Calculate R_1 and R_2 for any output voltage range using the formula shown in Equation 1. To ensure stability under no-load conditions, this resistive network must provide a current ≥ 10 µA.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 10\mu A \tag{1}$$

If greater voltage accuracy is required, consider the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

Copyright © 2011–2015, Texas Instruments Incorporated

8.2 Typical Application

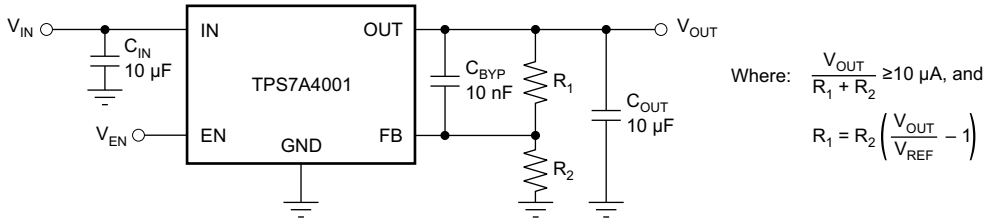


Figure 14. Example Circuit to Maximize Transient Performance

8.2.1 Design Requirements

For this design example, use the following parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
V_{IN}	12 V, with 55 V surge tolerance
V_{OUT}	5 V (ideal), 4.981 (actual)
I_{OUT}	28 mA
Accuracy	5 %
R1, R2	162 kΩ, 49.9 kΩ

8.2.2 Detailed Design Procedure

The maximum value of total feedback resistance can be calculated to be 500 kΩ. Equation 1 was used to calculate R1 and R2, and standard 1% resistors were selected to keep the accuracy within the 5% allocation. 10-uF ceramic input and output capacitors were selected, along with a 10-nF bypass capacitor for optimal AC performance.

8.2.2.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are required. Ceramic X7R capacitors offer improved voltage and temperature coefficients, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

NOTE

High ESR capacitors may degrade PSRR.

8.2.2.2 Input and Output Capacitor Requirements

The TPS7A4001 device high voltage linear regulator achieves stability with a minimum output capacitance of 4.7 µF and input capacitance of 1 µF; however, TI highly recommends to use 10-µF output and input capacitors to maximize AC performance.

8.2.2.3 Bypass Capacitor Requirements

Although a bypass capacitor (C_{BYP}) is not needed to achieve stability, TI highly recommends using a 10-nF bypass capacitor to maximize AC performance (including line transient, noise, and PSRR). For additional information regarding the performance improvements of using a bypass capacitor, see .

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

The presence of the C_{BYP} capacitor may greatly improve the line transient response of the TPS7A4001 device, as shown in Figure 1.

Copyright © 2011–2015, Texas Instruments Incorporated

8.2.3 Application Curves

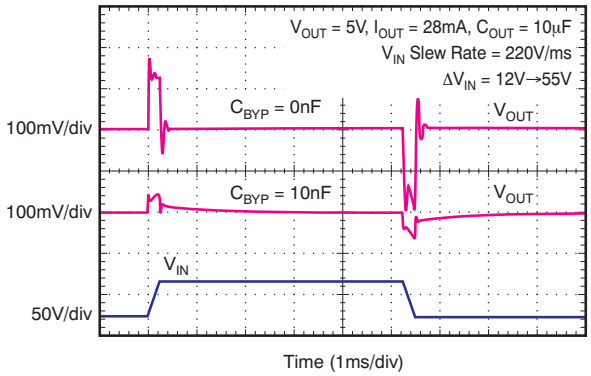


Figure 15. Line Transient Response vs C_{BYP}

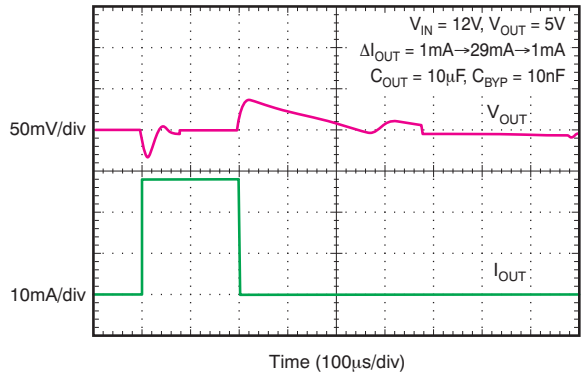


Figure 16. Load Transient Response

9 Power Supply Recommendations

The input supply for the LDO should not exceed its recommended operating conditions (7 V to 100 V). The input voltage should provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance. The input and output supplies should also be bypassed with 10-µF capacitors located near the input and output pins. There should be no other components located between these capacitors and the pins.

Copyright © 2011–2015, Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{BYP}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7A40 evaluation board, available at www.ti.com.

10.2 Layout Example

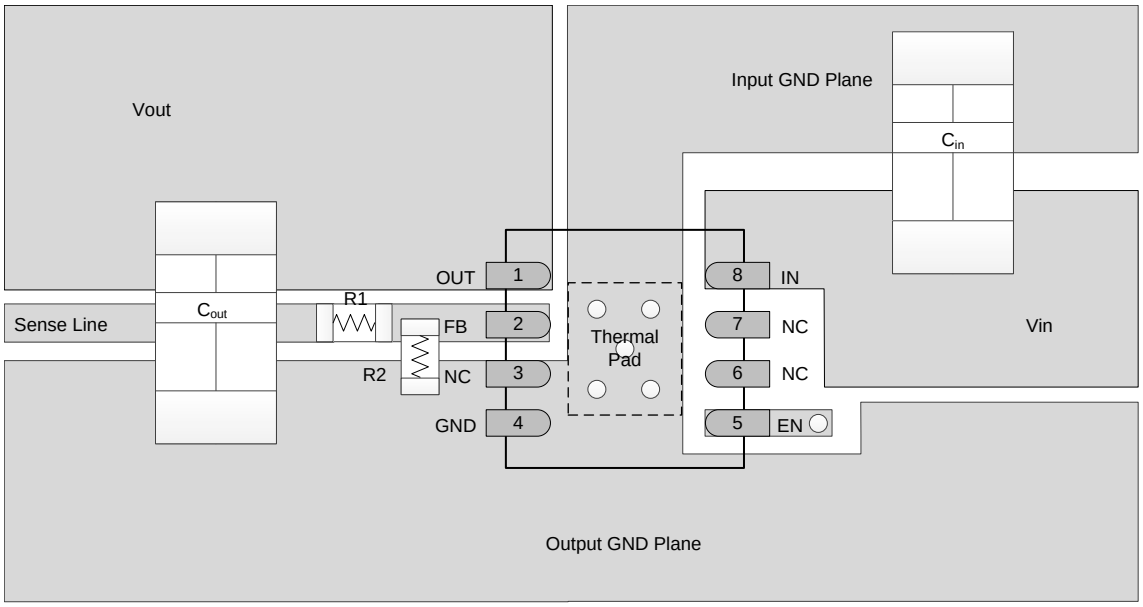


Figure 17. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Copyright © 2011–2015, Texas Instruments Incorporated

Thermal Considerations (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4001 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A4001 device into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT})\ I_{OUT} \quad (2)$$

Copyright © 2011–2015, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2011–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4001DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVQ	Samples
TPS7A4001DGNT	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

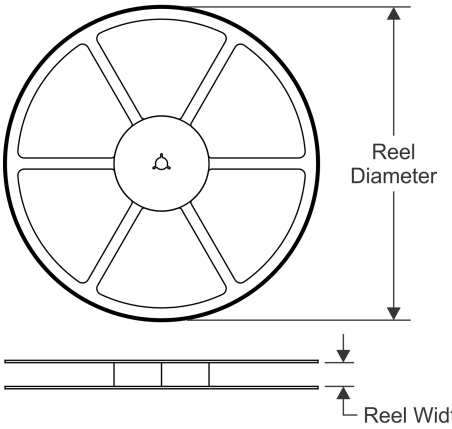
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

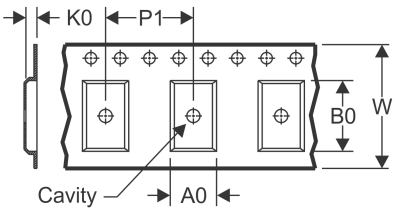
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

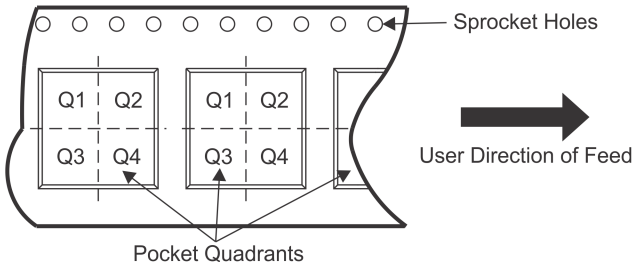


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

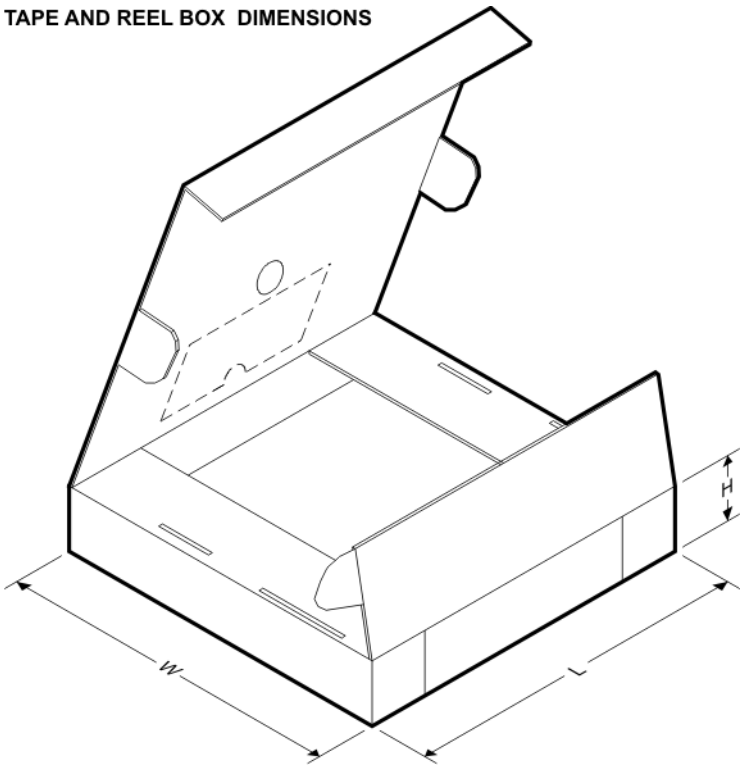
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4001DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A4001DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

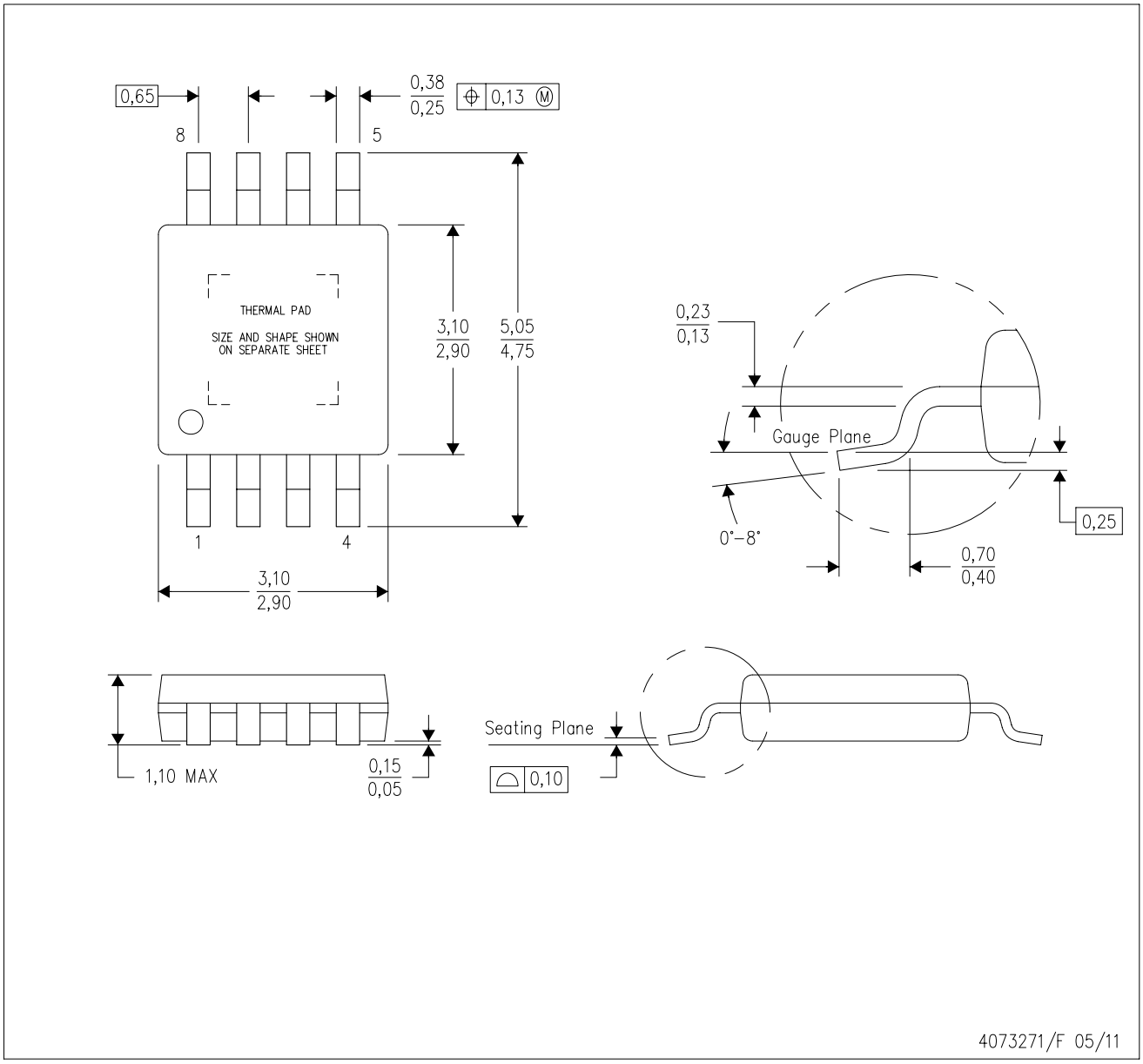
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4001DGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS7A4001DGNT	MSOP-PowerPAD	DGN	8	250	195.0	200.0	45.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

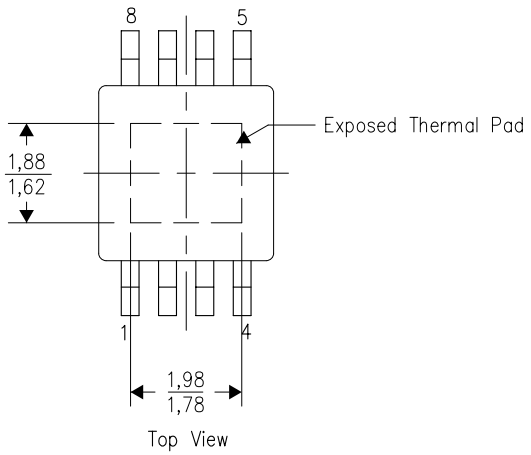
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



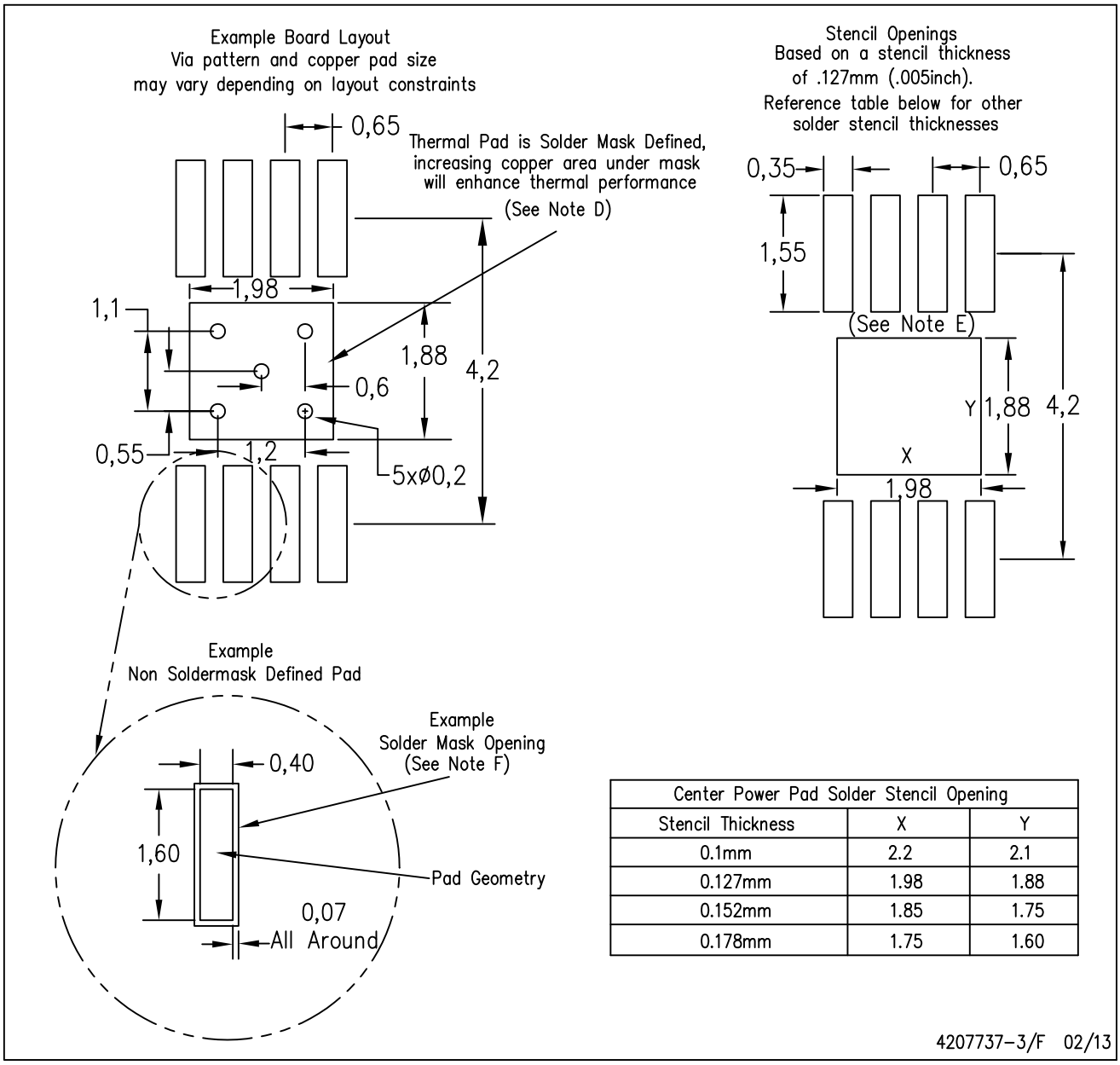
Exposed Thermal Pad Dimensions

4206323–3/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.2	2.1
0.127mm	1.98	1.88
0.152mm	1.85	1.75
0.178mm	1.75	1.60

4207737–3/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated