

CSD18536KCS 60 V N-Channel NexFET™ Power MOSFET

1 Features

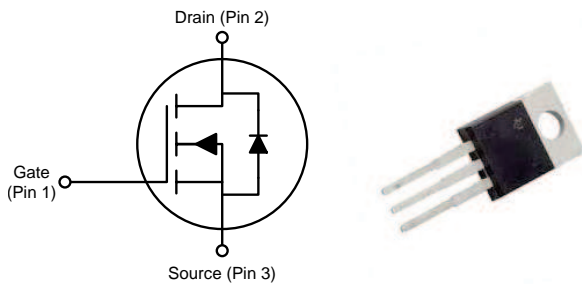
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 60 V, 1.3 mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

| $T_A = 25^\circ\text{C}$ | | TYPICAL VALUE | | UNIT |
|--------------------------|-------------------------------|-------------------------|-----|------|
| V_{DS} | Drain-to-Source Voltage | 60 | | V |
| Q_g | Gate Charge Total (10 V) | 108 | | nC |
| Q_{gd} | Gate Charge Gate-to-Drain | 14 | | nC |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS} = 4.5\text{ V}$ | 1.7 | mΩ |
| | | $V_{GS} = 10\text{ V}$ | 1.3 | mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 1.8 | | V |

Ordering Information⁽¹⁾

| Device | Package | Media | Qty | Ship |
|-------------|------------------------|-------|-----|------|
| CSD18536KCS | TO-220 Plastic Package | Tube | 50 | Tube |

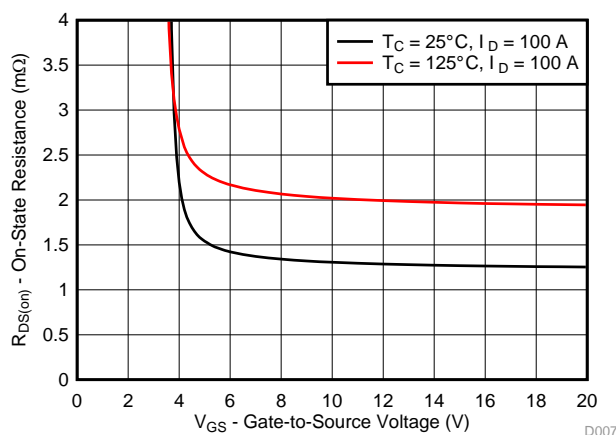
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ | | VALUE | UNIT |
|--------------------------|---|------------|------------------|
| V_{DS} | Drain-to-Source Voltage | 60 | V |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| I_D | Continuous Drain Current (Package limited) | 200 | A |
| | Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$ | 349 | |
| | Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$ | 247 | |
| I_{DM} | Pulsed Drain Current ⁽¹⁾ | 400 | A |
| P_D | Power Dissipation | 375 | W |
| T_J, T_{stg} | Operating Junction and Storage Temperature Range | -55 to 175 | $^\circ\text{C}$ |
| E_{AS} | Avalanche Energy, single pulse $I_D = 128\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$ | 819 | mJ |

(1) Max $R_{\theta JC} = 0.4^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$.

$R_{DS(on)}$ vs V_{GS}



Gate Charge

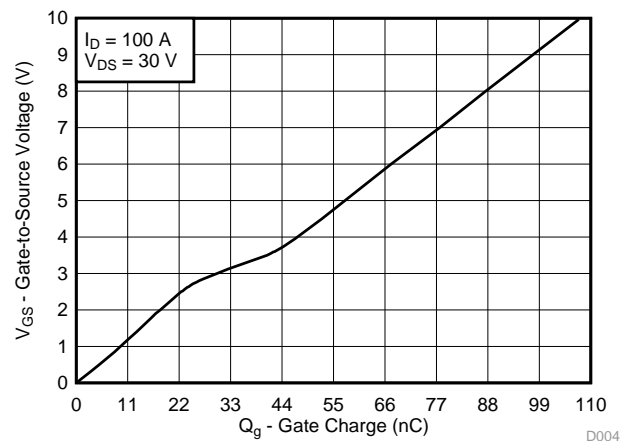


Table of Contents

| | | | |
|---|----------|---|----------|
| 1 Features | 1 | 6 Device and Documentation Support | 7 |
| 2 Applications | 1 | 6.1 Community Resources..... | 7 |
| 3 Description | 1 | 6.2 Trademarks | 7 |
| 4 Revision History | 2 | 6.3 Electrostatic Discharge Caution | 7 |
| 5 Specifications | 3 | 6.4 Glossary | 7 |
| 5.1 Electrical Characteristics..... | 3 | 7 Mechanical, Packaging, and Orderable Information | 8 |
| 5.2 Thermal Information | 3 | 7.1 KCS Package Dimensions..... | 8 |
| 5.3 Typical MOSFET Characteristics..... | 4 | | |

4 Revision History

Changes from Original (March 2015) to Revision A

Page

| | |
|--|----------|
| • Updated Gate Charge curve | 1 |
| • Changed C_{OSS} values From: TYP = 1700 pF MAX = 2210 pF To: TYP = 1410 pF MAX = 1840 pF in <i>Dynamic Characteristics</i> | 3 |
| • Changed Q_g values From: TYP = 83 nC MAX = 108 nC To: TYP = 108 nC MAX = 140 nC in the <i>Dynamic Characteristics</i> | 3 |
| • Changed $Q_{g(th)}$ value From: 12 nC To: 17 nC in the <i>Dynamic Characteristics</i> | 3 |
| • Changed $t_{d(on)}$ value From: 8 ns To: 11 ns in <i>Dynamic Characteristics</i> | 3 |
| • Changed t_r value From: 17 ns To: 5 ns in <i>Dynamic Characteristics</i> | 3 |
| • Changed $t_{d(off)}$ value From: 23 ns To: 24 ns in <i>Dynamic Characteristics</i> | 3 |
| • Changed t_f value From: 12 ns To: 4 ns in <i>Dynamic Characteristics</i> | 3 |
| • Updated Figure 4 | 4 |
| • Updated Figure 5 | 4 |
| • Added Community Resources | 7 |

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|--|-----|------|-------|---------------|
| STATIC CHARACTERISTICS | | | | | | |
| V_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 60 | | | V |
| I_{DSS} | Drain-to-Source Leakage Current | $V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate-to-Source Leakage Current | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-Source Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 1.4 | 1.8 | 2.2 | V |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS} = 4.5\text{ V}, I_D = 100\text{ A}$ | | 1.7 | 2.2 | m Ω |
| | | $V_{GS} = 10\text{ V}, I_D = 100\text{ A}$ | | 1.3 | 1.6 | m Ω |
| g_{fs} | Transconductance | $V_{DS} = 6\text{ V}, I_D = 100\text{ A}$ | | 312 | | S |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C_{iss} | Input Capacitance | $V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$ | | 8790 | 11430 | pF |
| C_{oss} | Output Capacitance | | | 1410 | 1840 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 39 | 51 | pF |
| R_G | Series Gate Resistance | | | 0.7 | 1.4 | Ω |
| Q_g | Gate Charge Total (10 V) | $V_{DS} = 30\text{ V}, I_D = 100\text{ A}$ | | 108 | 140 | nC |
| Q_{gd} | Gate Charge Gate-to-Drain | | | 14 | | nC |
| Q_{gs} | Gate Charge Gate-to-Source | | | 18 | | nC |
| $Q_{g(th)}$ | Gate Charge at V_{th} | | | 17 | | nC |
| Q_{oss} | Output Charge | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$ | | 230 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 100\text{ A}, R_G = 0\ \Omega$ | | 11 | | ns |
| t_r | Rise Time | | | 5 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 24 | | ns |
| t_f | Fall Time | | | 4 | | ns |
| DIODE CHARACTERISTICS | | | | | | |
| V_{SD} | Diode Forward Voltage | $I_{SD} = 100\text{ A}, V_{GS} = 0\text{ V}$ | | 0.9 | 1.0 | V |
| Q_{rr} | Reverse Recovery Charge | $V_{DS} = 30\text{ V}, I_F = 100\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$ | | 323 | | nC |
| t_{rr} | Reverse Recovery Time | | | 86 | | ns |

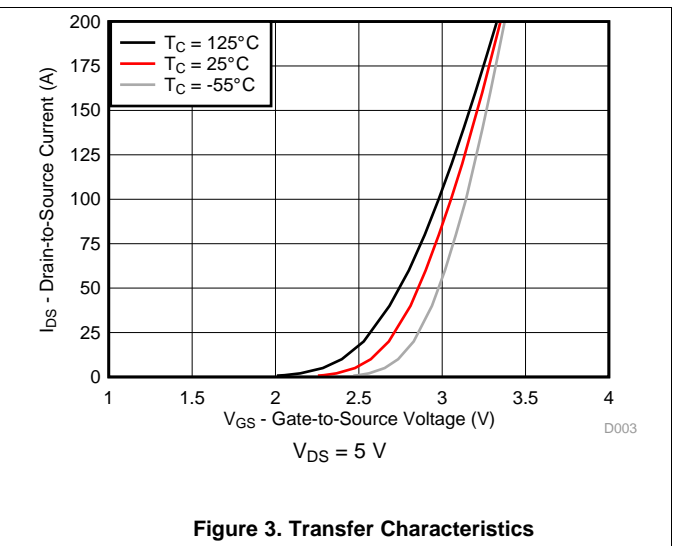
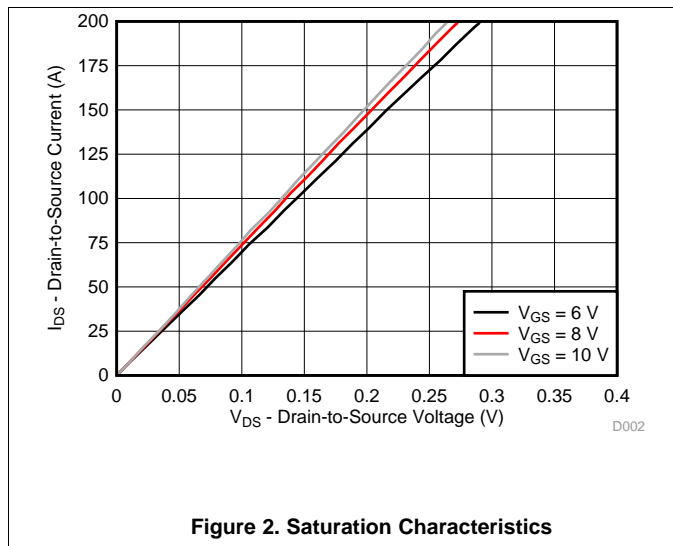
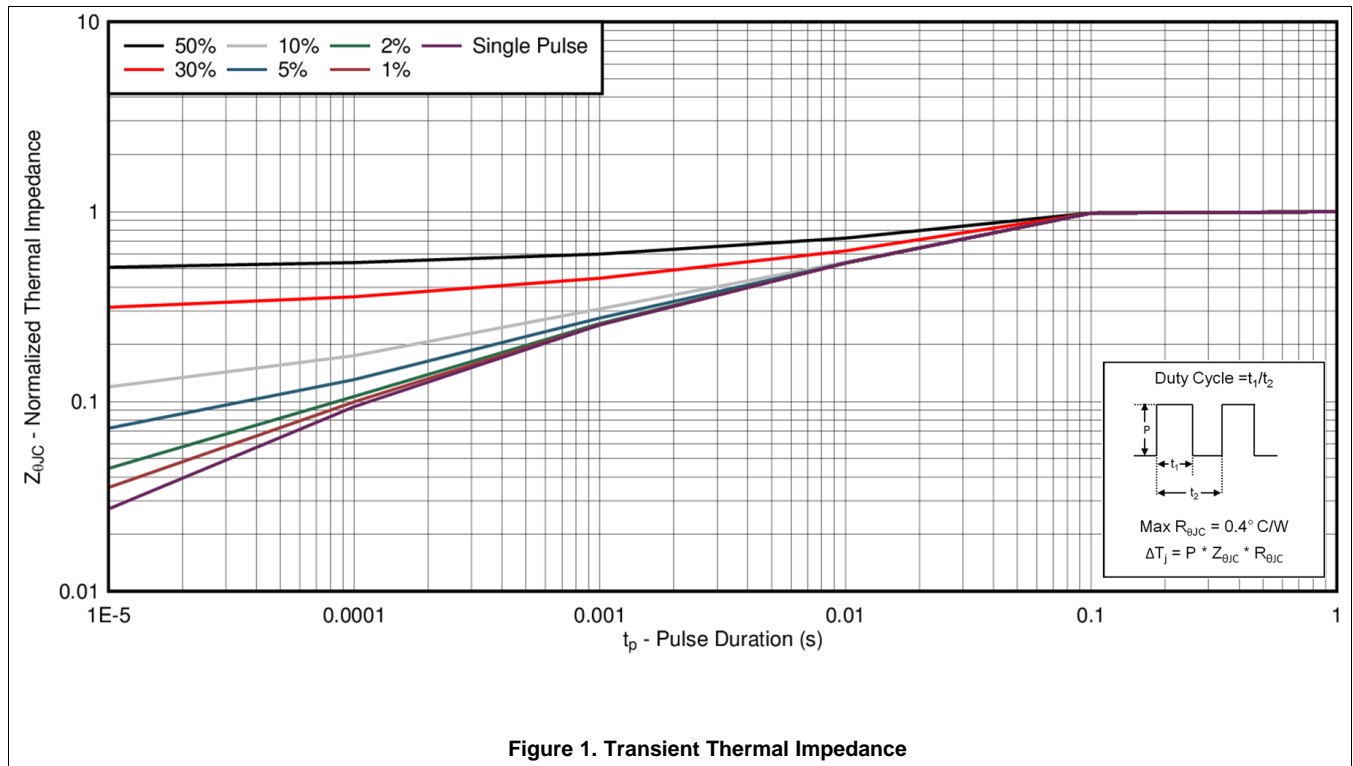
5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|-----------------|--|-----|-----|-----|---------------------------|
| $R_{\theta JC}$ | Junction-to-Case Thermal Resistance | | | 0.4 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance | | | 62 | |

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

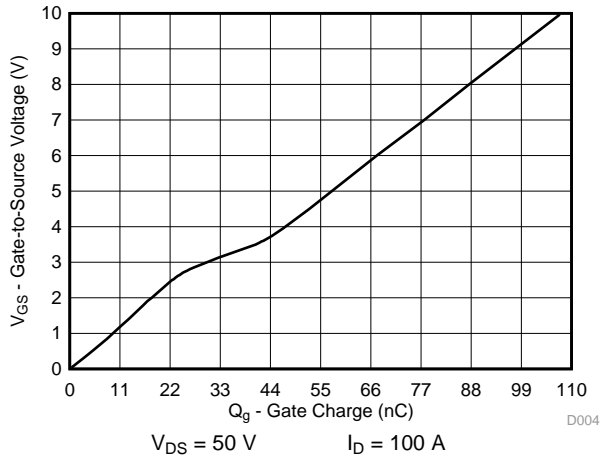


Figure 4. Gate Charge

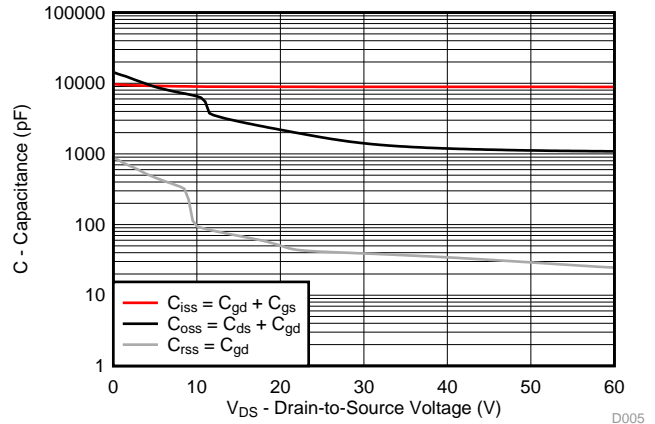


Figure 5. Capacitance

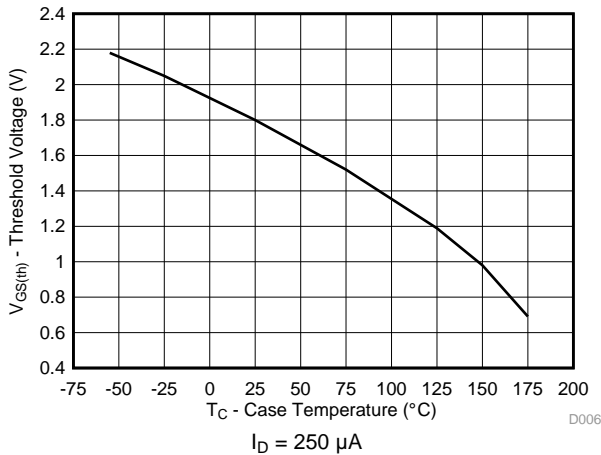


Figure 6. Threshold Voltage vs Temperature

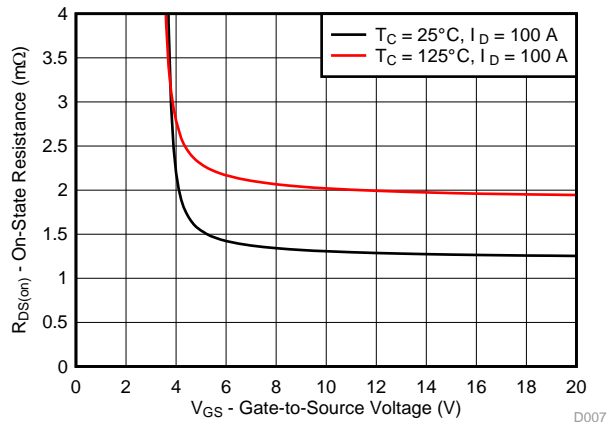


Figure 7. On-State Resistance vs Gate-to-Source Voltage

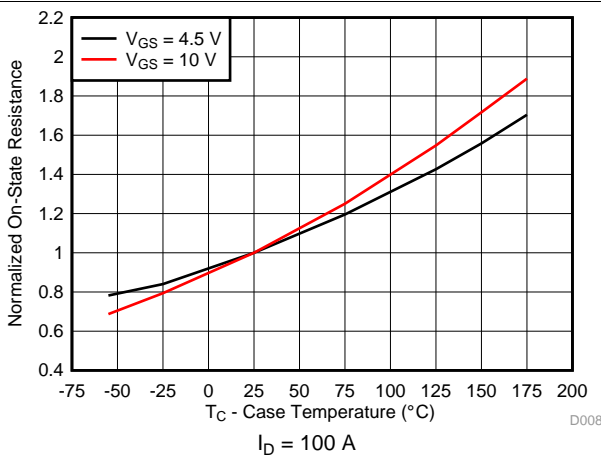


Figure 8. Normalized On-State Resistance vs Temperature

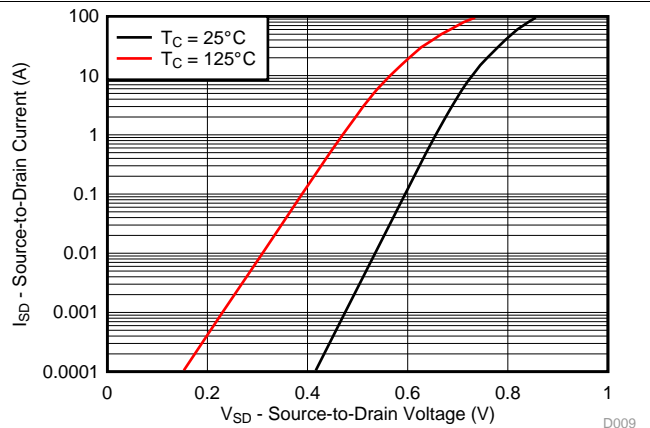


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

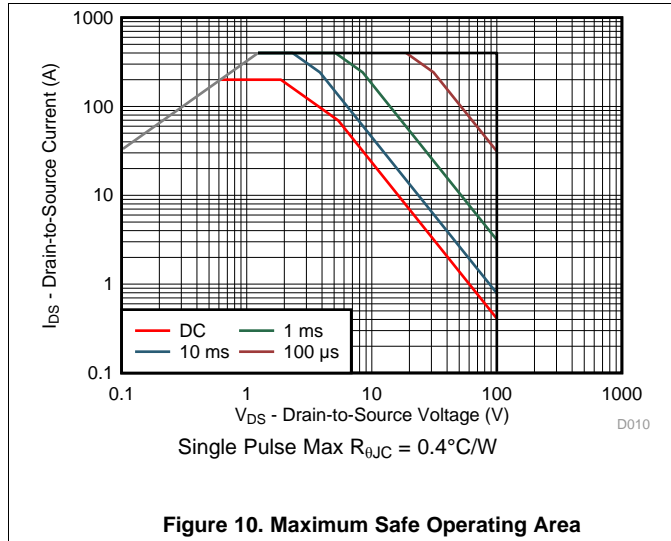


Figure 10. Maximum Safe Operating Area

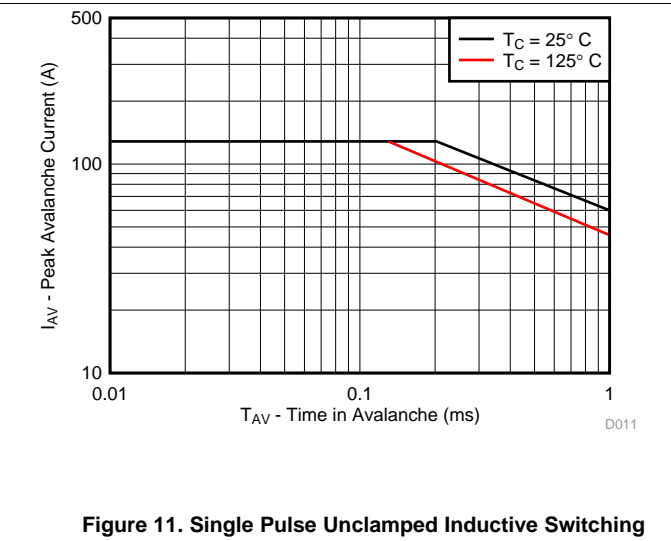


Figure 11. Single Pulse Unclamped Inductive Switching

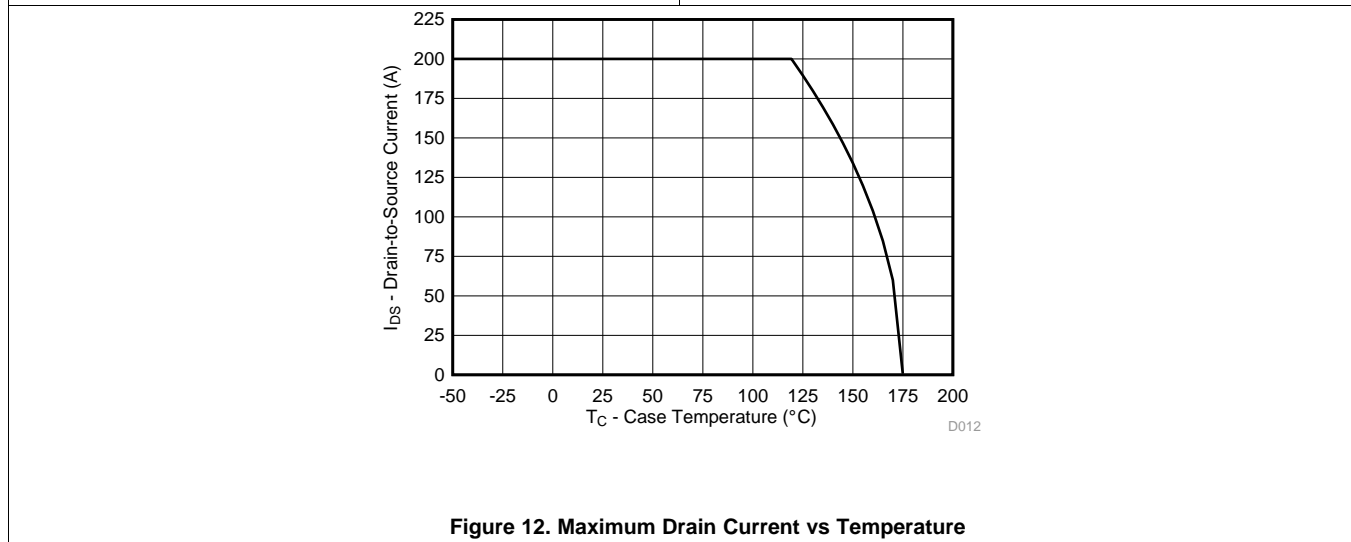


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

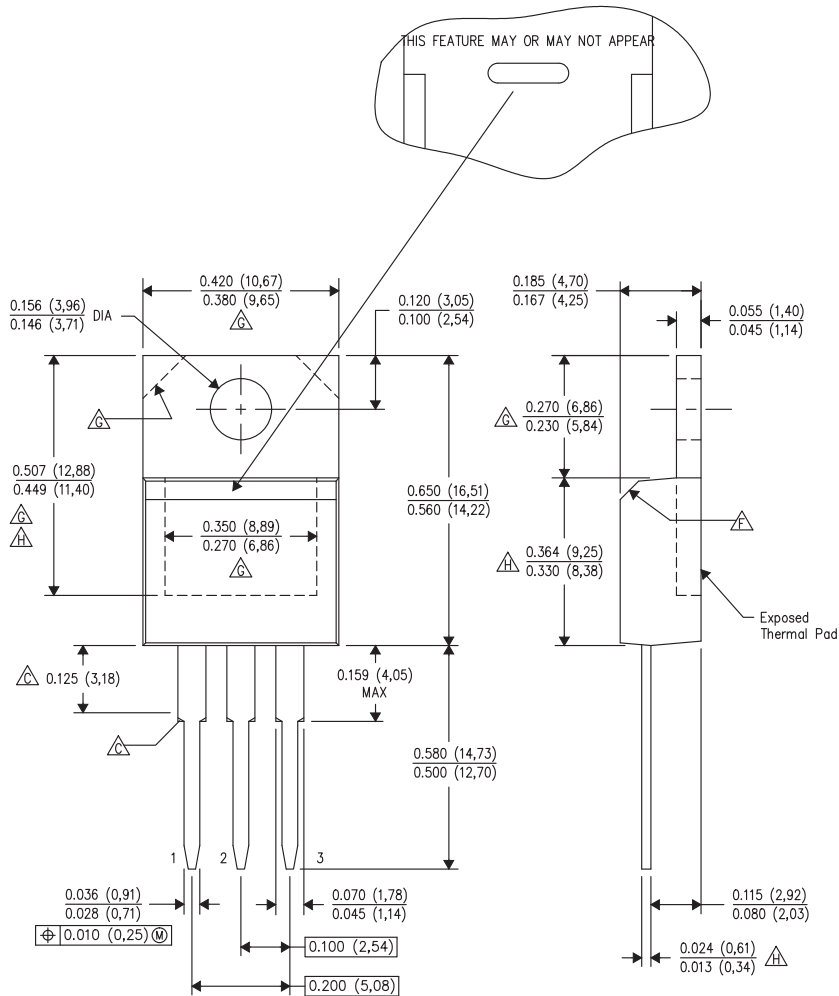
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions







- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Lead dimensions are not controlled within this area. Chamfer may or may not appear.
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 -  The chamfer is optional.
 -  Thermal pad contour optional within these dimensions.
 -  Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

Table 1. Pin Configuration

| Position | Designation |
|-------------|-------------|
| Pin 1 | Gate |
| Pin 2 / Tab | Drain |
| Pin 3 | Source |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| CSD18536KCS | ACTIVE | TO-220 | KCS | 3 | 50 | Pb-Free (RoHS Exempt) | CU SN | N / A for Pkg Type | | CSD18536KCS | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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