

# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

SLLS376D– MAY 2000 – REVISED JULY 2008

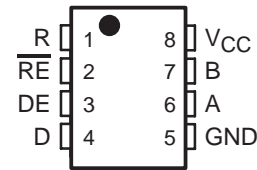
- Designed for Signaling Rates† Up to 30 Mbps
- Bus-Pin ESD Protection Exceeds 12 kV HBM
- Compatible With ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E)
- Low Skew
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Very Low Disabled Supply-Current Requirements . . . 700  $\mu$ A Maximum
- Common Mode Voltage Range of –7 V to 12 V
- Thermal-Shutdown Protection
- Driver Positive and Negative Current Limiting
- Open-Circuit Failsafe Receiver Design
- Receiver Input Sensitivity . . .  $\pm 200$  mV Max
- Receiver Input Hysteresis . . . 50 mV Typ
- Glitch-Free Power-Up and Power-Down Protection
- Available in Q-Temp Automotive High Reliability Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

## description

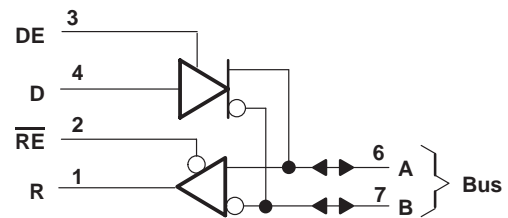
The SN65LBC176A, SN65LBC176AQ, and SN75LBC176A differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and are compatible with ANSI standard TIA/EIA-485-A and ISO 8482. The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

SN65LBC176AQD (Marked as B176AQ)  
SN65LBC176AD (Marked as BL176A)  
SN65LBC176AP (Marked as 65LBC176A)  
SN75LBC176AD (Marked as LB176A)  
SN75LBC176AP (Marked as 75LBC176A)

(TOP VIEW)



## logic diagram (positive logic)



## Function Tables

### DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

### RECEIVER

DIFFERENTIAL INPUTS $V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$-0.2$ V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit duration, and much higher signaling rates may be achieved using a different criteria (see *TYPICAL CHARACTERISTICS* section).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265  
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

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# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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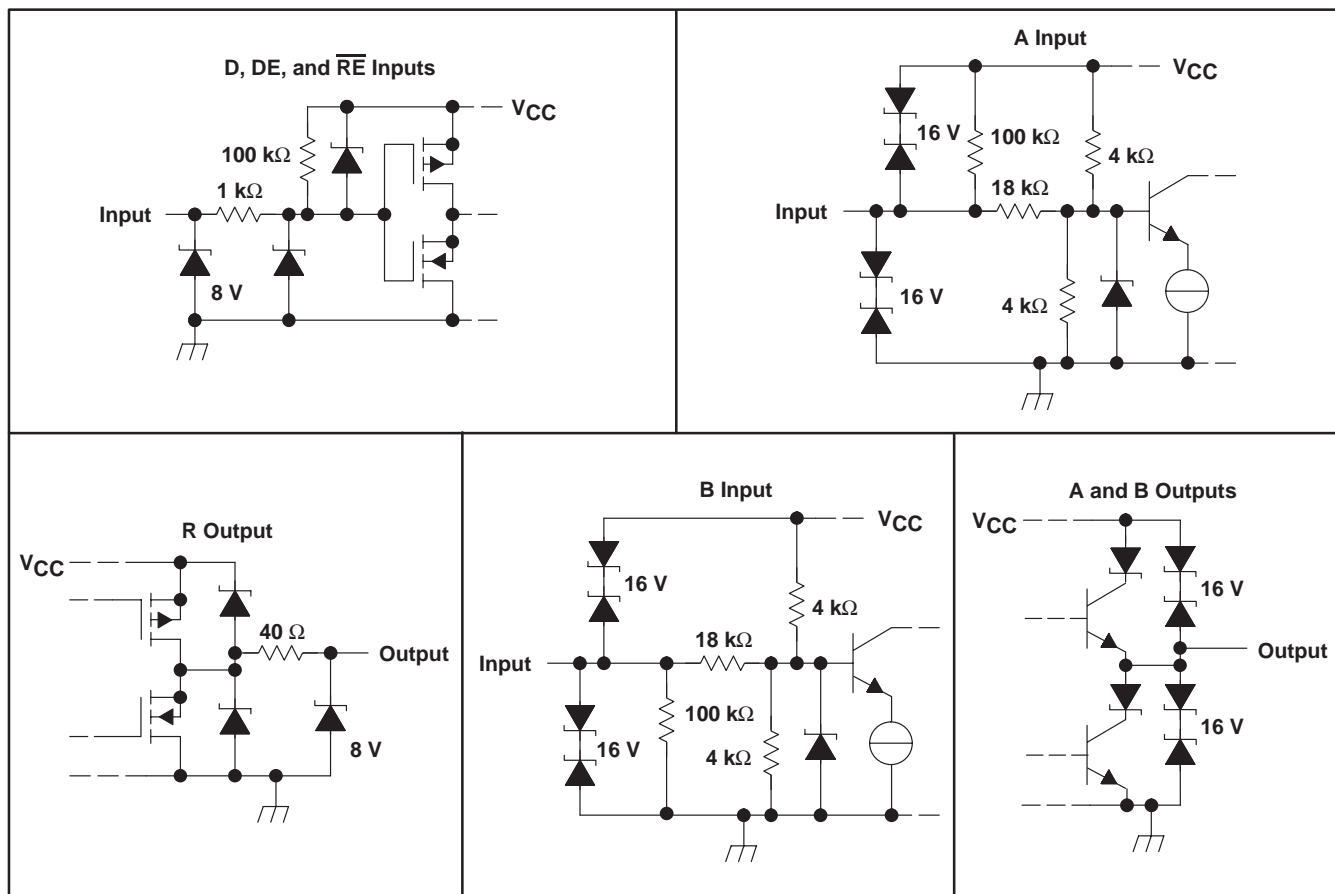
## description (continued)

The SN65LBC176A, SN65LBC176AQ, and SN75LBC176A combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC} = 0$ . This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver.

### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DUAL-IN-LINE
0°C to 70°C	SN75LBC176AD	SN75LBC176AP
–40°C to 85°C	SN65LBC176AD	SN65LBC176AP
–40°C to 125°C	SN65LBC176AQD	—

## schematics of inputs and outputs



# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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## absolute maximum ratings†

Supply voltage, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Voltage range at any bus terminal (A or B)	–10 V to 15 V
Input voltage, $V_I$ (D, DE, R, or $\overline{RE}$ )	–0.3 V to $V_{CC} + 0.5$ V
Electrostatic discharge: Bus terminals and GND, Class 3, A: (see Note 2)	12 kV
Bus terminals and GND, Class 3, B: (see Note 2)	400 V
All terminals, Class 3, A:	3 kV
All terminals, Class 3, B:	400 V
Continuous total power dissipation (see Note 3)	See Dissipation Rating Table
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
  2. Tested in accordance with MIL–STD–883C, Method 3015.7
  3. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$		–7		12	V
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2		$V_{CC}$	V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$	0		0.8	V
Differential input voltage, $V_{ID}$ (see Note 4)		–12§		12	V
High-level output current, $I_{OH}$	Driver	–60			mA
	Receiver	–8			
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			8	
Operating free-air temperature, $T_A$	SN65LBC176AQ	–40		125	°C
	SN65LBC176A	–40		85	
	SN75LBC176A	0		70	

§ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

NOTE 4: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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## driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18$ mA		-1.5	-0.8		V
$ V_{OD} $	Differential output voltage	$I_O = 0$	SN65LBC176AQ	1.5	4	6	V
			SN65LBC176A, SN75LBC176A		4		
		$R_L = 54$ $\Omega$ , See Figure 1	SN65LBC176AQ	0.9	1.5	6	V
			SN65LBC176A	1	1.5	3	
			SN75LBC176A	1.1	1.5	3	
		$V_{test} = -7$ V to 12 V, See Figure 2	SN65LBC176AQ	0.9	1.5	6	V
SN65LBC176A	1		1.5	3			
SN75LBC176A	1.1		1.5	3			
$\Delta V_{OD} $	Change in magnitude of differential output voltage	See Figures 1 and 2		-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 1	SN65LBC176AQ	1.8	2.4	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		SN65LBC176A, SN75LBC176A	1.8	2.4	2.8	
		SN65LBC176AQ	-0.2		0.2		
		SN65LBC176A, SN75LBC176A	-0.1		0.1		
$I_{OZ}$	High-impedance output current	See receiver input currents					
$I_{IH}$	High-level enable input current	$V_I = 2$ V		-100			$\mu$ A
$I_{IL}$	Low-level enable input current	$V_I = 0.8$ V		-100			$\mu$ A
$I_{OS}$	Short-circuit output current	$-7$ V $\leq V_O \leq 12$ V		-250		250	mA
$I_{CC}$	Supply current	$V_I = 0$ or $V_{CC}$ , No load	Receiver disabled and driver enabled		5	9	mA
			Receiver disabled and driver disabled		0.4	0.7	
			Receiver enabled and driver enabled		8.5	15	

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ$ C.

## driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN65LBC176AQ			SN65LBC176A SN75LBC176A			UNIT		
		MIN	TYP†	MAX	MIN	TYP†	MAX			
$t_{PLH}$	Propagation delay time, low-to-high-level output			2		12	2	6	12	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output			2		12	2	6	12	ns
$t_{sk(p)}$	Pulse skew ( $ t_{PLH} - t_{PHL} $ )					2		0.3	1	ns
$t_r$	Differential output signal rise time			1.2		11	4	7.5	11	ns
$t_f$	Differential output signal fall time			1.2		11	4	7.5	11	ns
$t_{PZH}$	Propagation delay time, high-impedance-to-high-level output					22		12	22	ns
$t_{PZL}$	Propagation delay time, high-impedance-to-low-level output					25		12	22	ns
$t_{PHZ}$	Propagation delay time, high-level-to-high-impedance output					22		12	22	ns
$t_{PLZ}$	Propagation delay time, low-level-to-high-impedance output					22		12	22	ns

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ$ C.



# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	$I_O = -8$ mA					0.2	V
$V_{IT-}$	Negative-going input threshold voltage	$I_O = 8$ mA			-0.2			V
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )						50	
$V_{IK}$	Enable-input clamp voltage	$I_I = -18$ mA			-1.5	-0.8		V
$V_{OH}$	High-level output voltage	$V_{ID} = 200$ mV,	$I_{OH} = -8$ mA,	See Figure 6	4	4.9		V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200$ mV,	$I_{OL} = 8$ mA,	See Figure 6		0.1	0.8	V
$I_{OZ}$	High-impedance-state output current	$V_O = 0$ to $V_{CC}$		SN65LBC176AQ	-10		10	$\mu$ A
				SN65LBC176A, SN75LBC176A	-1		1	
$I_I$	Bus input current	$V_{IH} = 12$ V,	$V_{CC} = 5$ V	Other input at 0 V		0.4	1	mA
		$V_{IH} = 12$ V,	$V_{CC} = 0$			0.5	1	
		$V_{IH} = -7$ V,	$V_{CC} = 5$ V		-0.8	-0.4		
		$V_{IH} = -7$ V,	$V_{CC} = 0$		-0.8	-0.3		
$I_{IH}$	High-level enable-input current	$V_{IH} = 2$ V			-100			$\mu$ A
$I_{IL}$	Low-level enable-input current	$V_{IL} = 0.8$ V			-100			$\mu$ A
$I_{CC}$	Supply current	$V_I = 0$ or $V_{CC}$ , No load	Receiver enabled and driver disabled			4	7	mA
			Receiver disabled and driver disabled			0.4	0.7	
			Receiver enabled and driver enabled			8.5	15	

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN65LBC176AQ			SN65LBC176A SN75LBC176A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{PLH}$	Propagation delay time, output $\uparrow$	7	30	30	7	13	20	ns
$t_{PHL}$	Propagation delay time, output $\downarrow$							
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )							
$t_r$	Rise time, output	5	5	5	2.1	3.3	3.3	ns
$t_f$	Fall time, output							
$t_{PZH}$	Output enable time to high level	50	50	50	30	45	45	ns
$t_{PZL}$	Output enable time to low level							
$t_{PHZ}$	Output disable time from high level							
$t_{PLZ}$	Output disable time from low level							

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .



# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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## PARAMETER MEASUREMENT INFORMATION

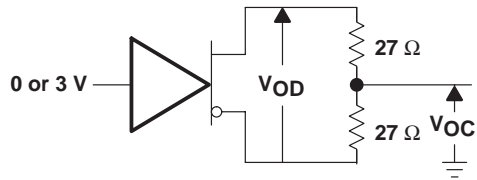
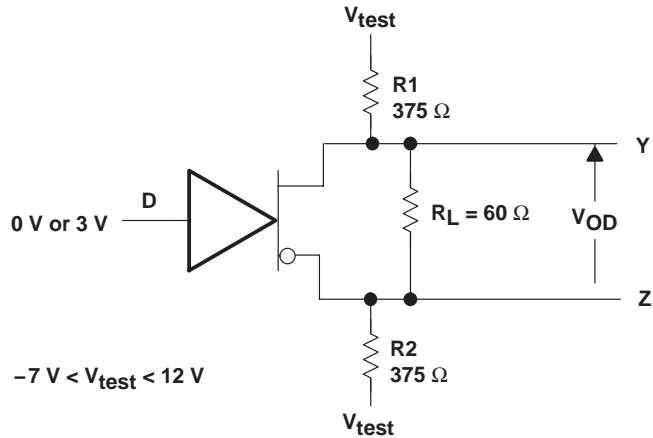
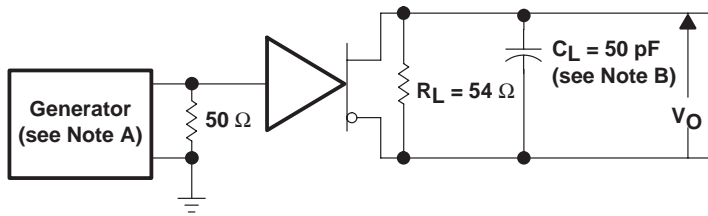


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

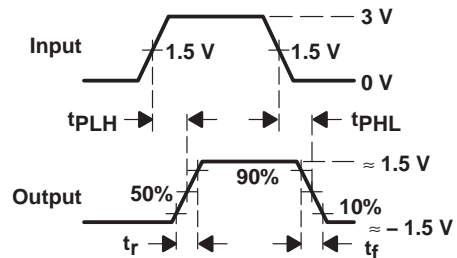


$-7\text{ V} < V_{\text{test}} < 12\text{ V}$

Figure 2. Driver  $V_{OD3}$



TEST CIRCUIT

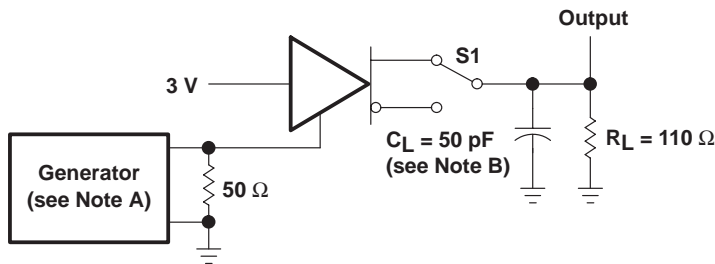


VOLTAGE WAVEFORMS

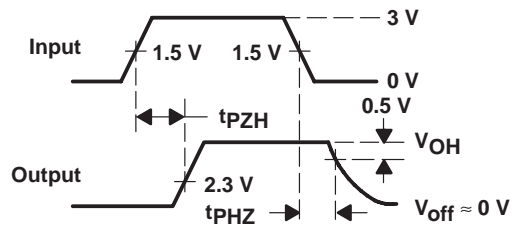
NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1\text{ MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ ,  $Z_O = 50\ \Omega$ .

B.  $C_L$  includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



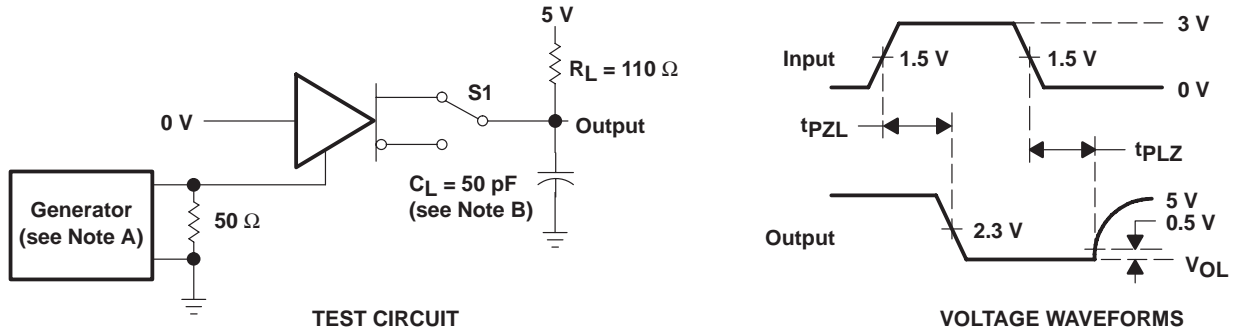
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1\text{ MHz}$ , 50% duty cycle,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ ,  $Z_O = 50\ \Omega$ .

B.  $C_L$  includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

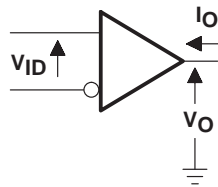
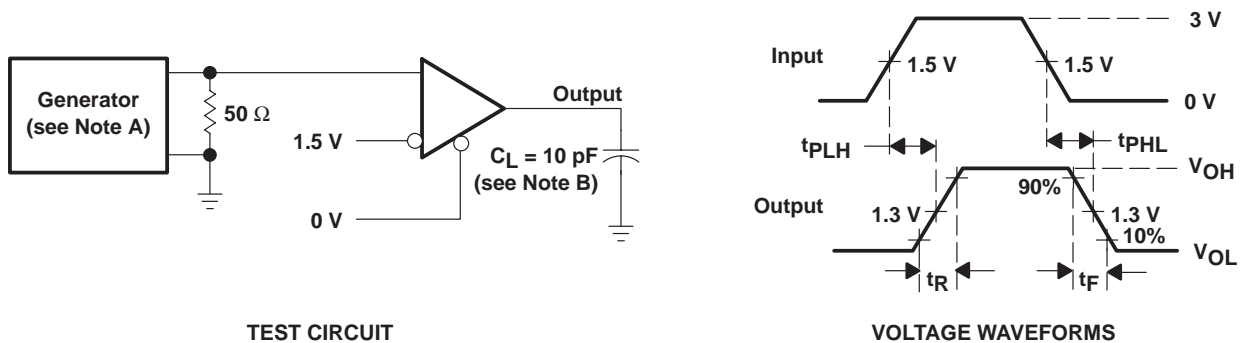


Figure 6. Receiver  $V_{OH}$  and  $V_{OL}$



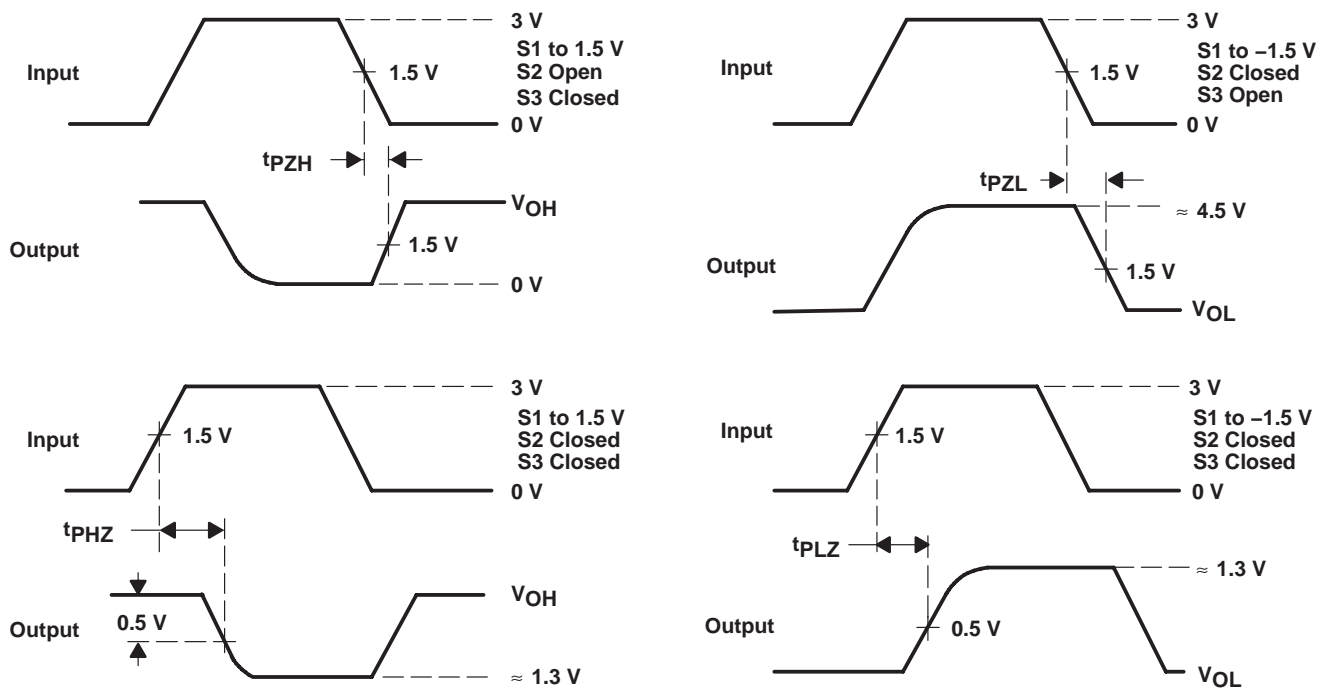
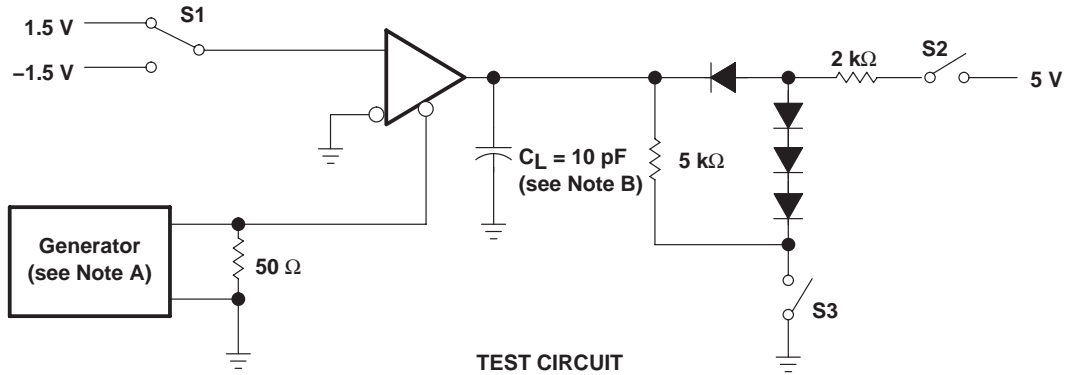
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 8. Receiver Test Circuit and Voltage Waveforms



TYPICAL CHARACTERISTICS

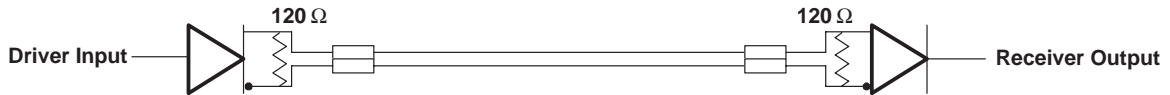
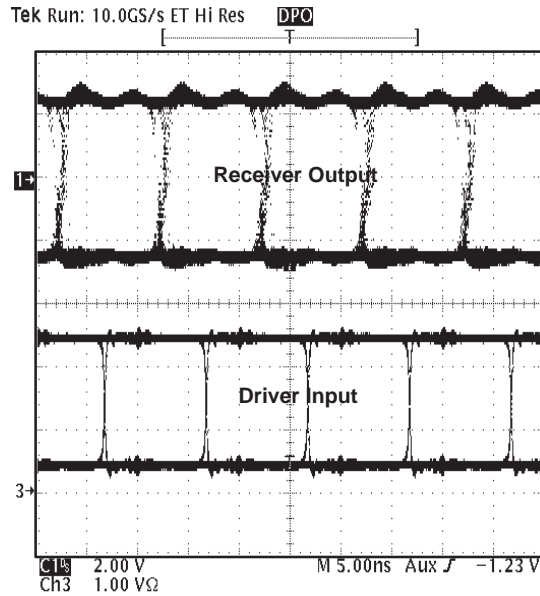


Figure 9. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard definition.

# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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## TYPICAL CHARACTERISTICS

**RMS SUPPLY CURRENT  
vs  
FREQUENCY**

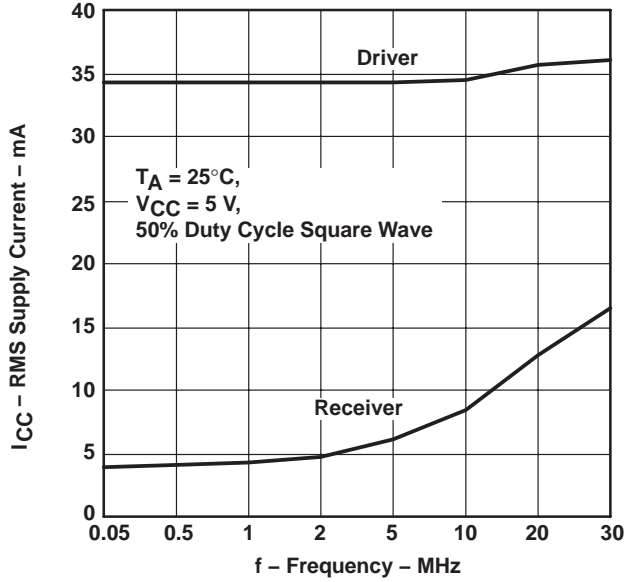


Figure 10

**LOGIC INPUT CURRENT  
vs  
INPUT VOLTAGE**

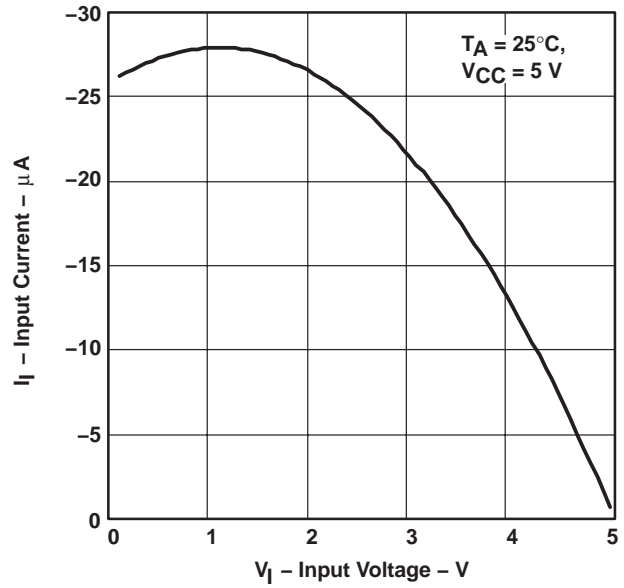


Figure 11

**INPUT CURRENT  
vs  
INPUT VOLTAGE**

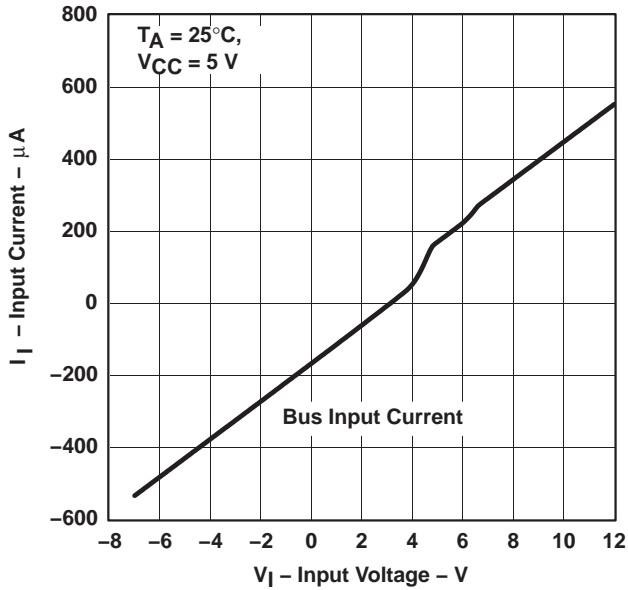


Figure 12

**LOW-LEVEL OUTPUT VOLTAGE  
vs  
LOW-LEVEL OUTPUT CURRENT**

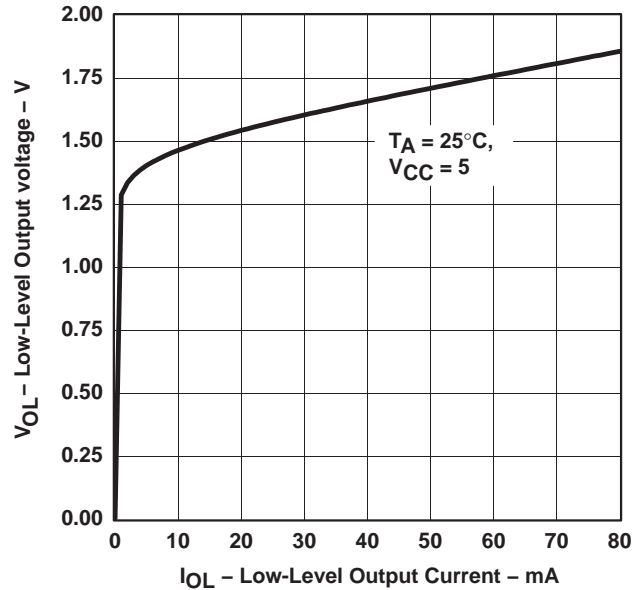


Figure 13



TYPICAL CHARACTERISTICS

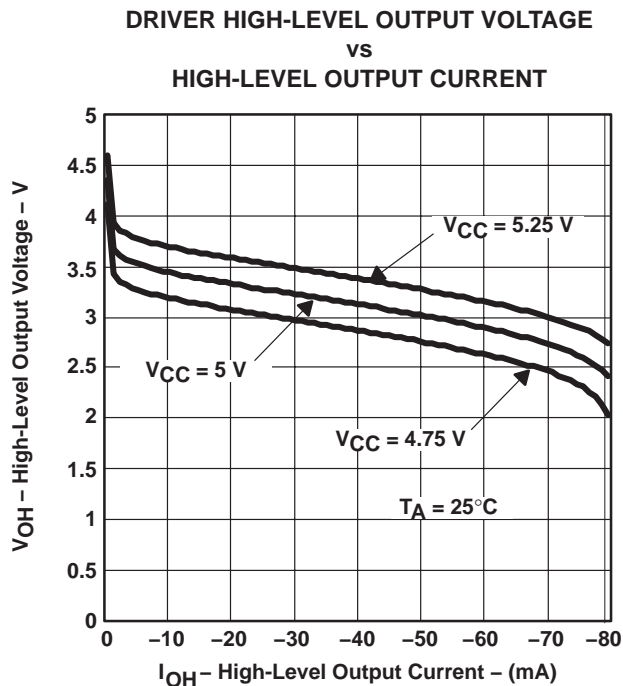


Figure 14

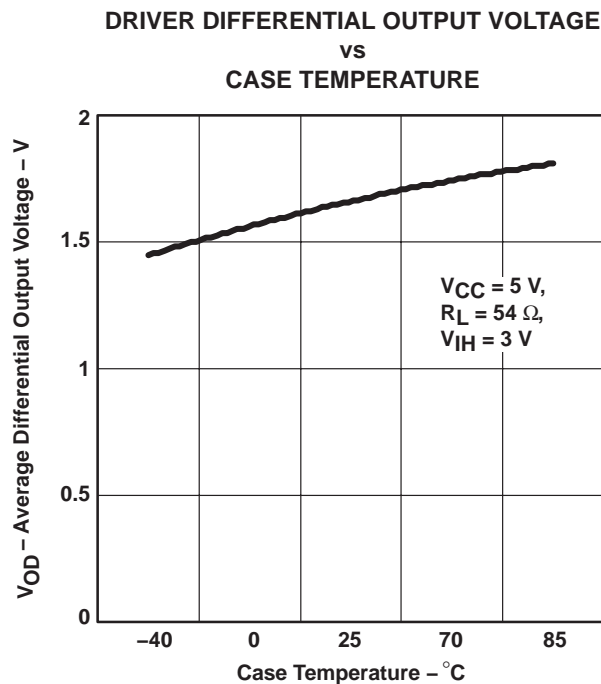


Figure 15

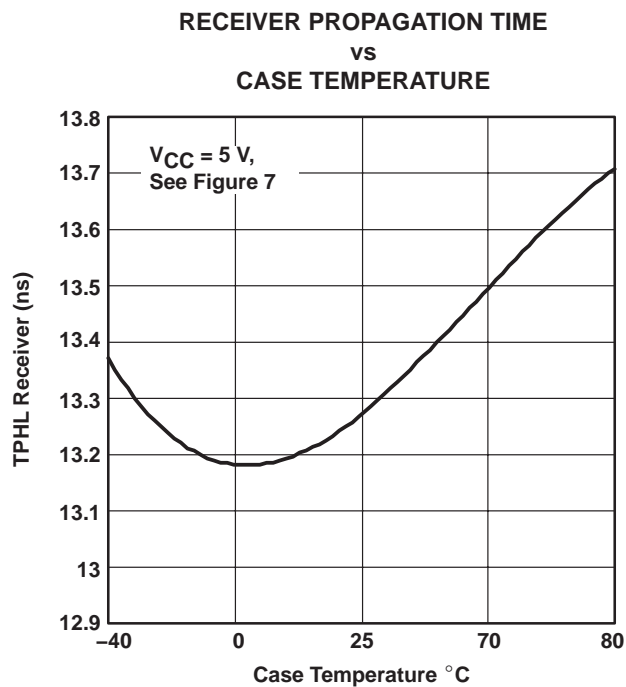


Figure 16

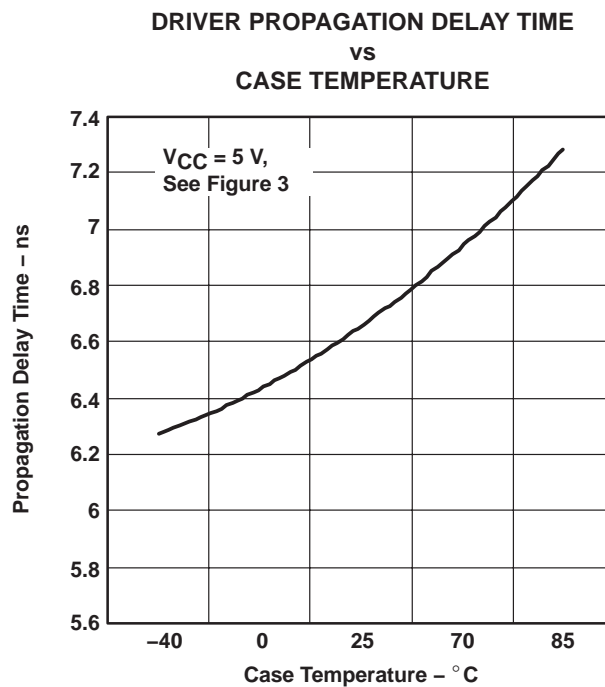


Figure 17

# SN65LBC176A, SN75LBC176A DIFFERENTIAL BUS TRANSCEIVERS

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## TYPICAL CHARACTERISTICS

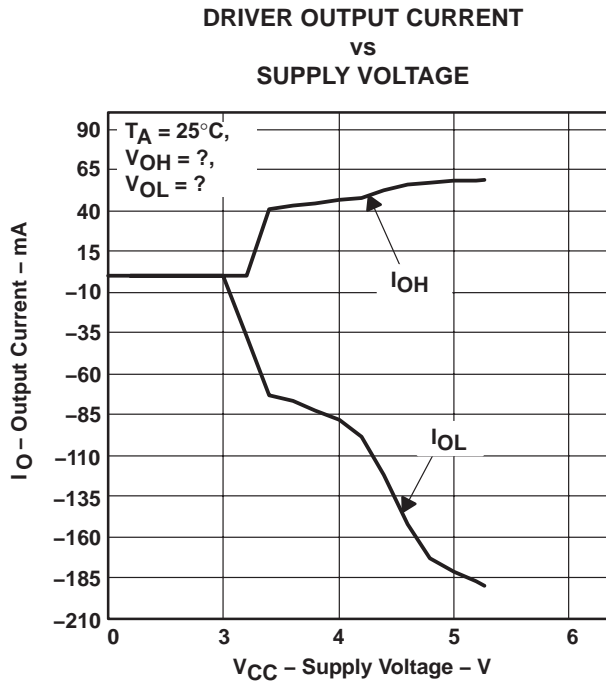


Figure 18

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LBC176AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	<a href="#">Samples</a>
SN65LBC176ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	<a href="#">Samples</a>
SN65LBC176ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	<a href="#">Samples</a>
SN65LBC176ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	<a href="#">Samples</a>
SN65LBC176AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC176A	<a href="#">Samples</a>
SN65LBC176APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC176A	<a href="#">Samples</a>
SN65LBC176AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	B176AQ	<a href="#">Samples</a>
SN65LBC176AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		B176AQ	<a href="#">Samples</a>
SN65LBC176AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	B176AQ	<a href="#">Samples</a>
SN65LBC176AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		B176AQ	<a href="#">Samples</a>
SN75LBC176AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	<a href="#">Samples</a>
SN75LBC176ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	<a href="#">Samples</a>
SN75LBC176ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	<a href="#">Samples</a>
SN75LBC176ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	<a href="#">Samples</a>
SN75LBC176AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC176A	<a href="#">Samples</a>
SN75LBC176APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC176A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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#### **OTHER QUALIFIED VERSIONS OF SN65LBC176A :**

- Enhanced Product: [SN65LBC176A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC176AQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176ADR	SOIC	D	8	2500	340.5	338.1	20.6
SN65LBC176ADR	SOIC	D	8	2500	367.0	367.0	38.0
SN65LBC176AQDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC176ADR	SOIC	D	8	2500	340.5	338.1	20.6



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE





4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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