

N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
80	0.062 at V _{GS} = 10 V	3.5	7.3 nC

FEATURES

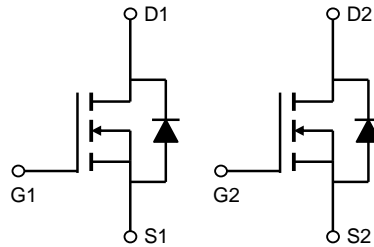
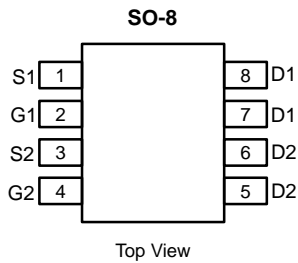
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- DC/DC Conversion
- Notebook System Power



Absolute Maximum Ratings T _A =25°C unless otherwise noted			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	80	V
Gate-Source Voltage	V _{GS}	±30	V
Continuous Drain Current	I _D	T _A =25°C	3.5
		T _A =70°C	2.9
Pulsed Drain Current ^C	I _{DM}	18	A
Avalanche Current ^C	I _{AR}	16	A
Repetitive avalanche energy L=0.1mH ^C	E _{AR}	12.8	mJ
Power Dissipation ^B	P _D	T _A =25°C	2
		T _A =70°C	1.3
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter	Symbol	Typ	Max	Units	
Maximum Junction-to-Ambient ^A	R _{θJA}	t ≤ 10s	48	62.5	°C/W
Maximum Junction-to-Ambient ^{A,D}		Steady-State	74	90	°C/W
Maximum Junction-to-Lead	R _{θJL}	32	40	°C/W	

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	80			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	3.5	4.2	5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	18			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=3.5\text{A}$ $T_J=125^\circ\text{C}$		62 113.0		m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=3.5\text{A}$		15		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.77	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
I_{SM}	Pulsed Body-diode Current ^c				18	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=40\text{V}, f=1\text{MHz}$	510	640	770	pF
C_{oss}	Output Capacitance		28	40	52	pF
C_{rss}	Reverse Transfer Capacitance		12	20	30	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=40\text{V}, I_D=3.5\text{A}$	8	11	13	nC
$Q_g(4.5\text{V})$	Total Gate Charge		4	5.5	7	
Q_{gs}	Gate Source Charge		4	5	6	nC
Q_{gd}	Gate Drain Charge		0.7	1.2	1.7	nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=40\text{V}, R_L=8\Omega,$ $R_{GEN}=3\Omega$		7.2		ns
t_r	Turn-On Rise Time			2.2		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			2		ns
t_{rr}	Body Diode Reverse Recovery Time		$I_F=3.5\text{A}, dI/dt=300\text{A}/\mu\text{s}$	14	20	26
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=3.5\text{A}, dI/dt=300\text{A}/\mu\text{s}$	35	50	65	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

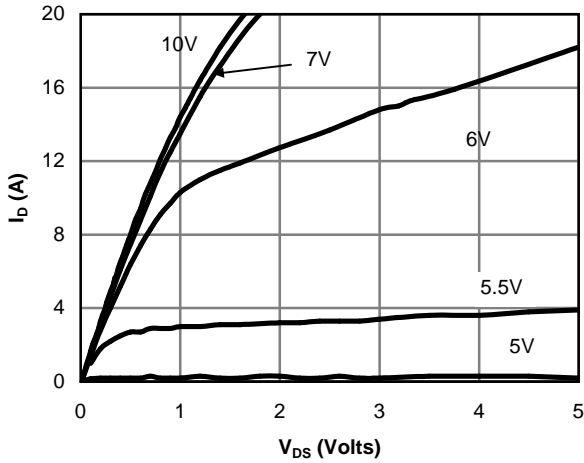


Fig 1: On-Region Characteristics (Note E)

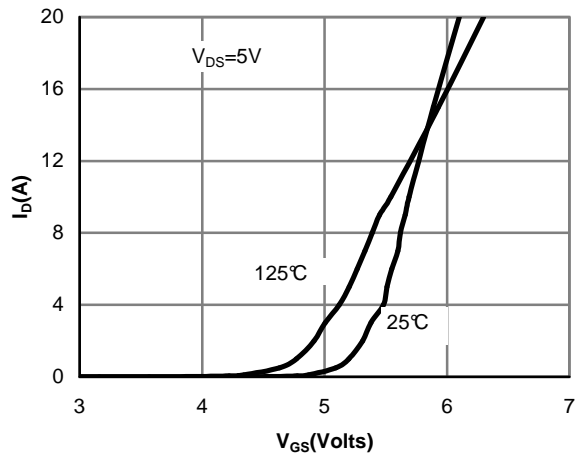


Figure 2: Transfer Characteristics (Note E)

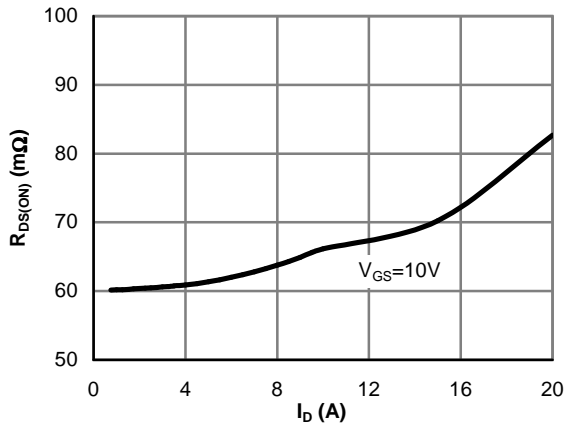


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

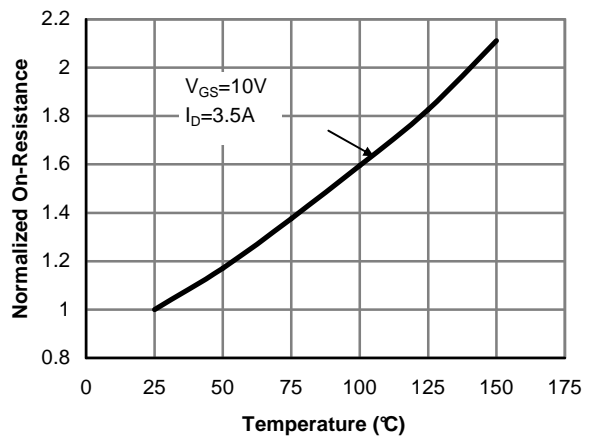


Figure 4: On-Resistance vs. Junction Temperature (Note E)

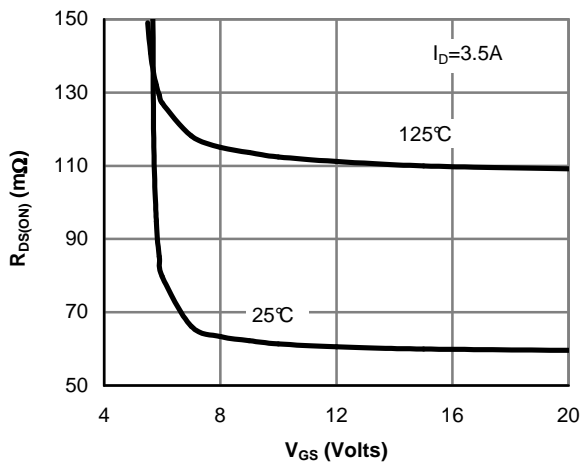


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

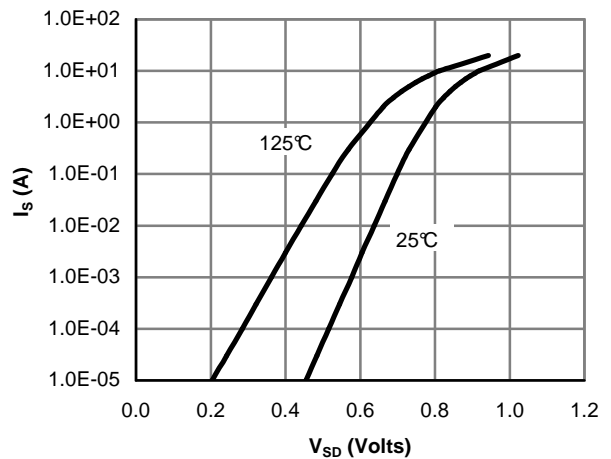


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

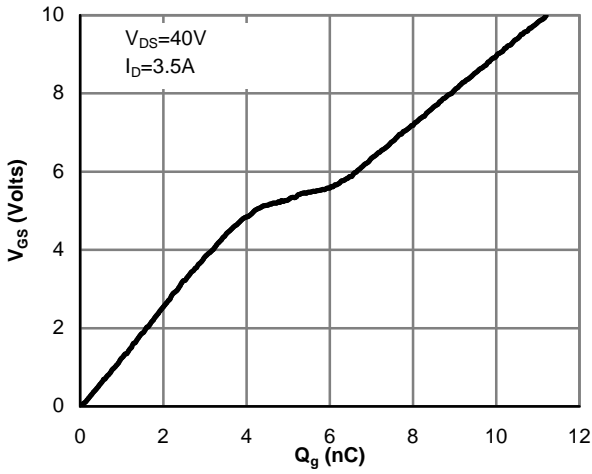


Figure 7: Gate-Charge Characteristics

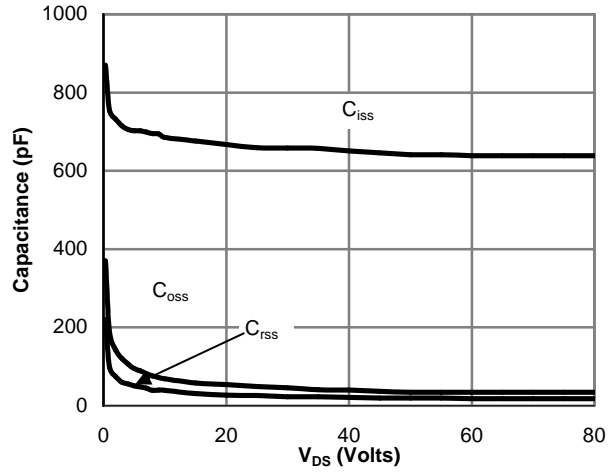


Figure 8: Capacitance Characteristics

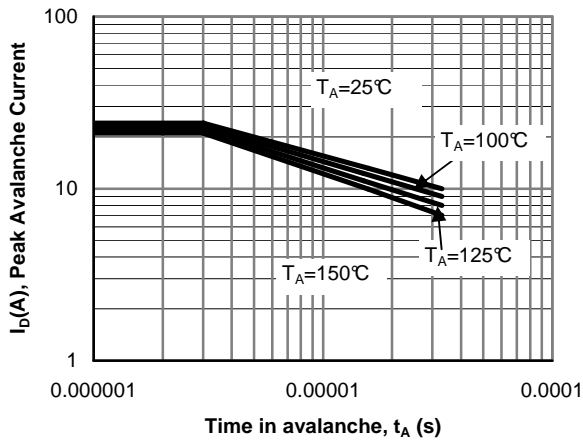


Figure 12: Single Pulse Avalanche capability

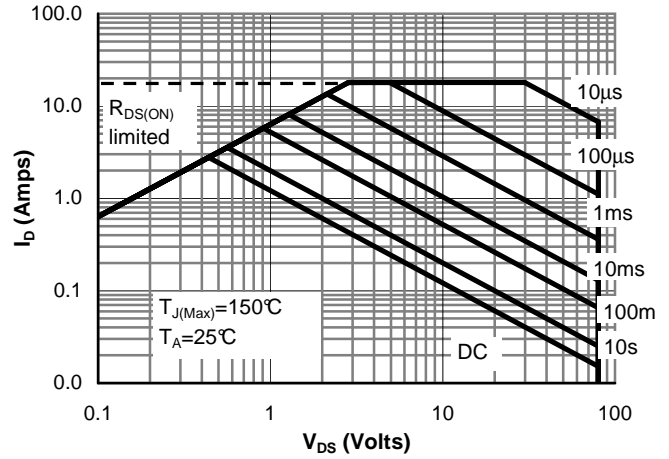


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

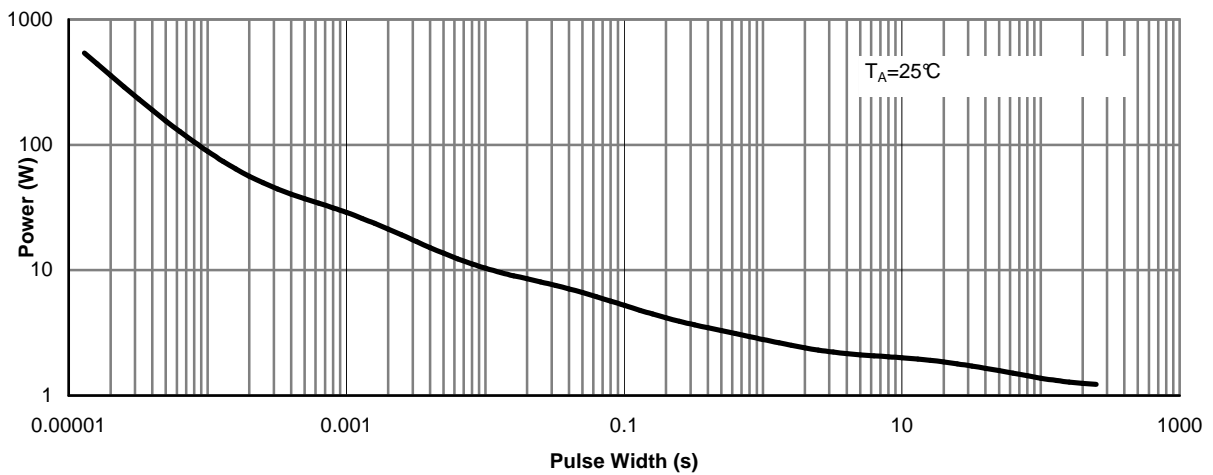


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

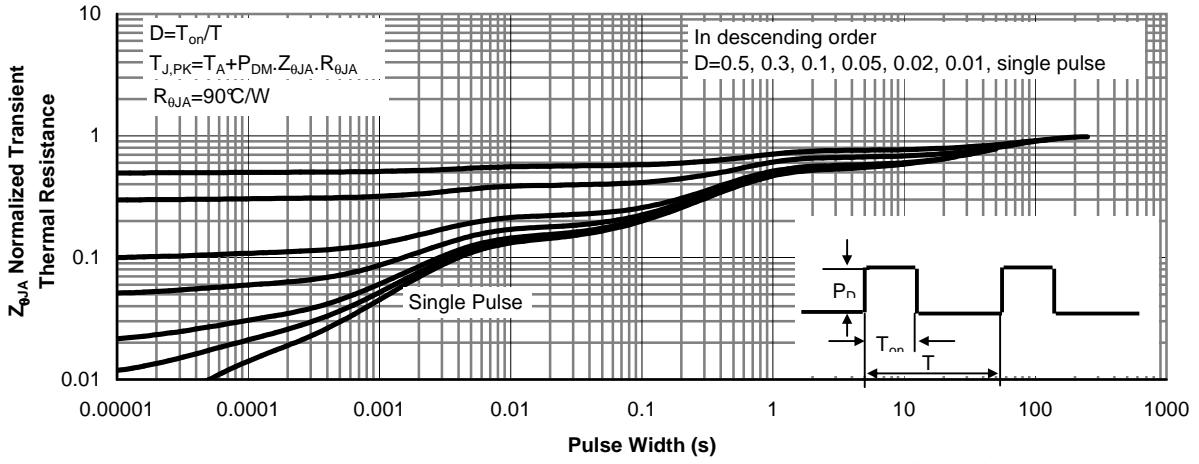
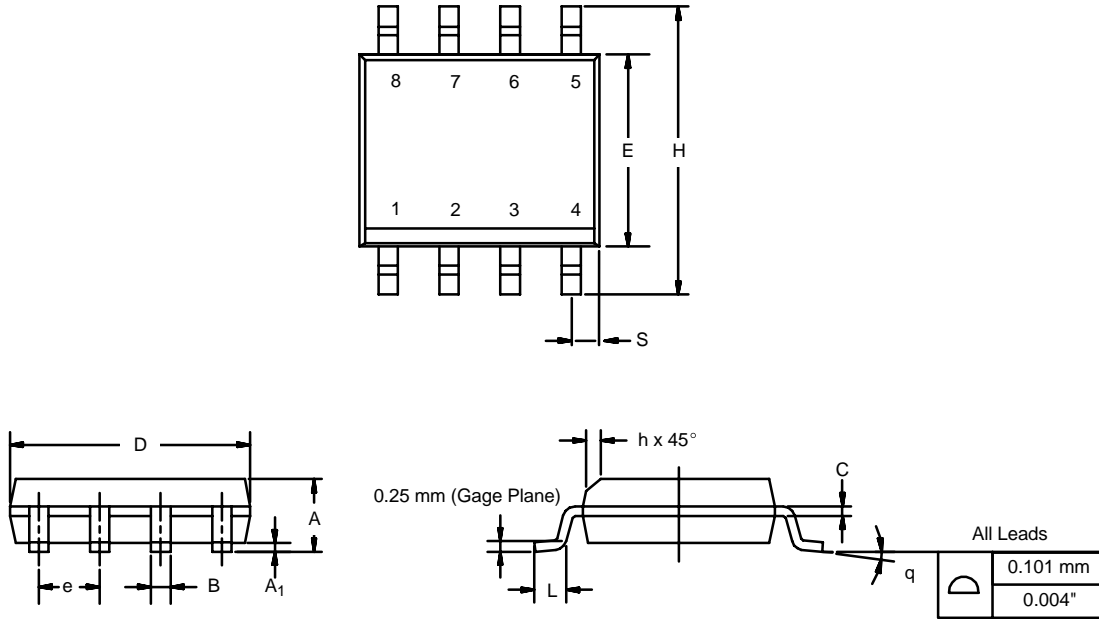


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

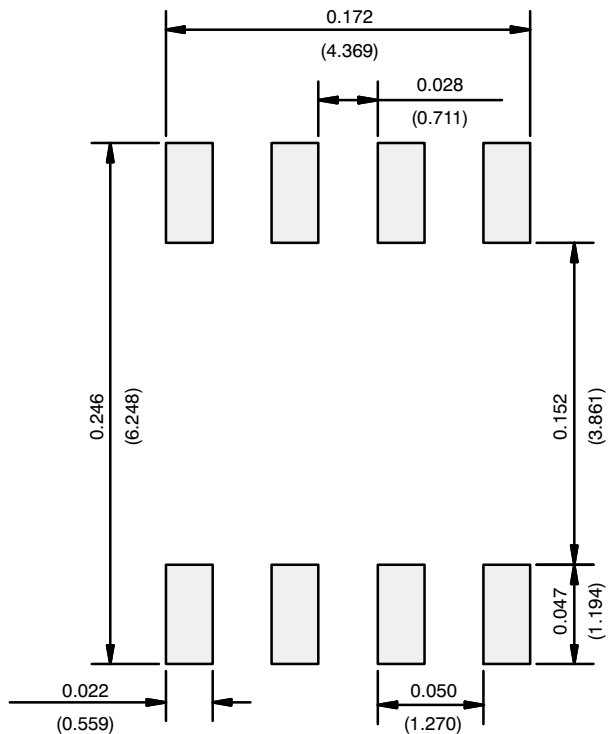
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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