74LV132

Quad 2-input NAND Schmitt trigger

Rev. 03 — 15 April 2004 Product data sheet

1. General description

The 74LV132 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC132 and 74HCT132.

The 74LV132 contains four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce V_{OLP} < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical output V_{OH} undershoot V_{OHV} > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

3. Applications

- Wave and pulse shaper
- Astable multivibrator
- Monostable multivibrator.

PHILIPS

4. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V		-	10	-	ns
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance per gate		[1] [2]	-	24	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs;
N = total number of load switching outputs.

[2] The condition is V_I = GND to V_{CC}.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV132N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV132D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV132DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV132PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

6. Functional diagram

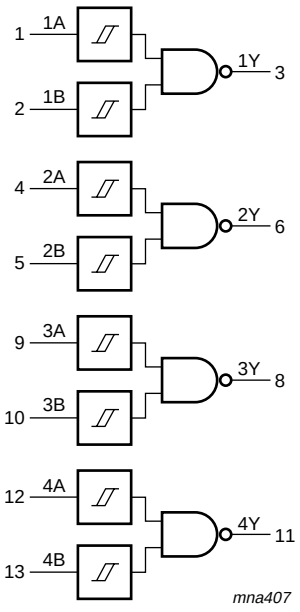


Fig 1. Logic symbol.

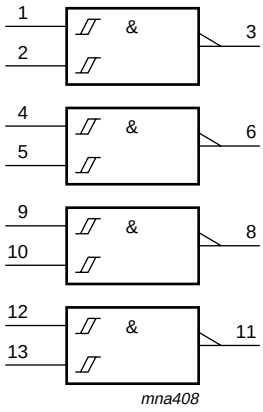


Fig 2. IEC logic symbol.

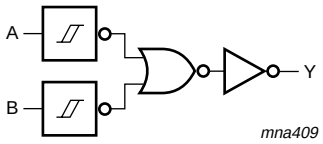


Fig 3. Logic diagram (one Schmitt trigger).

7. Pinning information

7.1 Pinning

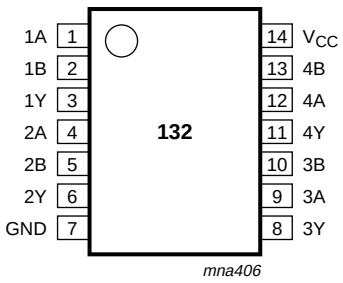


Fig 4. Pin configuration.

7.2 Pin description

Table 3: Pin description

Pin	Symbol	Description
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V_{CC}	supply voltage

8. Functional description

8.1 Function table

Table 4: Function table [1]

Input		Output
nA	**nB**	**nY**
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level.
L = LOW voltage level.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ Vor $V_O > V_{CC} + 0.5$ V	-	±50	mA
I_O	output source or sink current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{CC}, I_{GND}	V_{CC} or GND current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C				
	DIP14 package		[1]	-	750	mW
	SO14 package		[2]	-	500	mW
	SSOP14 and TSSOP14 packages		[3]	-	400	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

[3] Above 60 °C: P_{tot} derates linearly with 5.5 mW/K.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	5.5	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	operating ambient temperature	see Section 11 and 12		–40	-	+125	°C

[1] See remark in Section 11.

11. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); the 74LV132 is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}), data in this section is guaranteed from V_{CC} = 1.2 V to 5.5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 µA; V_{CC} = 1.2 V	-	1.2	-	V
		I_O = –100 µA; V_{CC} = 2.0 V	1.8	2.0	-	V
		I_O = –100 µA; V_{CC} = 2.7 V	2.5	2.7	-	V
		I_O = –100 µA; V_{CC} = 3.0 V	2.8	3.0	-	V
		I_O = –100 µA; V_{CC} = 4.5 V	4.3	4.5	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.40	2.82	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.60	4.20	-	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); the 74LV132 is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}), data in this section is guaranteed from V_{CC} = 1.2 V to 5.5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.2 V	-	0	-	V
		I_O = 100 µA; V_{CC} = 2.0 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 2.7 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 3.0 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 4.5 V	-	0	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	µA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC}$ – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				V
		I_O = –100 µA; V_{CC} = 1.2 V	-	-	-	V
		I_O = –100 µA; V_{CC} = 2.0 V	1.8	-	-	V
		I_O = –100 µA; V_{CC} = 2.7 V	2.5	-	-	V
		I_O = –100 µA; V_{CC} = 3.0 V	2.8	-	-	V
		I_O = –100 µA; V_{CC} = 4.5 V	4.3	-	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.20	-	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.50	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				V
		I_O = 100 µA; V_{CC} = 1.2 V	-	-	-	V
		I_O = 100 µA; V_{CC} = 2.0 V	-	-	0.2	V
		I_O = 100 µA; V_{CC} = 2.7 V	-	-	0.2	V
		I_O = 100 µA; V_{CC} = 3.0 V	-	-	0.2	V
		I_O = 100 µA; V_{CC} = 4.5 V	-	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	-	0.50	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	-	0.65	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	µA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC}$ – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	850	µA

[1] All typical values are measured at T_{amb} = 25 °C.

12. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay nA, nB, to nY	see Figure 5					
		V_{CC} = 1.2 V		-	65	-	ns
		V_{CC} = 2.0 V		-	18	34	ns
		V_{CC} = 2.7 V		-	15	24	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	-	12	20	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	-	9.0	14	ns
		C_L = 15 pF; V_{CC} = 3.3 V		-	10	-	ns
C_{PD}	power dissipation capacitance per gate		[4] [5]	-	24	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay nA, nB, to nY	see Figure 5					
		V_{CC} = 2.0 V		-	-	43	ns
		V_{CC} = 2.7 V		-	-	30	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	25	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	17	ns

[1] All typical values are measured at T_{amb} = 25 °C.

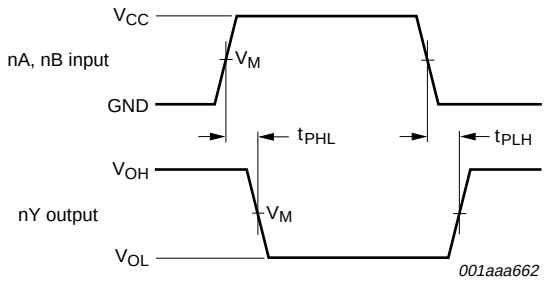
[2] Typical value measured at V_{CC} = 3.3 V.

[3] Typical value measured at V_{CC} = 5.0 V.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs;
N = total number of load switching outputs.

[5] The condition is V_I = GND to V_{CC}.

13. Waveforms



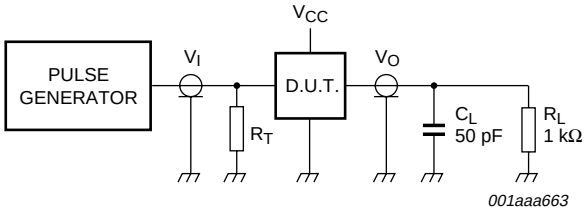
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig 5. Input (nA, nB) to output (nY) propagation delays.

Table 9: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

Fig 6. Load circuitry for switching times.

Table 10: Test data

Supply voltage	Input	
V_{CC}	V_I	t_r, t_f
< 2.7 V	V_{CC}	2.5 ns
2.7 V to 3.6 V	2.7 V	2.5 ns
≥ 4.5 V	V_{CC}	2.5 ns

14. Transfer characteristics

Table 11: Transfer characteristics

See Figure 7 and 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{T+}	positive going threshold	V_{CC} = 1.2 V	-	0.70	-	V
		V_{CC} = 2.0 V	0.8	1.10	1.4	V
		V_{CC} = 2.7 V	1.0	1.45	2.0	V
		V_{CC} = 3.0 V	1.2	1.60	2.2	V
		V_{CC} = 3.6 V	1.5	1.95	2.4	V
		V_{CC} = 4.5 V	1.7	2.50	3.2	V
		V_{CC} = 5.5 V	2.1	3.00	3.9	V
V_{T-}	negative going threshold	V_{CC} = 1.2 V	-	0.34	-	V
		V_{CC} = 2.0 V	0.3	0.65	0.9	V
		V_{CC} = 2.7 V	0.4	0.90	1.4	V
		V_{CC} = 3.0 V	0.6	1.05	1.5	V
		V_{CC} = 3.6 V	0.8	1.30	1.8	V
		V_{CC} = 4.5 V	0.9	1.60	2.0	V
		V_{CC} = 5.5 V	1.2	2.00	2.6	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 1.2 V	-	0.30	-	V
		V_{CC} = 2.0 V	0.2	0.55	0.8	V
		V_{CC} = 2.7 V	0.3	0.60	1.1	V
		V_{CC} = 3.0 V	0.4	0.65	1.2	V
		V_{CC} = 3.6 V	0.4	0.70	1.2	V
		V_{CC} = 4.5 V	0.4	0.80	1.4	V
		V_{CC} = 5.5 V	0.6	1.00	1.5	V
T_{amb} = −40 °C to +125 °C						
V_{T+}	positive going threshold	V_{CC} = 2.0 V	0.8	-	1.4	V
		V_{CC} = 2.7 V	1.0	-	2.0	V
		V_{CC} = 3.0 V	1.2	-	2.2	V
		V_{CC} = 3.6 V	1.5	-	2.4	V
		V_{CC} = 4.5 V	1.7	-	3.2	V
		V_{CC} = 5.5 V	2.1	-	3.9	V

Table 11: Transfer characteristics

See Figure 7 and 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T-}	negative going threshold	V_{CC} = 1.2 V	-	-	-	V
		V_{CC} = 2.0 V	0.3	-	0.9	V
		V_{CC} = 2.7 V	0.4	-	1.4	V
		V_{CC} = 3.0 V	0.6	-	1.5	V
		V_{CC} = 3.6 V	0.8	-	1.8	V
		V_{CC} = 4.5 V	0.9	-	2.0	V
		V_{CC} = 5.5 V	1.2	-	2.6	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 1.2 V	-	-	-	V
		V_{CC} = 2.0 V	0.2	-	0.8	V
		V_{CC} = 2.7 V	0.3	-	1.1	V
		V_{CC} = 3.0 V	0.4	-	1.2	V
		V_{CC} = 3.6 V	0.4	-	1.2	V
		V_{CC} = 4.5 V	0.4	-	1.4	V
		V_{CC} = 5.5 V	0.6	-	1.5	V

[1] All typical values are measured at T_{amb} = 25 °C.

15. Waveforms transfer characteristics

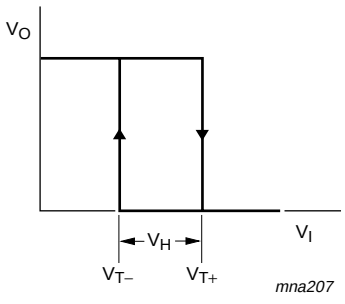
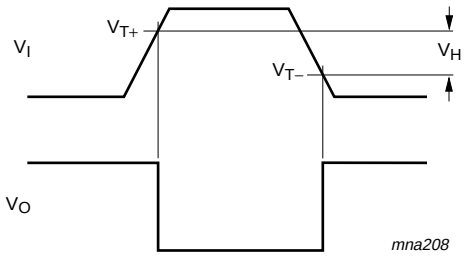
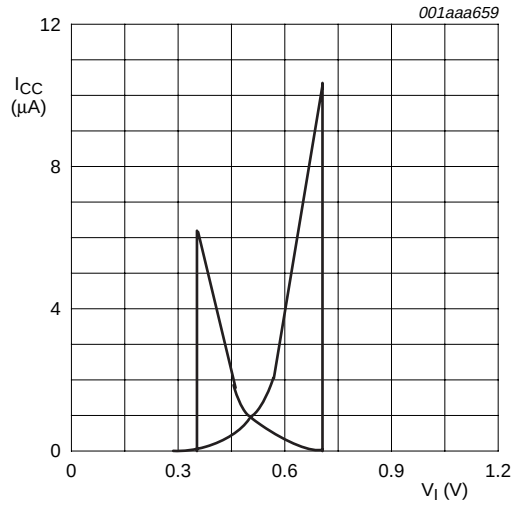


Fig 7. Transfer characteristic.



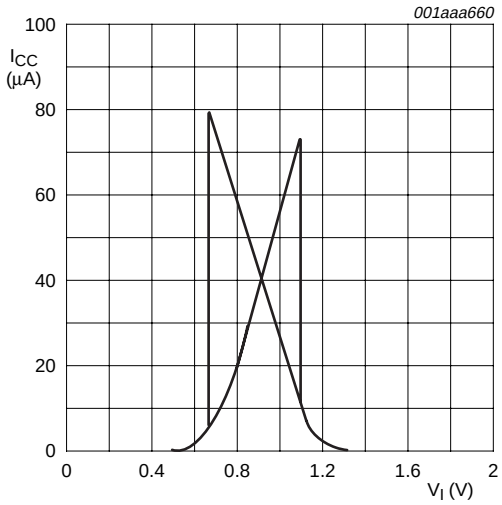
V_{T+} and V_{T-} limits are at 70 % and 20 %.

Fig 8. Definition of V_{T+}, V_{T-} and V_H.



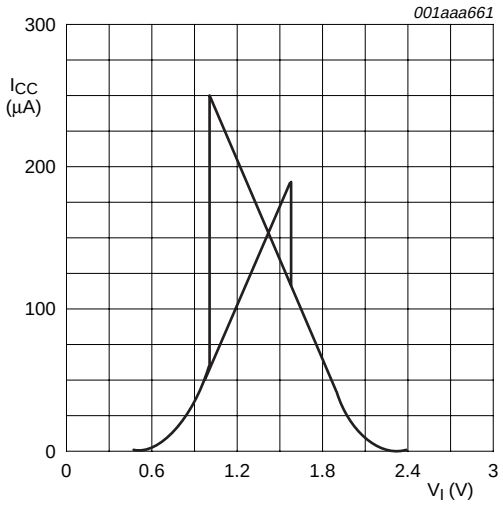
V_{CC} = 1.2 V.

Fig 9. Typical 74LV132 transfer characteristics.



V_{CC} = 2.0 V.

Fig 10. Typical 74LV132 transfer characteristics.

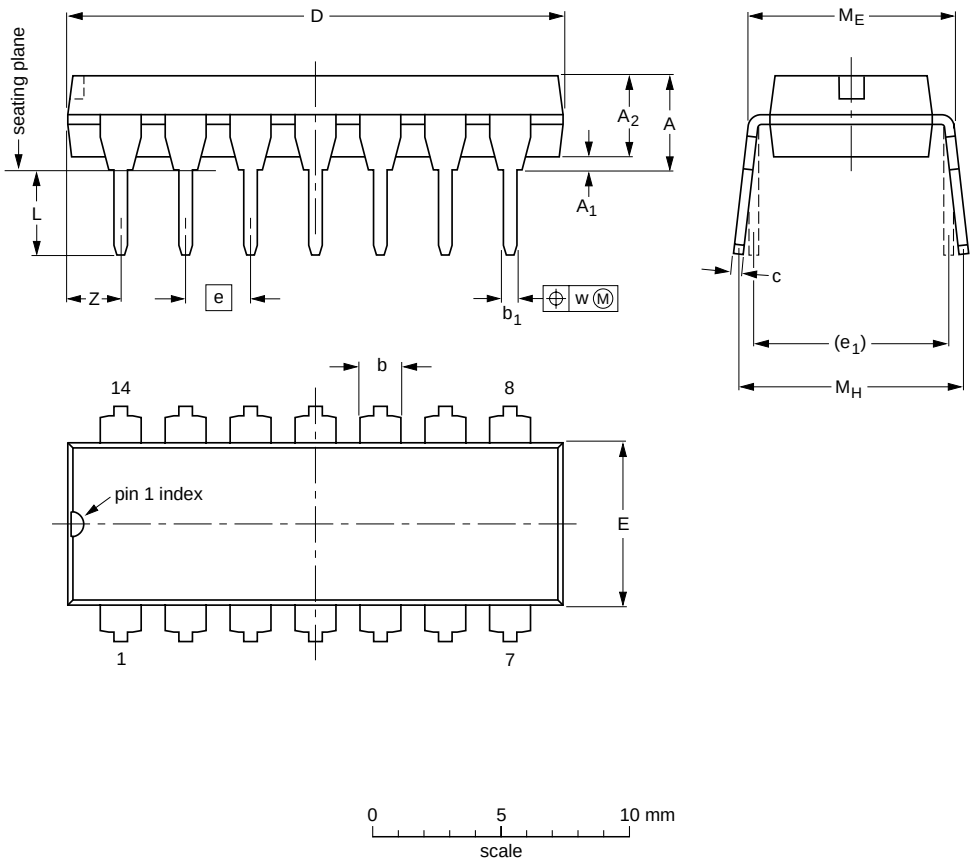


V_{CC} = 3.0 V.

Fig 11. Typical 74LV132 transfer characteristics.

16. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

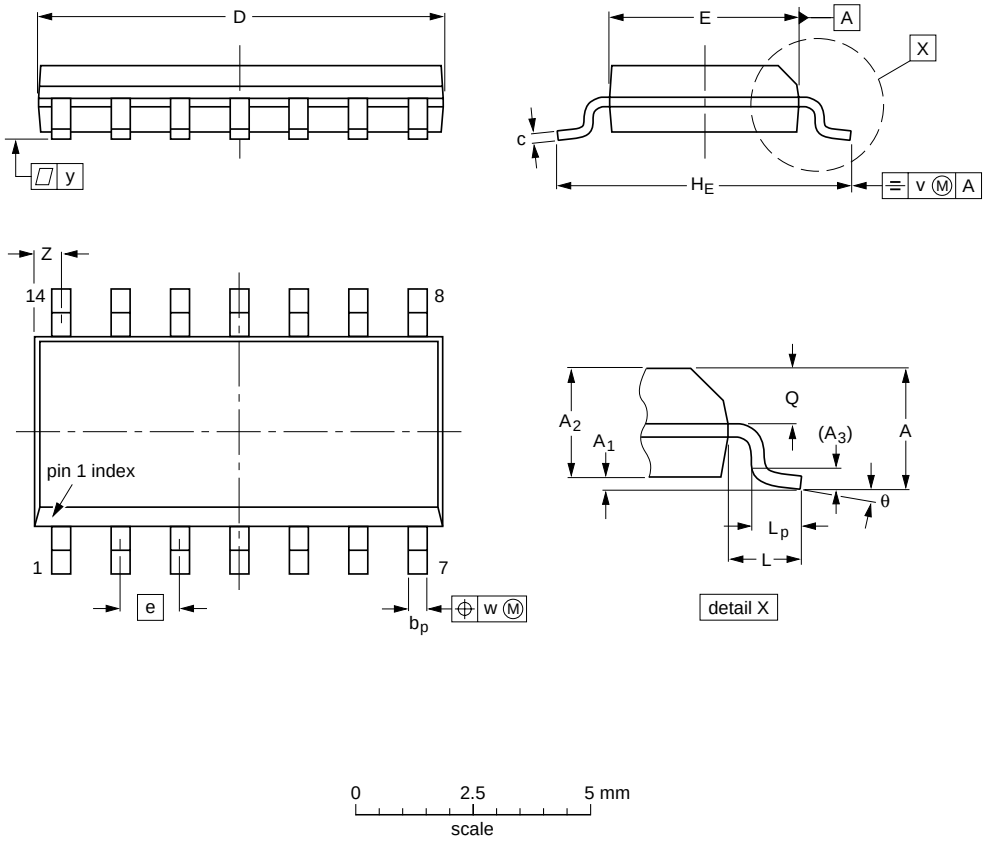
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 12. Package outline DIP14.

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

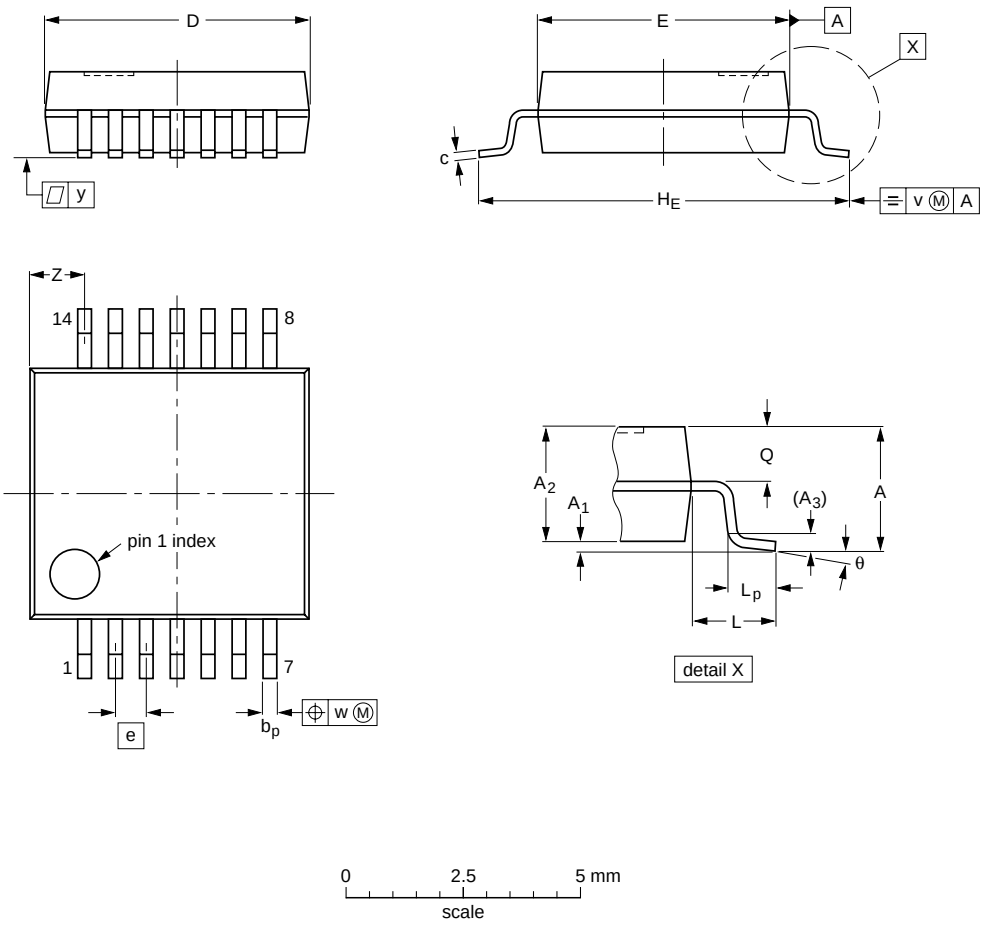
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SO14.

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

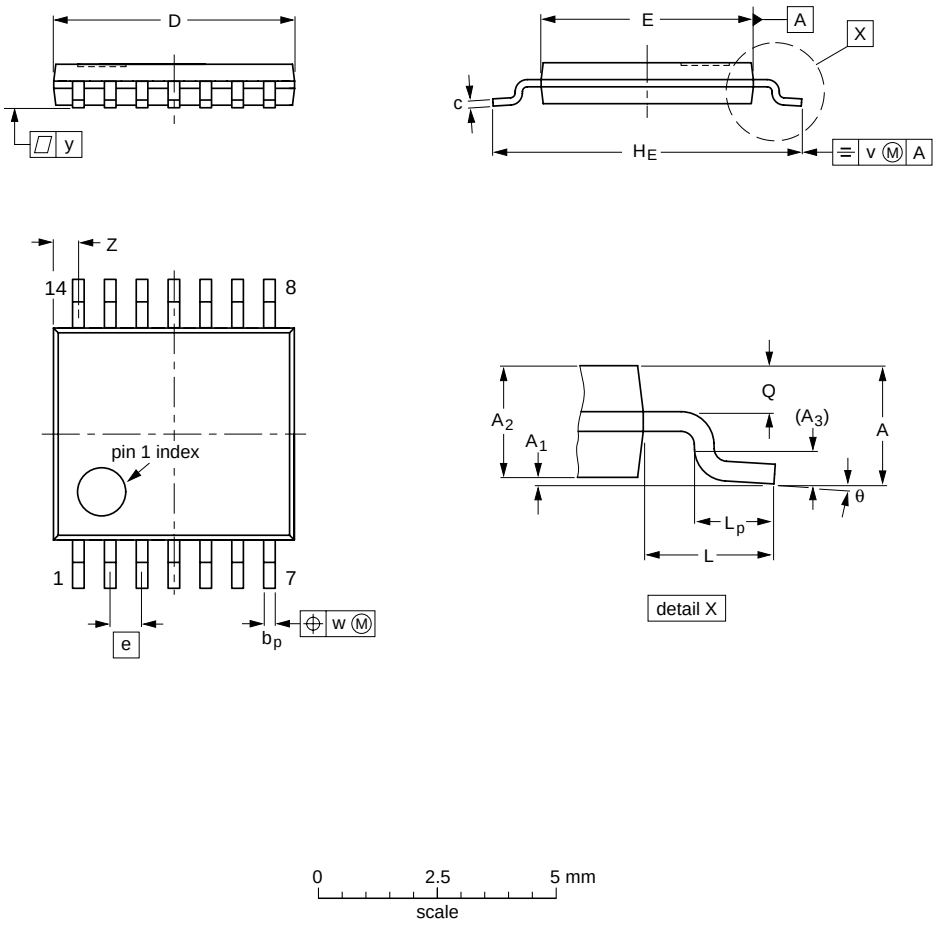
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 14. Package outline SSOP14.

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 15. Package outline TSSOP14.

17. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LV132_3	20040415	Product data	-	9397 750 13031	74LV132_2
Modifications:	• The format of this data sheet has been redesigned to comply with the presentation and information standard of Philips Semiconductors • Table 7 on page 5: deleted incorrect V_{IH} and V_{IL} specification.				
74LV132_2	19980801	Product data	-	9397 750 04422	74LV132_1

18. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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21. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

22. Contents

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