

## Product Profile

SN74LVC1G14 is a Schmitt trigger function of the NOT gate integrated circuit, can realize mathematical logic operation.  $Y = \bar{A}$  The chip is designed on an advanced CMOS process, featuring low power consumption and high output drive capability. The chip works well with a VCC supply voltage between 1.65 V and 5.5 V. The 74LVC1G14 is available in a variety of small package forms, which can be widely used in high-end precision instruments, miniaturized low-power handheld devices, and artificial intelligence.

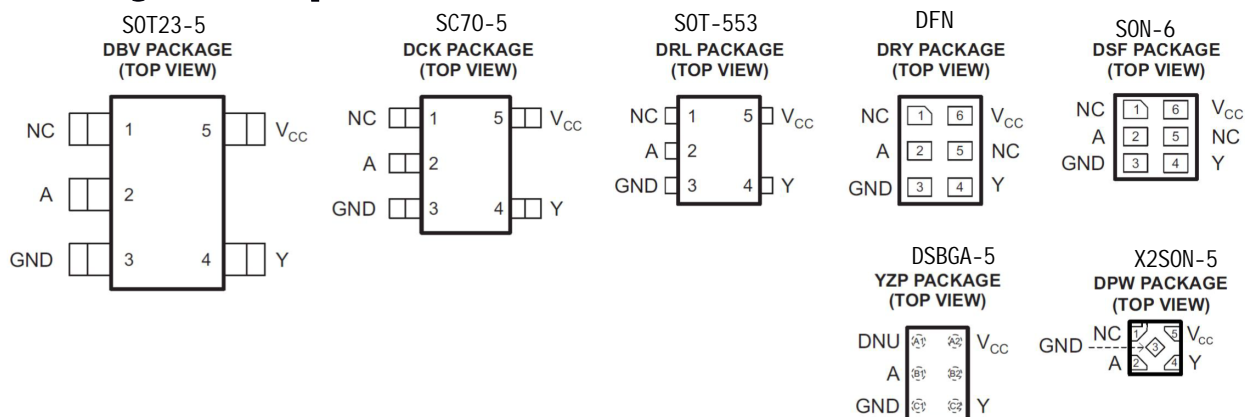
## Product Features

- Low input current: 0.1 uA typical
- Wide operating range: 1.65 V to 5.5 V
- Low quiescent power consumption: 0.1 uA typical
- Package: DBV/ DCK/ DRL/ YZP/ DRY/ DSF/ DPW
- High output drive VCC = 4.5 V, greater than 32 MA

## Product Usage

- Portable audio interface Blu-ray player and home theater
- Digital TV
- Solid state hard disk
- Intelligent wearable devices, such as wireless headphones, smart watches, etc.

## Package form and pin function definition



Name	Pin				Description
	DBV/ DCK/ DRL	DRY/DSF	YZP	DPW	
NC	1	1,5	A1, B2	1	Empty foot
A	2	2	B1	2	Input
GND	3	3	C1	3	Power supply ground
Y	4	4	C2	4	Output
VCC	5	6	A2	5	Power supply positive

Note: NC null pin, no connecting wire inside.

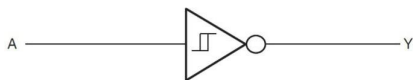
■ limiting parameter

Parameter	SYMBOLS	Limit value	Unit
Operating voltage	V <sub>CC</sub>	6.5	V
Input	V <sub>IN</sub>	-0.5 to 6.5	V
Output Voltage (1)	V <sub>OUT</sub>	-0.5 to 6.5	V
Single pin output current	I <sub>OUT</sub>	25	mA
V <sub>CC</sub> or GND Current	I <sub>CC</sub>	50	mA
Storage temperature	T <sub>S</sub>	-65-150	°C
Lead Soldering Temperature	T <sub>w</sub>	260,10s	°C

Note:1. Under VCC = 0V power-off state, the output can withstand the limit voltage.

2. The limit parameter refers to the limit value which cannot be exceeded under any condition. If this limit value is exceeded, physical damage such as product degradation may be caused; at the same time, near the limit parameters, it is impossible to guarantee that the chip can work normally.

■ Principle Logic Diagram



■ Truth Table

Inputs	Output
A	Y
L	H
H	L

## ■ Operating conditions

PROJECTS	SYMBOLS	Test Conditions	Min.	TYP	Max.	Unit
Operating voltage	$V_{CC}$	-	1.65	-	5.5	V
Input High Voltage	$V_{IH}$	$V_{CC} = 1.65V \sim 1.95V$	$0.65 * V_{CC}$	-	-	V
		$V_{CC} = 2.3V \sim 2.7V$	1.7V	-	-	
		$V_{CC} = 3V \sim 5.5V$	$0.7 * V_{CC}$	-	-	
Low-Level Input Voltage	$V_{IL}$	$V_{CC} = 1.65V \sim 1.95V$	-	-	$0.35 * V_{CC}$	V
		$V_{CC} = 2.3V \sim 2.7V$	-	-	0.7	
		$V_{CC} = 3V \sim 5.5V$	-	-	$0.3 * V_{CC}$	
Input Voltage	$V_I$	-	0	-	5.5	V
Output Voltage	$V_O$	-	0	-	$V_{CC}$	V
High Level Output Current	$I_{OH}$	$V_{CC} = 1.65V$	-	-	-4	mA
		$V_{CC} = 2.3V$	-	-	-8	
		$V_{CC} = 3V$	-	-	-16	
		$V_{CC} = 4.5V$	-	-	-32	
Low Level Output Current	$I_{OL}$	$V_{CC} = 1.65V$	-	-	4	mA
		$V_{CC} = 2.3V$	-	-	8	
		$V_{CC} = 3V$	-	-	16	
		$V_{CC} = 4.5V$	-	-	32	

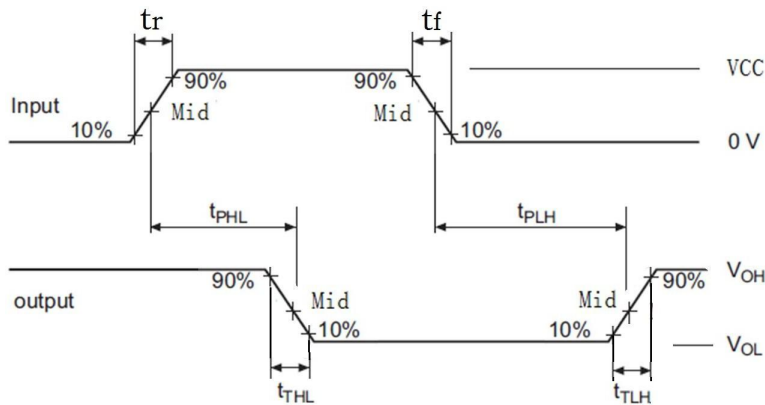
## ■ electrical characteristics

DC electrical characteristics: TA = 25 °C

PROJECTS	SYMBOLS		Test Conditions	Vcc	TYP	Max.	Unit
Upper critical voltage	VT+		-	1.65V	1	-	V
				2.3V	1.35	-	
				3V	1.7	-	
				4.5V	2.5	-	
				5.5V	3	-	
lower critical voltage	VT-		-	1.65V	0.5	-	V
				2.3V	0.7	-	
				3V	1.1	-	
				4.5V	1.65	-	
				5.5V	1.9	-	
Hysteresis Width Voltage	$\Delta V_T$ (VT+ - VT-)		-	1.65V	0.5	-	V
				2.3V	0.65	-	
				3V	0.6	-	
				4.5V	0.85	-	
				5.5V	1.1	-	
High level load voltage	VOH		IOH = -100 uA	1.65V~5.5V	1.64	-	V
			IOH = -4 mA	1.65V	1.47	-	
			IOH = -8mA	2.3V	2.15	-	
			IOH = -16 mA	3V	2.73	-	
			IOH = -32 mA	4.5V	4.0	-	
Low Level Load Voltage	VOL		IOH = 100 uA	1.65V~5.5V	0.01	-	V
			IOH = 4 mA	1.65V	0.11	-	
			IOH = 8 mA	2.3V	0.11	-	
			IOH = 16 mA	3V	0.2	-	
			IOH = 32 mA	4.5V	0.35	-	
Input Current	II	A	VI = 5.5V or GND	0~5.5V	0.01	± 5	uA
Shutdown Current	IOFF	VI	VI = 5.5V	0	0.01	± 10	uA
		VO	VO = 5.5V	0	0.01	± 10	
Operating current	ICC		VI = 5.5 V, IO = 0	1.65V~5.5V	0.01	10	uA
			VI = GND, IO = 0		0.01	10	
Operating current variation value	$\Delta ICC$		A=Vcc -0.6V	3V~5.5V	25	-	uA

AC electrical characteristics: Ta = 25 °C Vcc = 5.0V, tr = tf ≤ 20ns, see test method.

PROJECTS	SYMBOLS	Test Conditions	Min.	TYP	Max.	Unit
Maximum transmission delay time A,B to Y	t <sub>PHL</sub>	CL = 15 pF	-	20	-	ns
	t <sub>PLH</sub>	CL = 15 pF	-	20	-	ns

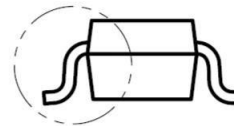
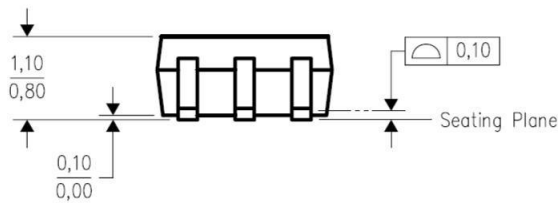
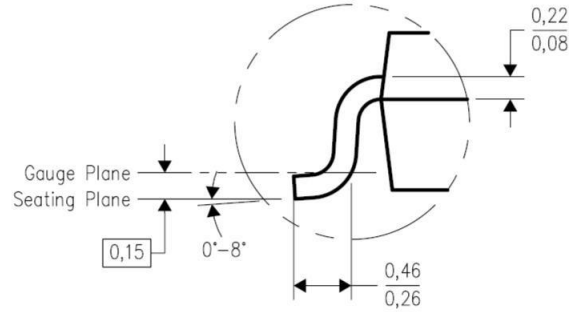
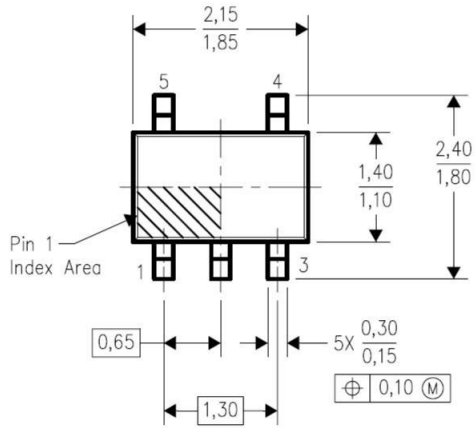


Note:1. The CL capacitor is an external patch capacitor (0603), which is connected near the output pin, and the capacitor ground is close to chip GND;

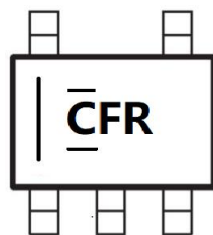
2. Input: port input level, f = 500 kHz, D = 50%; tr = tf ≤ 20 ns;
3. Output: Y-Terminal Output Test.



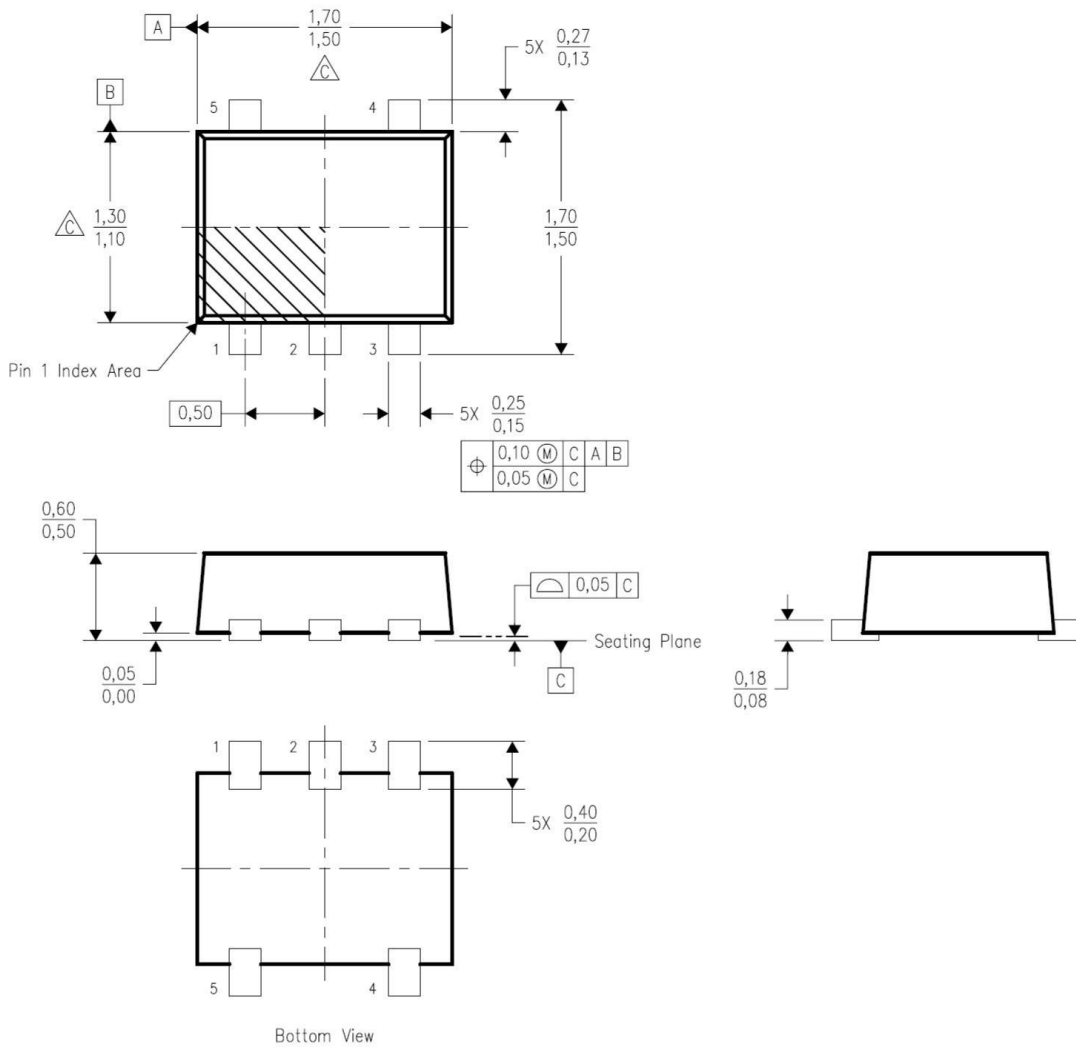
■ Package Information  
DCK (SC70-5)



■ Marking

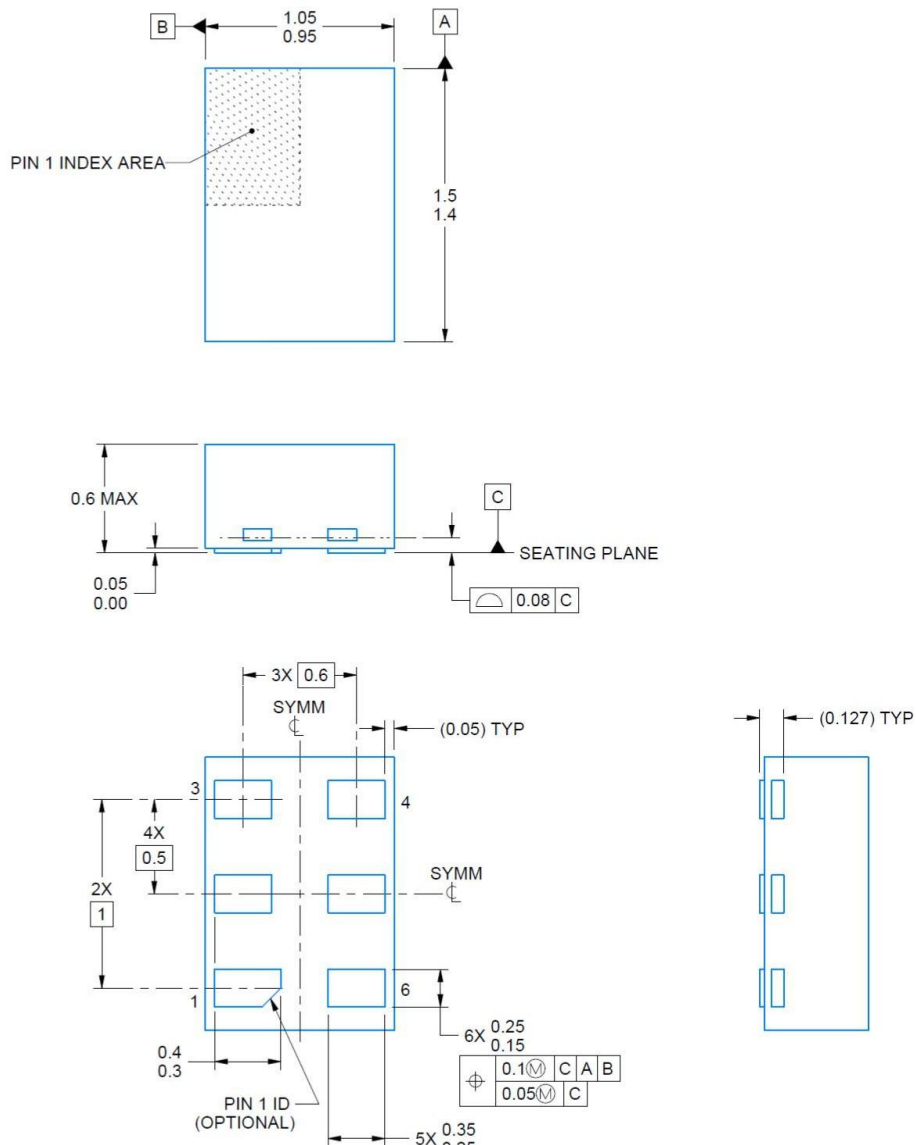


DRL(SOT-553)



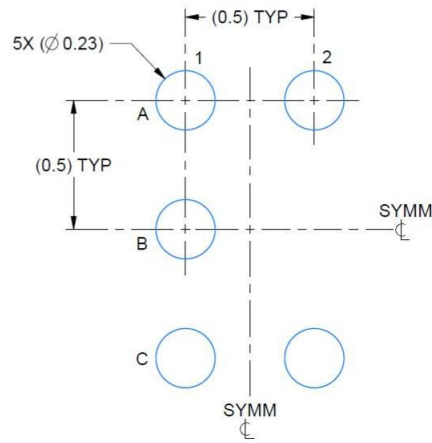


DRY(DFN)





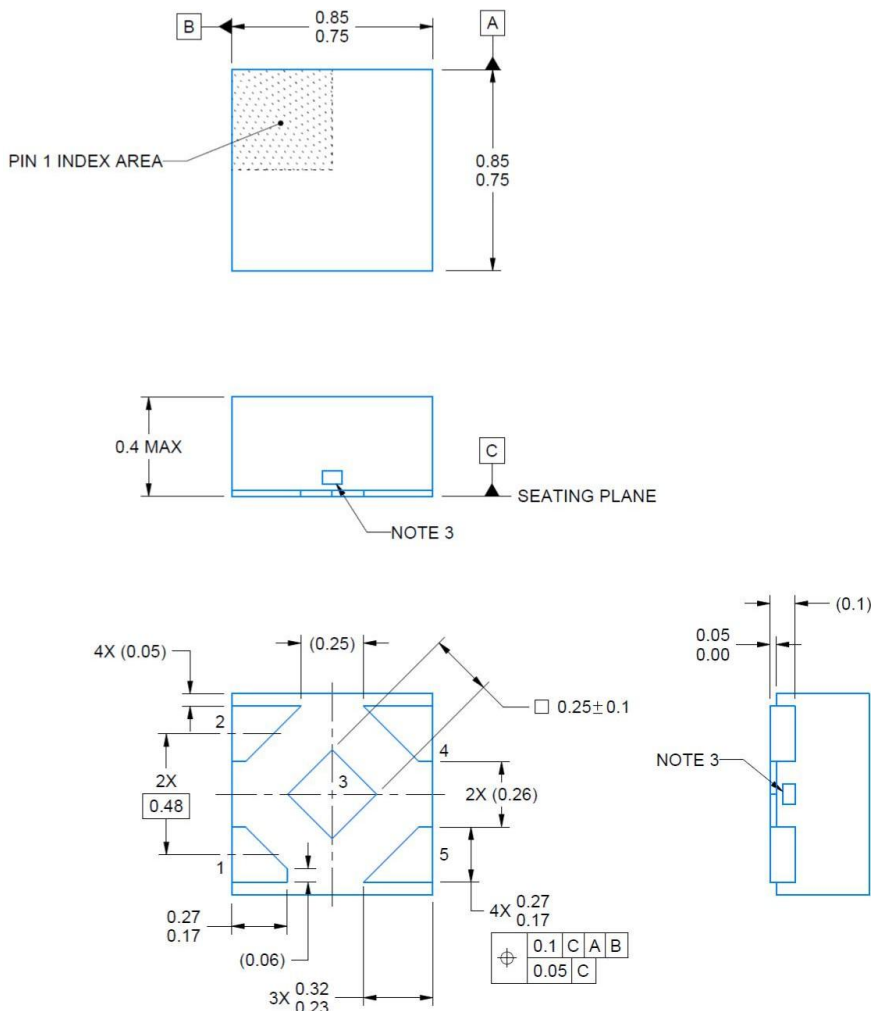
YZP(DSBGA-5)



LAND PATTERN EXAMPLE  
SCALE:40X



DPW(X2SON-5)



Ordering information

Order code	Package	Baseqty	Deliverymode
SN74LVC1G14DBVR	SOT23-5	3000	Tape and reel
SN74LVC1G14DCKR	SC70-5	3000	Tape and reel
SN74LVC1G14DSFR	SON-6	5000	Tape and reel
SN74LVC1G14DRYR	DFN(1*1.5)	5000	Tape and reel
SN74LVC1G14YZPR	DSBGA-5	3000	Tape and reel
SN74LVC1G14DPWR	X2SON-5	3000	Tape and reel
SN74LVC1G14DRLR	SOT-553	4000	Tape and reel