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DS34C87T CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS34C87T is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87T accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. This device has separate enable circuitry for each pair of the four drivers. The DS34C87T is pin compatible to the DS3487T.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

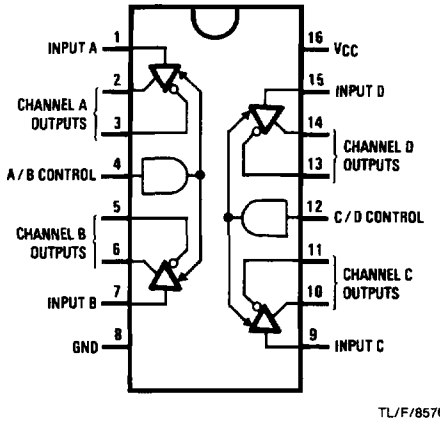
Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount

3

Connection and Logic Diagrams

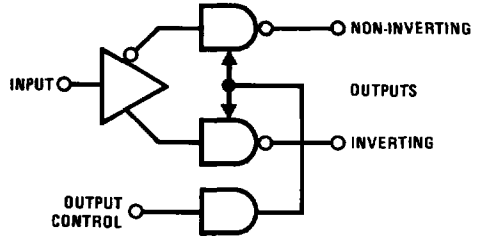
Dual-In-Line Package



TL/F/8576–1

Top View

Order Number DS34C87TJ, DS34C87TM or DS34C87TN
See NS Package Number J16A, M16A or N16E



TL/F/8576–2

Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Power Dissipation (P_D) @ 25°C (Note 3)	
Ceramic "J" Package	2419 mW
Plastic "N" Package	1736 mW
SOIC Package	1226 mW
Lead Temperature (T_L) (Soldering 4 sec)	260°C

This device does not meet 2000V ESD rating. (Note 12)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A) DS34C87T	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 48 mA			0.3	0.5	V
V_T	Differential Output Voltage	R_L = 100 Ω (Note 5)		2.0	3.1		V
$\lvert V_T\rvert - \lvert \overline{V}_T\rvert$	Difference In Differential Output	R_L = 100 Ω (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100 Ω (Note 5)			2.0	3.0	V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference In Common Mode Output	R_L = 100 Ω (Note 5)				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	μA
I_{CC}	Quiescent Supply Current	I_{OUT} = 0 μA, V_{IN} = V_{CC} or GND V_{IN} = 2.4V or 0.5V (Note 6)			200 0.8	500 2.0	μA mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, Control = V_{IL}			±0.5	±5.0	μA
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Notes 5, 7)		−30		−150	mA
I_{OFF}	Power Off Output Leakage Current	V_{CC} = 0V (Note 5)	V_{OUT} = 6V V_{OUT} = −0.25V			100 −100	μA μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.89 mW/°C, J Package 16.13 mW/°C, and M Package 9.80 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V ±10%, t_r, t_f ≤ 6 ns (*Figures 1, 2, 3,* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open		6	11	ns
Skew	(Note 8)	S1 Open		0.5	3	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	ns
t_{PZH}	Output Enable Time	S1 Closed		12	25	ns
t_{PZL}	Output Enable Time	S1 Closed		13	26	ns
t_{PHZ}	Output Disable Time (Note 9)	S1 Closed		4	8	ns
t_{PLZ}	Output Disable Time (Note 9)	S1 Closed		6	12	ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			6		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 9: Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

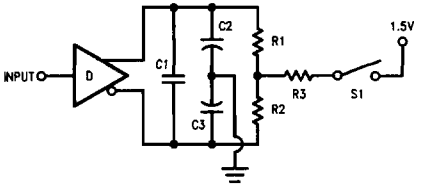
V_{CC} = 5V, T_A = +25°C, t_r ≤ 6 ns, t_f ≤ 6 ns (*Figures 4, 5, 6, 7, 8* and *9*) (Note 11)

Symbol	Parameter	Conditions	DS34C87		DS3487		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output		6	10	10	15	ns
Skew	(Note 8)		1.5	2.0			ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times		4	7	10	15	ns
t_{PHZ}	Output Disable Time (Note 9)	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	8	11	17	25	ns
t_{PLZ}	Output Disable Time (Note 9)	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	7	10	15	25	ns
t_{PZH}	Output Enable Time	C_L = 50 pF, R_L = ∞, S1 Open, S2 Closed	11	19	11	25	ns
t_{PZL}	Output Enable Time	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Open	14	21	15	25	ns

Note 11: This table is provided for comparison purposes only. The values in this table for the DS34C87 reflect the performance of the device but are not tested or guaranteed.

Note 12: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥ 1500V
Outputs ≥ 1000V
EIAJ (0Ω, 200 pF)
All Pins ≥ 350V

AC Test Circuit and Switching Time Waveforms



TL/F/8576–3

Note: C1 = C2 = C3 = 40 pF (including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω

FIGURE 1. AC Test Circuit

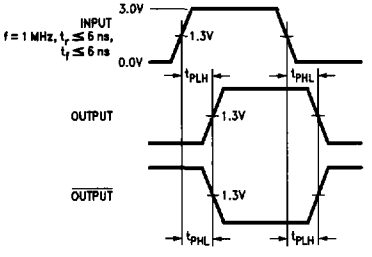


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FIGURE 2. Propagation Delays

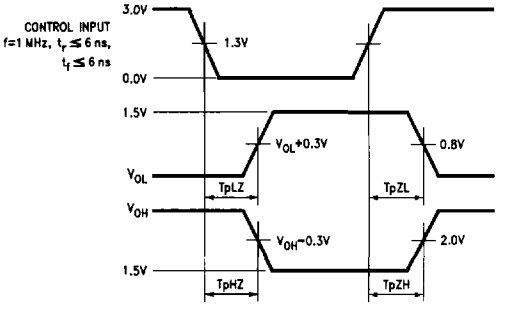

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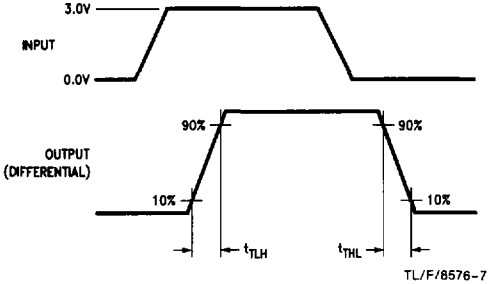
FIGURE 3. Enable and Disable Times



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Input pulse; f = 1 MHz, 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times

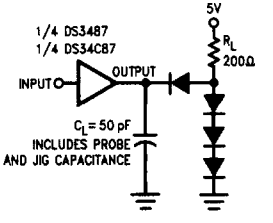

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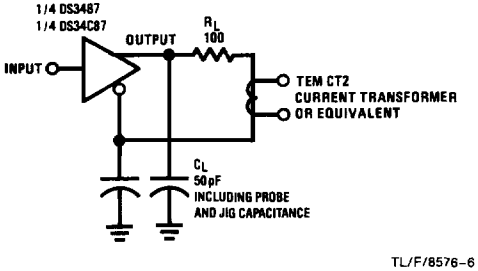
FIGURE 5. Propagation Delays Test Circuit for "LS-Type" Load



TL/F/8576–6

FIGURE 6. Differential Rise and Fall Times Test Circuit for "LS-Type" Load

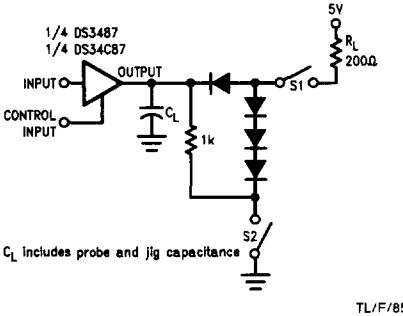


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FIGURE 7. Load Enable and Disable Times Test Circuit for "LS-Type" Load

AC Test Circuit and Switching Time Waveforms (Continued)

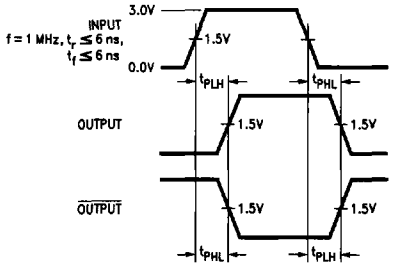

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FIGURE 8. Load Propagation Delays for "LS-Type" Load

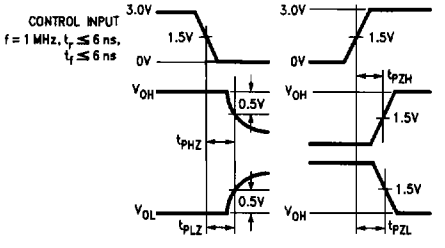

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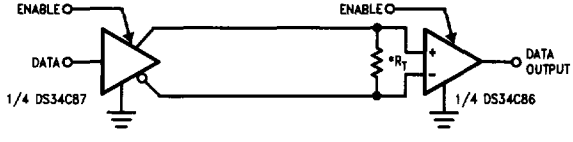
FIGURE 9. Load Enable and Disable Times for "LS-Type" Load

Typical Applications

Two-Wire Balanced System, RS-422



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*R_T is optional although highly recommended to reduce reflection.