

## Product Overview

The NSi824x devices are high reliability quad-channel digital isolators. The NSi824x device is safety certified by UL1577 support several insulations withstand voltages (3kVrms, 5kVrms, 8kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi824x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSi824x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi824x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

## Key Features

- Up to 5000V<sub>rms</sub> Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- AEC-Q100 Grade 1 available for all devices
- High CMTI: 250kV/us
- Chip level ESD: HBM: ±8kV
- Robust Electromagnetic Compatibility (EMC)
  - System-Level ESD, EFT, and Surge Immunity
  - Low Emissions
- Default output high level or low-level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
  - SOP16(300mil)
  - SSOP16
  - SOP16(600mil)

## Safety Regulatory Approvals

- UL recognition: up to 5000V<sub>rms</sub> for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

## Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

## Device Information

Part Number	Package	Body Size
NSi824xW-Q1SWR	SOP16(300mil)	10.30mm × 7.50mm
NSi824xS-Q1SSR	SSOP16	4.90mm × 3.90mm
NSi824xW-Q1SWWR	SOP16(600mil)	10.52mm × 14.0mm

## Functional Block Diagrams

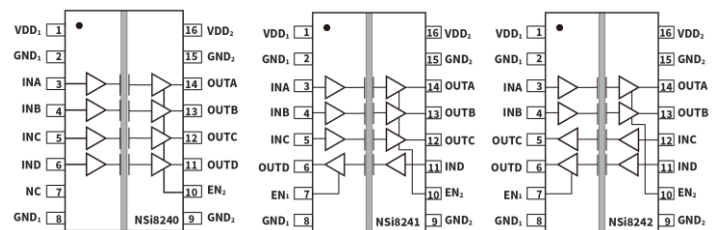


Figure 1. NSi824x Block Diagram

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### 1. Pin Configuration and Functions

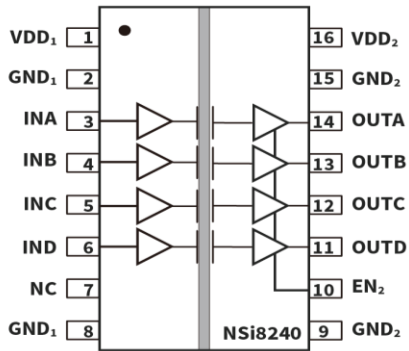


Figure 1.1 NSi8240W Package

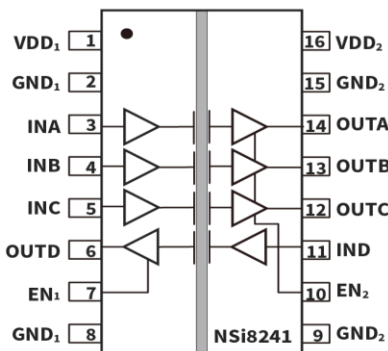


Figure 1.2 NSi8241W Package

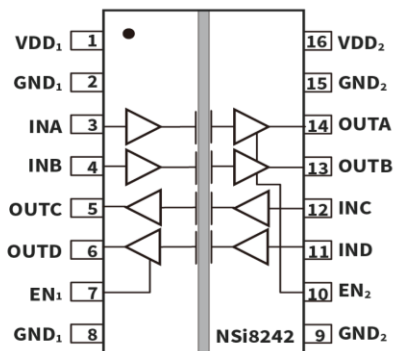


Figure 1.3 NSi8242W Package

**Table 1.1 NSi8240W/ NSi8241W/ NSi8242W Pin Configuration and Description**

<i>NSi8240 W PIN NO.</i>	<i>NSi8241 W PIN NO.</i>	<i>NSi8242 W PIN NO.</i>	<i>SYMBOL</i>	<i>FUNCTION</i>
1	1	1	VDD <sub>1</sub>	Power Supply for Isolator Side 1
2	2	2	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
3	3	3	INA	Logic Input A
4	4	4	INB	Logic Input B
5	5	12	INC	Logic Input C
6	11	11	IND	Logic Input D
7	7	7	NC/ EN <sub>1</sub>	No Connection. Or Output Enable 1. Active high logic input. When EN <sub>1</sub> is high or NC, the output of Side 1 is enabled. When EN <sub>1</sub> is low, the output of Side 1 is disabled to high impedance state.
8	8	8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	9	9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
10	10	10	EN <sub>2</sub>	Output Enable 2. Active high logic input. When EN <sub>2</sub> is high or NC, the output of Side 2 is enabled. When EN <sub>2</sub> is low, the output of Side 2 is disabled to high impedance state.
11	6	6	OUTD	Logic Output D
12	12	5	OUTC	Logic Output C
13	13	13	OUTB	Logic Output B
14	14	14	OUTA	Logic Output A

15	15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	16	VDD2	Power Supply for Isolator Side 2

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	VINA, VINB, VINC, VIND, VOUTA, VOUTB, VOUTC, VOUTD	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I <sub>o</sub>	-15		15	mA	
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>			6.25	kV	
Operating Temperature	T <sub>opr</sub>	-40		125	°C	
Junction Temperature	T <sub>j</sub>			150	°C	
Storage Temperature	T <sub>stg</sub>	-65		150	°C	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

## 3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T <sub>opr</sub>	-40		125	°C
High Level Input Voltage	V <sub>IH</sub>	2			V
Low Level Input Voltage	V <sub>IL</sub>			0.8	V
Data rate	DR			150	Mbps

## 4. Thermal Information

Parameters	Symbol	SOP16(300mil)	SSOP16	SOP16(600mil)	Unit
IC Junction-to-Air Thermal Resistance	$\theta_{JA}$	78.9	140	78.9	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	41.6	54.4	41.1	°C/W
Junction-to-board thermal resistance	$\theta_{JB}$	43.6	51.9	49.5	°C/W

## 5. Specifications

### 5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD <sub>POR</sub>		2.2		V	POR threshold as during power-up
	VDD <sub>HYS</sub>		0.1		V	POR threshold Hysteresis
Input Threshold	V <sub>IT</sub>		1.6		V	Input Threshold at rising edge
	V <sub>IT_HYS</sub>		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V <sub>IH</sub>	2			V	
Low Level Input Voltage	V <sub>IL</sub>			0.8	V	
High Level Output Voltage	V <sub>OH</sub>	VDD-0.4			V	I <sub>OH</sub> = -4mA
Low Level Output Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 4mA
Output Impedance	R <sub>out</sub>		50		ohm	
Input Pull high or low Current	I <sub>pull</sub>		8	15	uA	
Start Up Time after POR	tr <sub>bs</sub>		10		us	
Common Mode Transient Immunity	CMTI	±200	±250		kV/us	See <a href="#">Figure 5.11</a> , C <sub>L</sub> = 15pF

**5.2. Supply Current Characteristics – 5V Supply**

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8240</b>					
	I <sub>DD1</sub> (Q0)		1.24	2.04	mA	All Input 0V for NSi8240x0 Or All Input at supply for NSi8240x1
	I <sub>DD2</sub> (Q0)		2.94	4.84	mA	
	I <sub>DD1</sub> (Q1)		5.26	8.68	mA	All Input at supply for NSi8240x0 Or All Input 0V for NSi8240x1
	I <sub>DD2</sub> (Q1)		3.02	4.98	mA	
	I <sub>DD1</sub> (1M)		3.4	5.1	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.78	4.39	mA	
	I <sub>DD1</sub> (10M)		3.56	5.34	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.26	6.68	mA	
	I <sub>DD1</sub> (100M)		4.98	7.47	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		18.44	38.12	mA	
	<b>NSi8241</b>					
	I <sub>DD1</sub> (Q0)		1.66	2.74	mA	All Input 0V for NSi8241x0 Or All Input at supply for NSi8241x1
	I <sub>DD2</sub> (Q0)		2.51	4.14	mA	
	I <sub>DD1</sub> (Q1)		4.70	7.76	mA	All Input at supply for NSi8241x0 Or All Input 0V for NSi8241x1
	I <sub>DD2</sub> (Q1)		3.58	5.91	mA	
	I <sub>DD1</sub> (1M)		3.25	4.875	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.94	4.41	mA	
	I <sub>DD1</sub> (10M)		3.74	5.61	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.09	6.135	mA	
	I <sub>DD1</sub> (100M)		8.35	12.76	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		15.08	29.67	mA	
	<b>NSi8242</b>					
	I <sub>DD1</sub> (Q0)		2.09	3.44	mA	All Input 0V for NSi8242x0 Or All Input at supply for NSi8242x1
	I <sub>DD2</sub> (Q0)		2.09	3.44	mA	
	I <sub>DD1</sub> (Q1)		4.14	6.83	mA	All Input at supply for NSi8242x0 Or All Input 0V for NSi8242x1
	I <sub>DD2</sub> (Q1)		4.14	6.83	mA	
	I <sub>DD1</sub> (1M)		3.09	4.635	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.09	4.635	mA	
	I <sub>DD1</sub> (10M)		3.91	5.865	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.91	5.865	mA	
	I <sub>DD1</sub> (100M)		11.71	21.22	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		11.71	21.22	mA	

**5.3. Supply Current Characteristics –3.3V Supply**

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8240</b>					
	I <sub>DD1</sub> (Q0)		1.19	1.96	mA	All Input 0V for NSi8240x0 Or All Input at supply for NSi8240x1
	I <sub>DD2</sub> (Q0)		2.87	4.74	mA	
	I <sub>DD1</sub> (Q1)		5.21	8.59	mA	All Input at supply for NSi8240x0 Or All Input 0V for NSi8240x1
	I <sub>DD2</sub> (Q1)		2.95	4.86	mA	
	I <sub>DD1</sub> (1M)		3.32	4.98	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.62	4.22	mA	
	I <sub>DD1</sub> (10M)		3.42	5.13	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.60	5.72	mA	
	I <sub>DD1</sub> (100M)		4.40	6.6	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		13.00	25.73	mA	
	<b>NSi8241</b>					
	I <sub>DD1</sub> (Q0)		1.61	2.66	mA	All Input 0V for NSi8241x0 Or All Input at supply for NSi8241x1
	I <sub>DD2</sub> (Q0)		2.45	4.04	mA	
	I <sub>DD1</sub> (Q1)		4.64	7.66	mA	All Input at supply for NSi8241x0 Or All Input 0V for NSi8241x1
	I <sub>DD2</sub> (Q1)		3.51	5.79	mA	
	I <sub>DD1</sub> (1M)		3.15	4.725	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.80	4.2	mA	
	I <sub>DD1</sub> (10M)		3.47	5.205	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.56	5.34	mA	
	I <sub>DD1</sub> (100M)		6.55	9.825	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		10.85	20.31	mA	
	<b>NSi8242</b>					
	I <sub>DD1</sub> (Q0)		2.03	3.35	mA	All Input 0V for NSi8242x0 Or All Input at supply for NSi8242x1
	I <sub>DD2</sub> (Q0)		2.03	3.35	mA	
	I <sub>DD1</sub> (Q1)		4.08	6.72	mA	All Input at supply for NSi8242x0 Or All Input 0V for NSi8242x1
	I <sub>DD2</sub> (Q1)		4.08	6.72	mA	
	I <sub>DD1</sub> (1M)		2.97	4.455	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.97	4.455	mA	
	I <sub>DD1</sub> (10M)		3.51	5.265	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.51	5.265	mA	
	I <sub>DD1</sub> (100M)		8.70	14.93	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		8.70	14.93	mA	

**5.4. Supply Current Characteristics–2.5V Supply**

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40 °C to 125 °C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25 °C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8240</b>					
	I <sub>DD1</sub> (Q0)		1.17	1.92	mA	All Input 0V for NSi8240x0 Or

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I <sub>DD2</sub> (Q0)		2.83	4.66	mA	All Input at supply for NSi8240x1
	I <sub>DD1</sub> (Q1)		5.13	8.46	mA	All Input at supply for NSi8240x0
	I <sub>DD2</sub> (Q1)		2.89	4.77	mA	Or All Input 0V for NSi8240x1
	I <sub>DD1</sub> (1M)		3.28	4.92	mA	All Input with 1Mbps,
	I <sub>DD2</sub> (1M)		2.54	4.1	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (10M)		3.34	5.01	mA	All Input with 10Mbps,
	I <sub>DD2</sub> (10M)		3.30	5.23	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (100M)		3.96	5.94	mA	All Input with 100Mbps,
	I <sub>DD2</sub> (100M)		10.44	20.15	mA	C <sub>L</sub> =15pF
<b>NSi8241</b>						
	I <sub>DD1</sub> (Q0)		1.58	2.61	mA	All Input 0V for NSi8241x0 Or
	I <sub>DD2</sub> (Q0)		2.41	3.98	mA	All Input at supply for NSi8241x1
	I <sub>DD1</sub> (Q1)		4.57	7.54	mA	All Input at supply for NSi8241x0
	I <sub>DD2</sub> (Q1)		3.45	5.69	mA	Or All Input 0V for NSi8241x1
	I <sub>DD1</sub> (1M)		3.10	4.65	mA	All Input with 1Mbps,
	I <sub>DD2</sub> (1M)		2.73	4.095	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (10M)		3.33	4.995	mA	All Input with 10Mbps,
	I <sub>DD2</sub> (10M)		3.31	4.965	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (100M)		5.58	8.37	mA	All Input with 100Mbps,
	I <sub>DD2</sub> (100M)		8.82	16.05	mA	C <sub>L</sub> = 15pF
<b>NSi8242</b>						
	I <sub>DD1</sub> (Q0)		2.00	3.29	mA	All Input 0V for NSi8242x0 Or
	I <sub>DD2</sub> (Q0)		2.00	3.29	mA	All Input at supply for NSi8242x1
	I <sub>DD1</sub> (Q1)		4.01	6.62	mA	All Input at supply for NSi8242x0
	I <sub>DD2</sub> (Q1)		4.01	6.62	mA	Or All Input 0V for NSi8242x1
	I <sub>DD1</sub> (1M)		2.91	4.365	mA	All Input with 1Mbps,
	I <sub>DD2</sub> (1M)		2.91	4.365	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (10M)		3.32	4.98	mA	All Input with 10Mbps,
	I <sub>DD2</sub> (10M)		3.32	4.98	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (100M)		7.20	12.21	mA	All Input with 100Mbps,
	I <sub>DD2</sub> (100M)		7.20	12.21	mA	C <sub>L</sub> = 15pF



**5.5. Switching Characteristics - 5V Supply**

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t <sub>PLH</sub>	2.5	6.54	15	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>	2.5	8.30	15	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT</sub> (PK)		350		ps	
Channel-to-Channel Delay Skew	t <sub>SK</sub> (c2c)			2.5	ns	
Part-to-Part Delay Skew	t <sub>SK</sub> (p2p)			5.0	ns	
Disable high to Tri-State	t <sub>PHZ</sub>		10.0	30	ns	See <a href="#">Figure 5.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZH</sub>		8.3	30	ns	See <a href="#">Figure 5.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Disable low to Tri-State	t <sub>PLZ</sub>		10.2	30	ns	See <a href="#">Figure 5.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZL</sub>		8.6	30	ns	See <a href="#">Figure 5.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k

**5.6. Switching Characteristics - 3.3V Supply**

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t <sub>PLH</sub>	2.5	7.5	15	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>	2.5	8.7	15	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 5.9</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT</sub> (PK)		350		ps	
Channel-to-Channel Delay Skew	t <sub>SK</sub> (c2c)			2.5	ns	
Part-to-Part Delay Skew	t <sub>SK</sub> (p2p)			5.0	ns	
Disable high to Tri-State	t <sub>PHZ</sub>		11.6	30	ns	See <a href="#">Figure 5.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZH</sub>		11.7	30	ns	See <a href="#">Figure 5.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Disable low to Tri-State	t <sub>PLZ</sub>		14.5	30	ns	See <a href="#">Figure 5.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Enable to Data high Valid	$t_{PZL}$		11.8	30	ns	See <a href="#">Figure 5.10</a> , $C_L = 15pF$ , $R_L=1k$

### 5.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	$t_{PLH}$	2.5	9.0	15	ns	See <a href="#">Figure 5.9</a> , $C_L = 15pF$
	$t_{PHL}$	2.5	9.3	15	ns	See <a href="#">Figure 5.9</a> , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See <a href="#">Figure 5.9</a> , $C_L = 15pF$
Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 5.9</a> , $C_L = 15pF$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 5.9</a> , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	
Disable high to Tri-State	$t_{PHZ}$		12.2	30	ns	See <a href="#">Figure 5.10</a> , $C_L = 15pF$ , $R_L=1k$
Enable to Data high Valid	$t_{PZH}$		17.0	30	ns	See <a href="#">Figure 5.10</a> , $C_L = 15pF$ , $R_L=1k$
Disable low to Tri-State	$t_{PLZ}$		17.2	30	ns	See <a href="#">Figure 5.10</a> , $C_L = 15pF$ , $R_L=1k$
Enable to Data high Valid	$t_{PZL}$		17.8	30	ns	See <a href="#">Figure 5.10</a> , $C_L = 15pF$ , $R_L=1k$

### 5.8. Typical Performance Characteristics

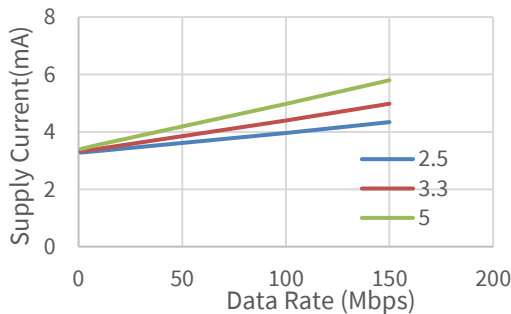


Figure 5.1 NSi8240 VDD1 Supply Current vs Data Rate

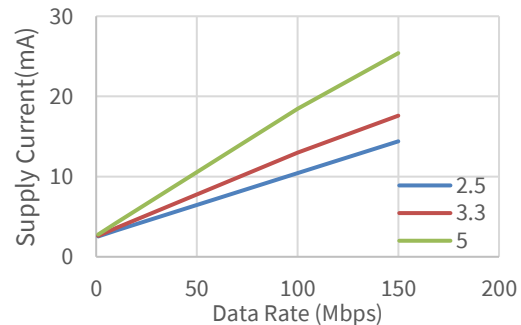


Figure 5.2 NSi8240 VDD2 Supply Current vs Data Rate

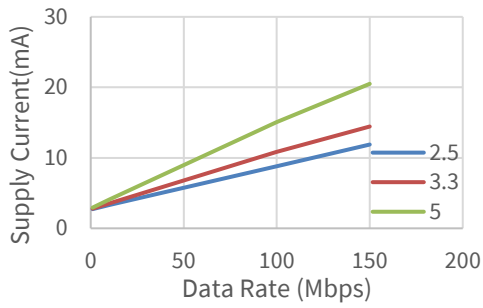


Figure 5.3 NSi8241 VDD1 Supply Current vs Data Rate

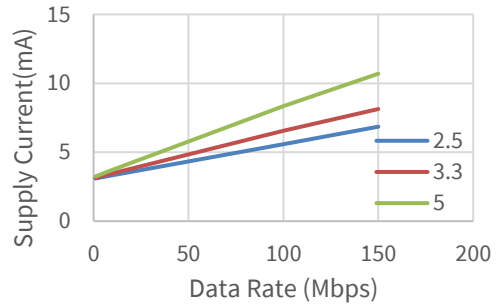


Figure 5.4 NSi8241 VDD2 Supply Current vs Data Rate

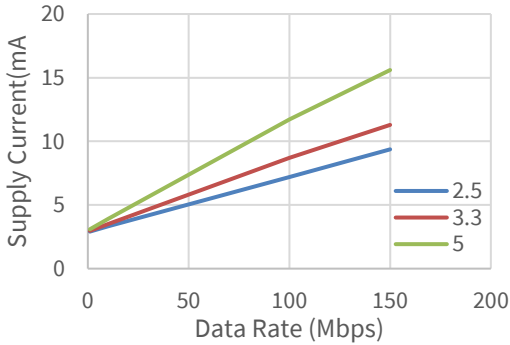


Figure 5.5 NSi8242 VDD1 Supply Current vs Data Rate

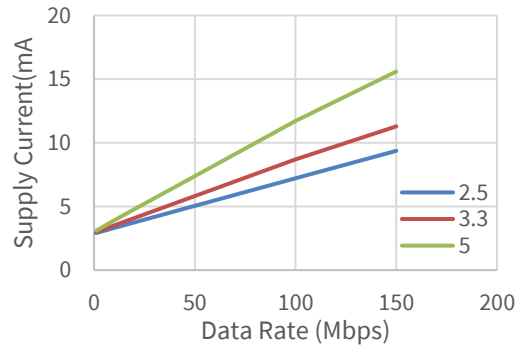


Figure 5.6 NSi8242 VDD2 Supply Current vs Data Rate

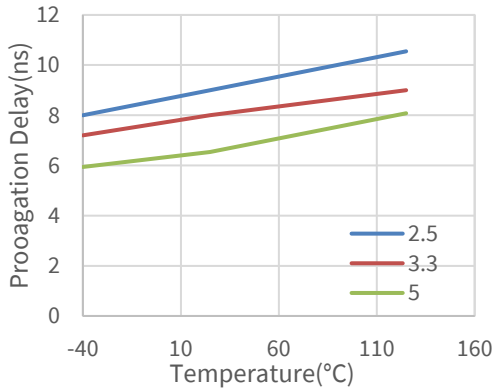


Figure 5.7 Rising Edge Propagation Delay Vs Temp

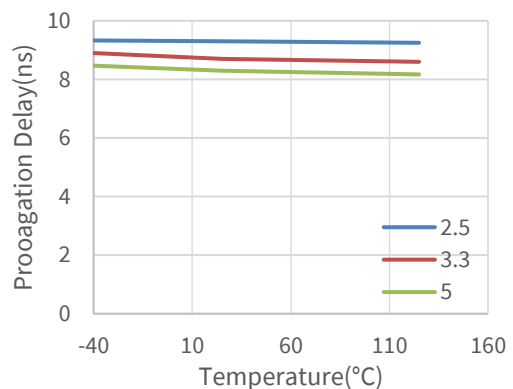


Figure 5.8 Falling Edge Propagation Delay Vs Temp

**5.9. Parameter Measurement Information**

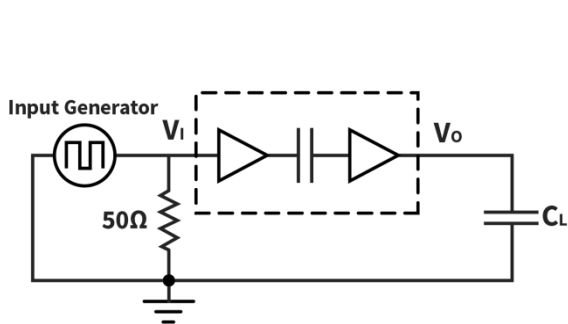
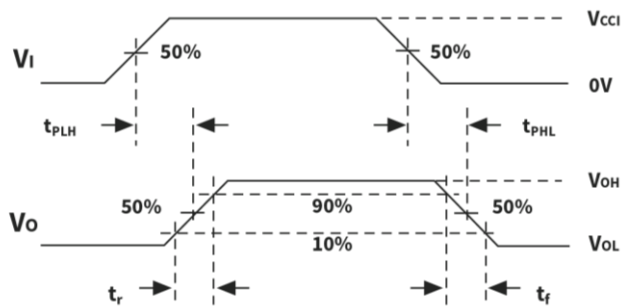


Figure 5.9 Switching Characteristics Test Circuit and Waveform



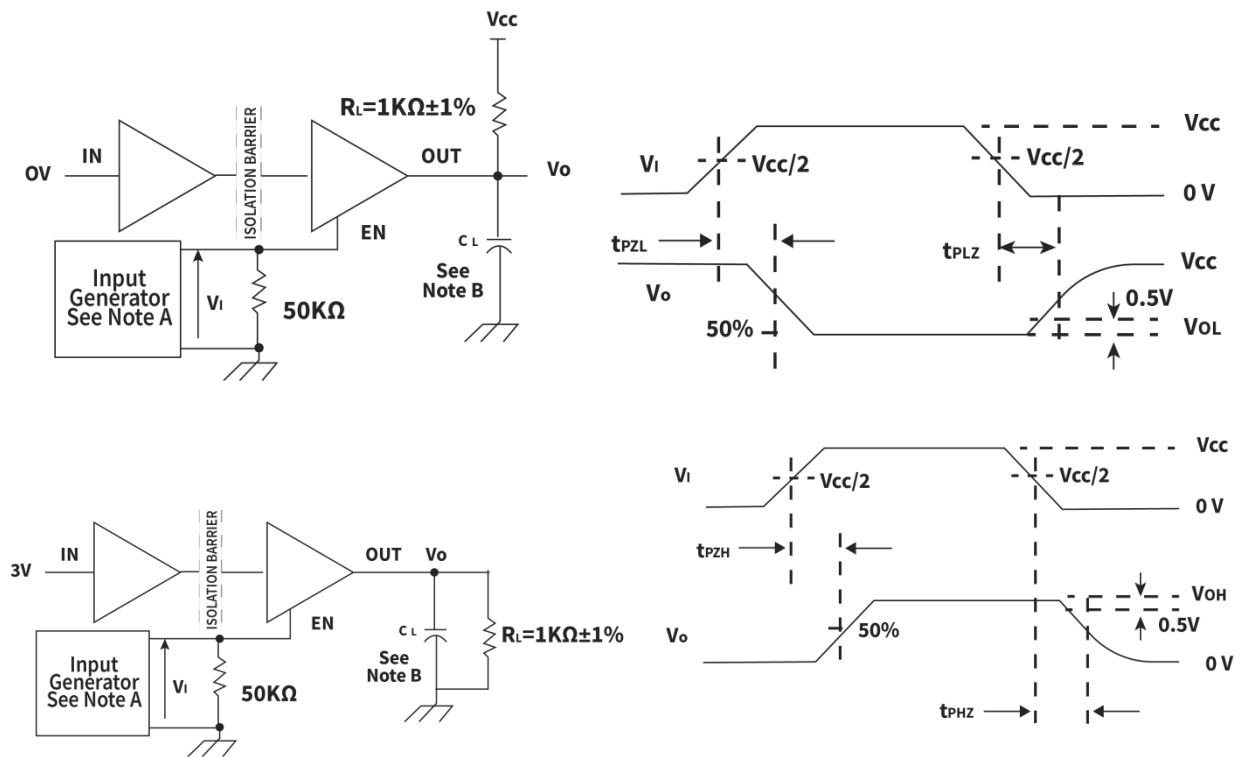


Figure 5.10 Enable/Disable Propagation Delay Time Test Circuit and Waveform

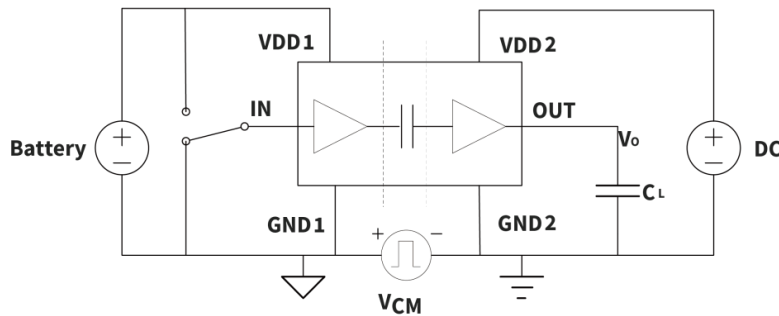


Figure 5.11 Common-Mode Transient Immunity Test Circuit

## 6. High Voltage Feature Description

### 6.1. Insulation and Safety Related Specifications

Description	Test Condition	Symbo l	Value			Unit
			SOP16 (300mil)	SSOP16	SOP16 (600mil)	
Min. External Air Gap (Clearance)		CLR	8	3.9	15	mm
Min. External Tracking (Creepage)		CPG	8	3.9	15	mm
Distance through the Insulation		DTI	28			um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600	>400	>600	V
Material Group	IEC 60112		I	II	I	
Installation Classification per DIN VDE 0110						
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to III	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	I to II	I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to IV	I	I to IV	
For Rated Mains Voltage ≤ 1000Vrms			I to III	/	I to IV	
Insulation Specification per DIN VDE V 0884-11:2017-01 <sup>1)</sup>						
Climatic Category			40/125/21			
Pollution Degree	per DIN VDE 0110, Table 1		2			
Maximum Working Isolation Voltage	AC voltage	V <sub>IOWM</sub>	1500	400	1500	V <sub>RMS</sub>
	DC voltage		2121	565	2121	V <sub>DC</sub>
Maximum Repetitive Isolation Voltage		V <sub>IORM</sub>	2121	565	2121	V <sub>peak</sub>
Input to Output Test Voltage, Method B1	V <sub>ini. b</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.875, t <sub>ini</sub> = t <sub>m</sub> = 1 sec, q <sub>pd</sub> ≤ 5 pC, 100% production test	V <sub>pd (m)</sub>	3977	/	3977	V <sub>peak</sub>
	V <sub>ini. b</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.5, t <sub>ini</sub> = t <sub>m</sub> = 1 sec, q <sub>pd</sub> ≤ 5 pC, 100% production test	V <sub>pd (m)</sub>	/	847	/	V <sub>peak</sub>
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	V <sub>ini. a</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.6, t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec, q <sub>pd</sub> ≤ 5 pC	V <sub>pd (m)</sub>	3394	/	3394	V <sub>peak</sub>
	V <sub>ini. a</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.3, t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec, q <sub>pd</sub> ≤ 5 pC	V <sub>pd (m)</sub>	/	678	/	V <sub>peak</sub>
Input to Output Test Voltage, Method A. After Input and Output	V <sub>ini. a</sub> = V <sub>IOTM</sub> , V <sub>pd(m)</sub> = V <sub>IORM</sub> × 1.2,	V <sub>pd (m)</sub>	2545	678	2545	V <sub>peak</sub>

Description	Test Condition	Symbol	Value			Unit
Safety Test Subgroup 2 and Subgroup 3	$t_{ini} = 60 \text{ sec}, t_m = 10 \text{ sec}, q_{pd} \leq 5 \text{ pC}$					
Maximum Transient Isolation Voltage	$t = 60 \text{ sec}$	$V_{IOTM}$	8000	5000	12000	$V_{peak}$
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	$V_{IOSM}$	6250	/	6250	$V_{peak}$
	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.3 \times V_{IOSM}$	$V_{IOSM}$	/	5384	/	$V_{peak}$
Isolation Resistance	$V_{IO} = 500 \text{ V}, T_{amb} = T_s$	$R_{IO}$	$>10^9$			$\Omega$
	$V_{IO} = 500 \text{ V}$ $100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$		$>10^{11}$			$\Omega$
Isolation Capacitance	$f = 1\text{MHz}$	$C_{IO}$	1.2			pF
Insulation Specification per UL1577						
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}, t = 1 \text{ sec}, 100\% \text{ production test}$	$V_{ISO}$	5000	3000	8000	$V_{rms}$

- 1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

### 6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi824x-Q1SWR (SOP16(300mil)/SOP16(600mil))

Description	Test Condition	Value		Unit
Safety Supply Power	$R_{\theta JA} = 78.9 \text{ }^\circ\text{C}/\text{W}^1, T_J = 150 \text{ }^\circ\text{C}, T_A = 25 \text{ }^\circ\text{C}$	1584		mW
Safety Supply Current	$R_{\theta JA} = 78.9 \text{ }^\circ\text{C}/\text{W}^1, V_I = 5\text{V}, T_J = 150 \text{ }^\circ\text{C}, T_A = 25 \text{ }^\circ\text{C}$	316.8		mA
Safety Temperature <sup>2)</sup>		150		$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SOP16(300mil)/SOP16(600mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

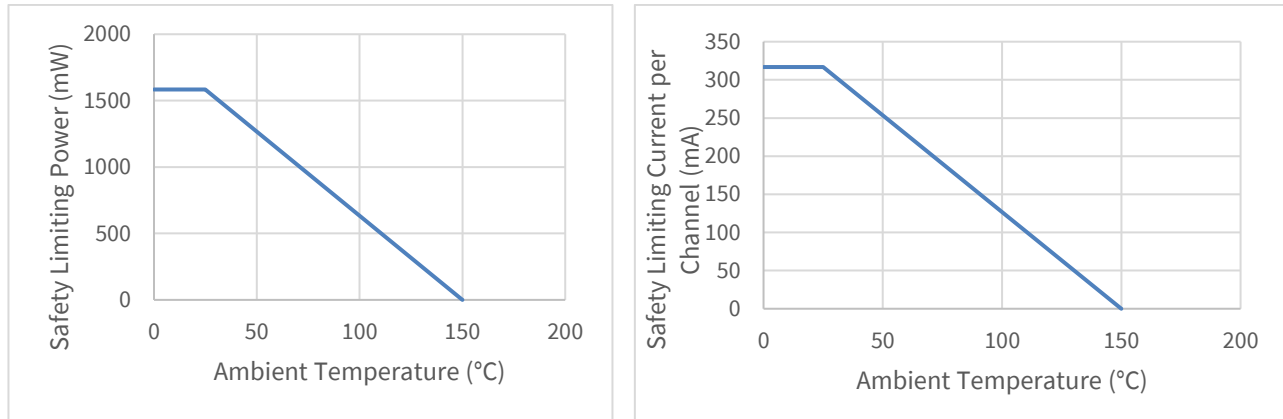


Figure 6.1 NSi824xW Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi824x-Q1SSR (SSOP16)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 140^{\circ}\text{C}/\text{W}^{1)}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$	880	mW
Safety Supply Current	$R_{\theta JA} = 140^{\circ}\text{C}/\text{W}^{1)}$ , $V_I = 5\text{V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$	176	mA
Safety Temperature <sup>2)</sup>		150	°C

- 1) Calculate with the junction-to-air thermal resistance,  $R_{\theta JA}$ , of SSOP16 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature ( $T_J$ ) specified for the device.

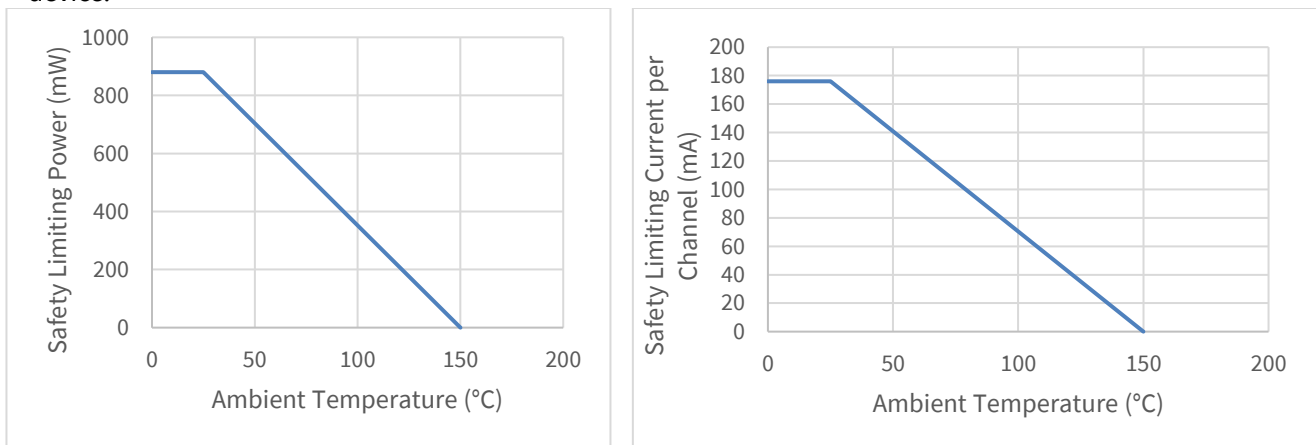


Figure 6.2 NSi824xS Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

**6.3. Regulatory Information**

The NSi824xW-Q1SWR are approved or pending approval by the organizations listed in table.

<b>CUL</b>			<b>VDE</b>		<b>CQC</b>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	5000V <sub>rms</sub>	Single Protection, 5000V <sub>rms</sub> Isolation voltage	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V <sub>rms</sub> Isolation voltage	Single Protection, 5000V <sub>rms</sub> Isolation voltage			Reinforce Insulation 2121V <sub>peak</sub> , V <sub>IOSM</sub> =6250V <sub>peak</sub>	Reinforced insulation
File (E500602)	File (E500602)			File (40052820)	File (CQC20001264939)

The NSi824xS-Q1SSR are approved or pending approval by the organizations listed in table.

<b>CUL</b>			<b>VDE</b>		<b>CQC</b>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	3000V <sub>rms</sub>	Single Protection, 3000V <sub>rms</sub> Isolation voltage	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V <sub>rms</sub> Isolation voltage	Single Protection, 3000V <sub>rms</sub> Isolation voltage			Basic Insulation 565V <sub>peak</sub> , V <sub>IOSM</sub> =5384V <sub>peak</sub>	Basic insulation
File (pending)	File (pending)			File (pending)	File (pending)

The NSi824xW-Q1SWWR are approved or pending approval by the organizations listed in table.

<b>CUL</b>			<b>VDE</b>		<b>CQC</b>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	8000V <sub>rms</sub>	Single Protection, 8000V <sub>rms</sub> Isolation voltage	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 8000V <sub>rms</sub> Isolation voltage	Single Protection, 8000V <sub>rms</sub> Isolation voltage			Reinforce Insulation 2121V <sub>peak</sub> , V <sub>IOSM</sub> =6250V <sub>peak</sub>	Reinforced insulation
File (pending)	File (pending)			File (pending)	File (pending)



## 7. Function Description

### 7.1. Overview

The NSi824x is a Quad-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi824x devices are high reliability quad-channel digital isolator with AEC-Q100 qualified. The NSi824x device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi824x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi824x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi824x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi824x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 7.1 Output status vs. power status

<b>Input</b>	<b>EN<sub>x</sub></b>	<b>VDD1 status</b>	<b>VDD2 status</b>	<b>Output</b>	<b>Comment</b>
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output Disabled, the output is high impedance
X	H or NC	Unready	Ready	L(NSi824xx 0) H(NSi824xx 1)	The output follows the same status with the input after input side VDD1 is powered on.
X	L	Unready	Ready	Z	Output Disabled, the output is high impedance
X	X	Ready	Unready	X	The output follows the same status with the input after output side VDD2 is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDD1 is input side power; VDD2 is out side power.					

**7.2. OOK Modulation**

NSi824x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

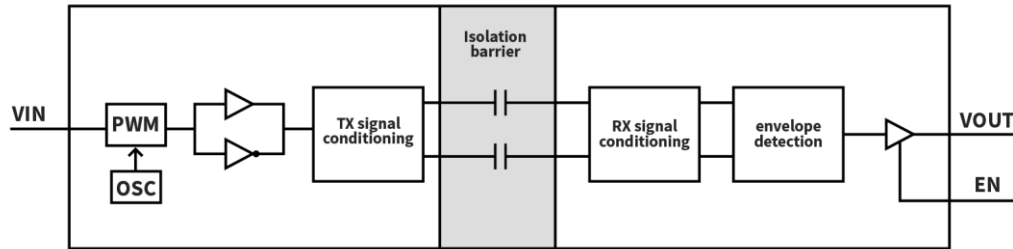


Figure 7.1 Single Channel Function Block Diagram

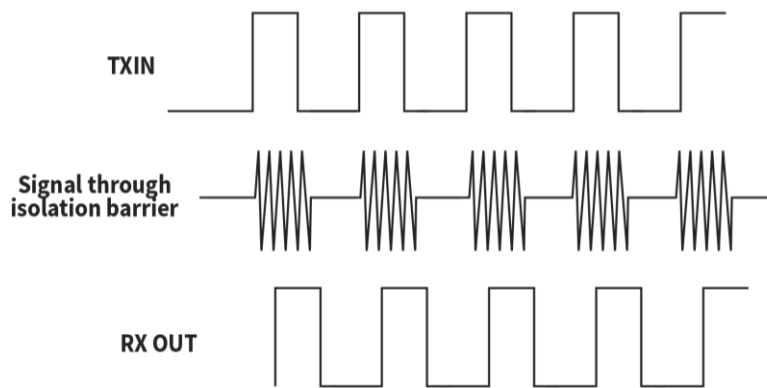


Figure 7.2 OOK Modulation

## 8. Application Note

### 8.1. Typical Application Circuit

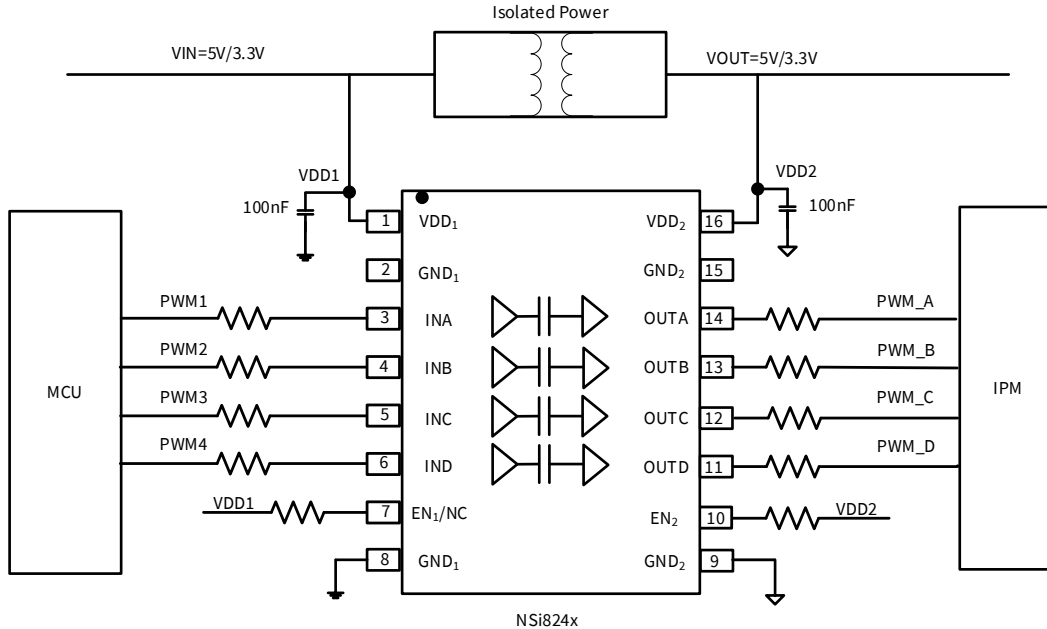


Figure 8.1 Typical PWM isolation circuit for IPM

### 8.2. PCB Layout

The NSi824x requires a 0.1  $\mu\text{F}$  bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300  $\Omega$ ) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50  $\Omega$ ,  $\pm 40\%$ . When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

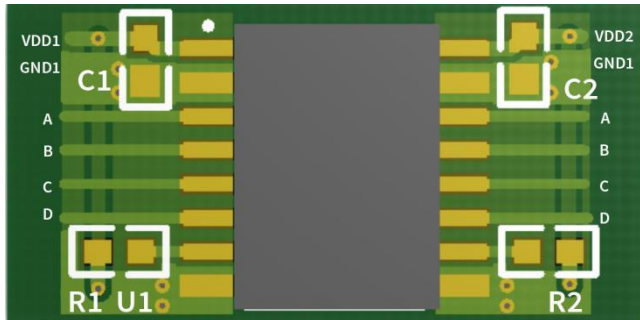


Figure 8.2 Recommended PCB Layout — Top Layer



Figure 8.3 Recommended PCB Layout — Bottom Layer

**8.3. High Speed Performance**

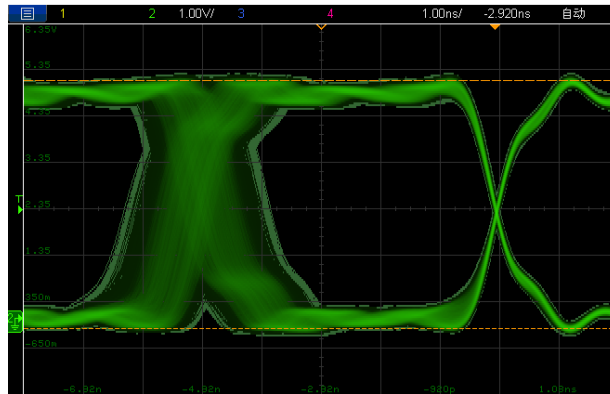


Figure8.4 Eye Diagram

**8.4. Typical Supply Current Equations**

The typical supply current of NSi824x can be calculated using below equations.  $I_{DD1}$  and  $I_{DD2}$  are typical supply currents measured in mA,  $f$  is data rate measured in Mbps,  $C_L$  is the capacitive load measured in pF

**NSi8240:**

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD1 * f * C_L * c1 * 10^{-9}$$

When  $a1$  is the channel number of low input at side 1,  $b1$  is the channel number of high input at side 1,  $c1$  is the channel number of switch signal input at side 1.

**NSi8241:**

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When  $b1$  is the channel number of high input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of high input at side 2,  $c2$  is the channel number of switch signal input at side 2.

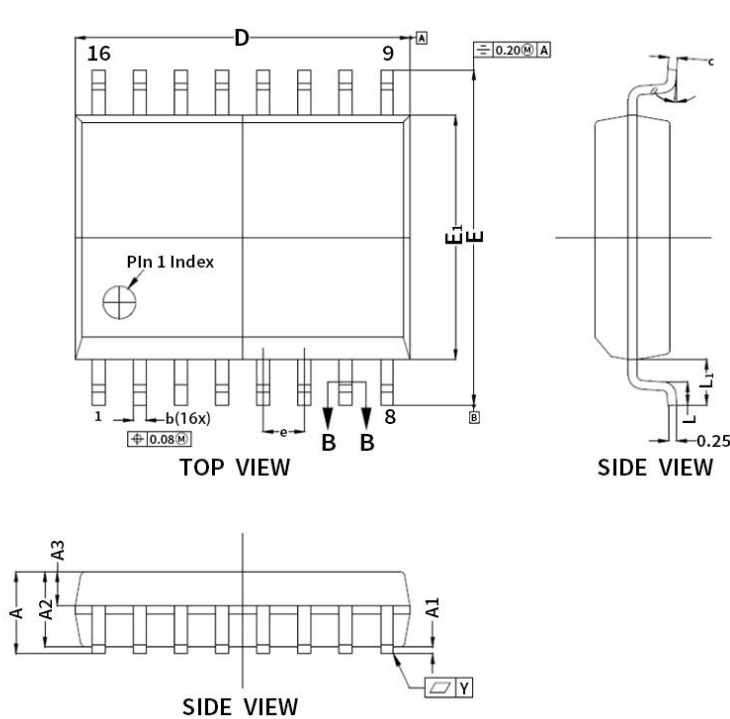
**NSi8242:**

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When  $b1$  is the channel number of high input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of high input at side 2,  $c2$  is the channel number of switch signal input at side 2.

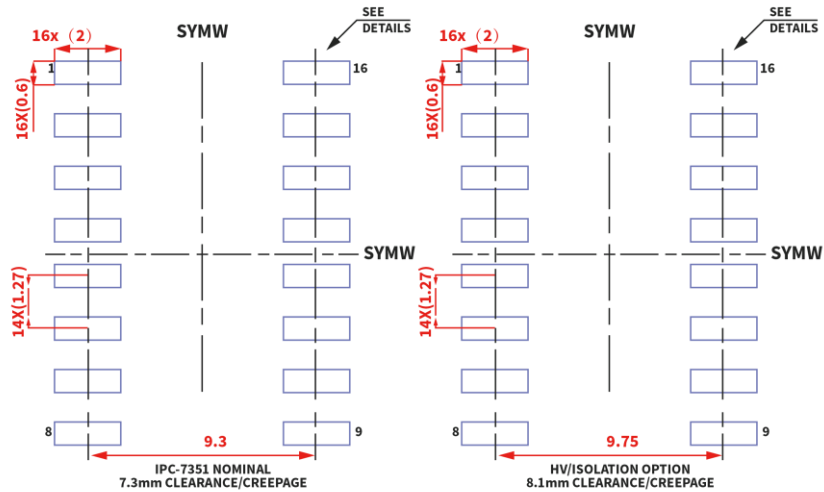
### 9. Package Information



\* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 9.1 SOP16(300mil) Package Shape and Dimension in millimeters

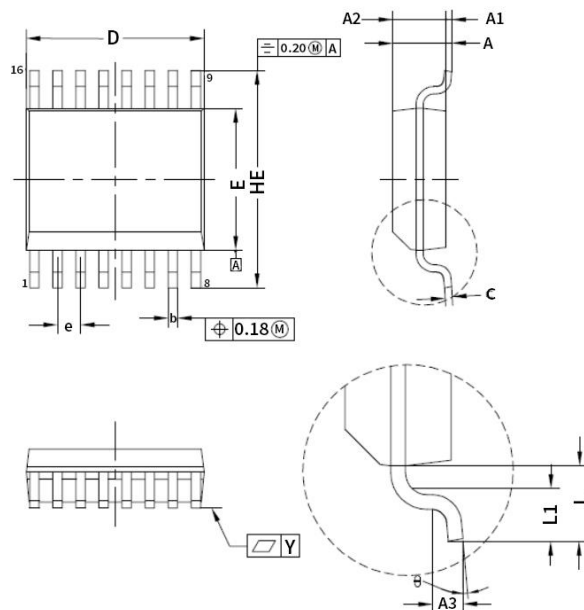


#### LAND PATTERN EXAMPLE(mm)



#### SOLDER MASK DETAILS

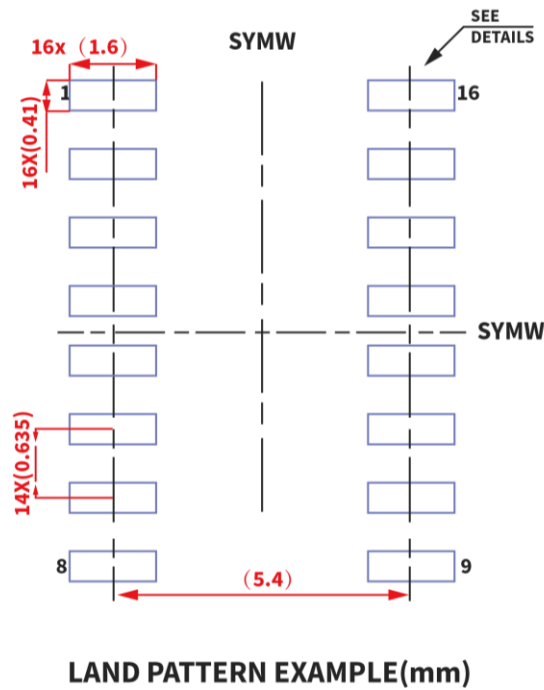
Figure 9.2 SOP16(300mil) Package Board Layout Example



\* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

Figure 9.3 SSOP16 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)

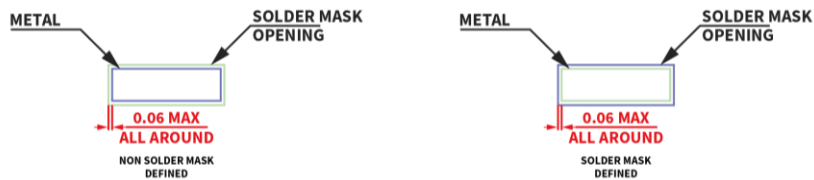
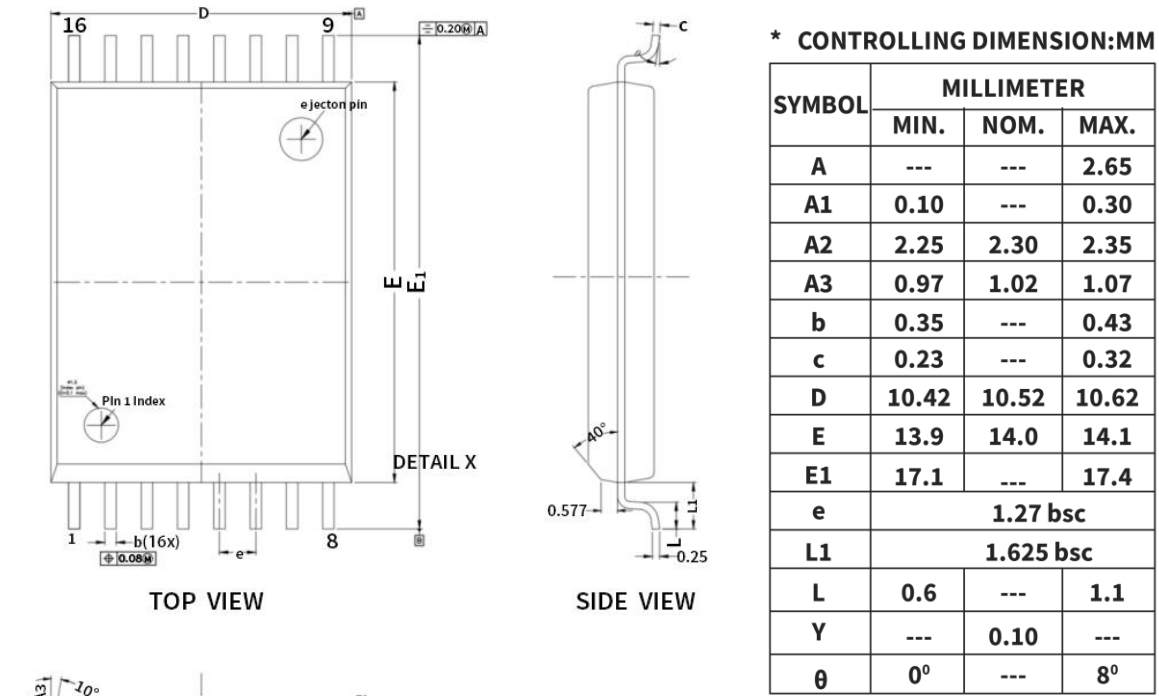


Figure 9.4 SSOP16 Package Board Layout Example



**NOTES**  
 1.0 COPWNARITY APPUES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.5 SOP16(600mil)/SOWW16 Package Shape and Dimension in millimeters

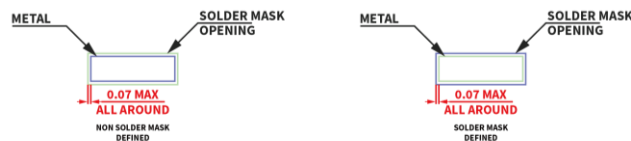
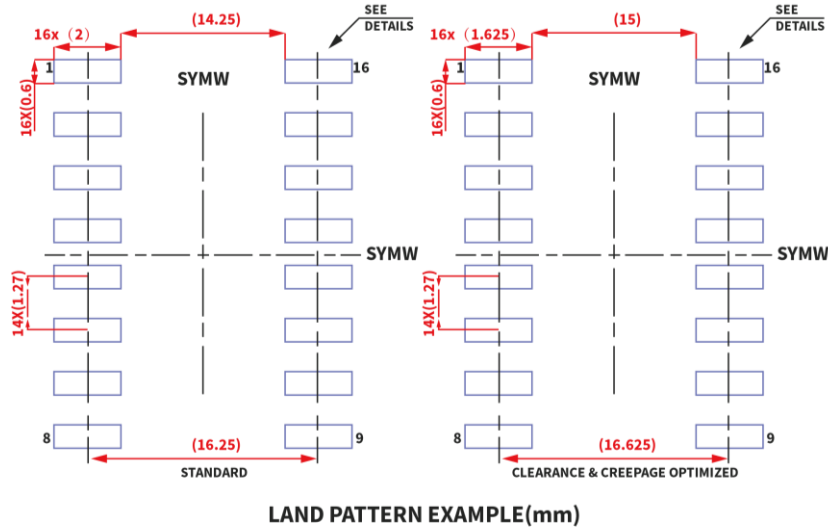


Figure 9.6 SOP16(600mil)/SOWW16 Package Board Layout Example

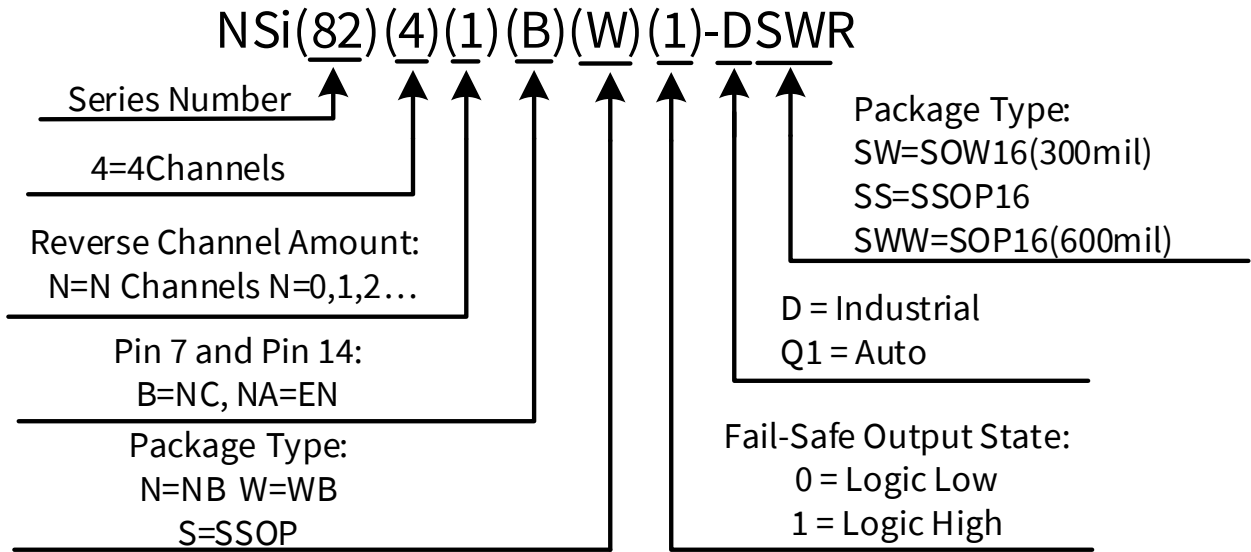
10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSi8240W0-Q1SWR	5	4	0	150	Low	-40 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8240W1-Q1SWR	5	4	0	150	High	-40 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8241W0-Q1SWR	5	3	1	150	Low	-40 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8241W1-Q1SWR	5	3	1	150	High	-40 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8242W0-Q1SWR	5	2	2	150	Low	-40 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8242W1-Q1SWR	5	2	2	150	High	-40 to 125 °C	2	SOP16 (300mil)	SOW16	1000
NSi8240S0-Q1SSR	3	4	0	150	Low	-40 to 125 °C	1	SSOP16	SSOP16	2500
NSi8240S1-Q1SSR	3	4	0	150	High	-40 to 125 °C	1	SSOP16	SSOP16	2500
NSi8241S0-Q1SSR	3	3	1	150	Low	-40 to 125 °C	1	SSOP16	SSOP16	2500
NSi8241S1-Q1SSR	3	3	1	150	High	-40 to 125 °C	1	SSOP16	SSOP16	2500
NSi8242S0-Q1SSR	3	2	2	150	Low	-40 to 125 °C	1	SSOP16	SSOP16	2500
NSi8242S1-Q1SSR	3	2	2	150	High	-40 to 125 °C	1	SSOP16	SSOP16	2500
NSi8240W0-Q1SWWR	8	4	0	150	Low	-55 to 125 °C	3	SOP16 (600mil)	SOWW16	1000
NSi8240W1-Q1SWWR	8	4	0	150	High	-55 to 125 °C	3	SOP16 (600mil)	SOWW16	1000
NSi8241W0-Q1SWWR	8	3	1	150	Low	-55 to 125 °C	3	SOP16 (600mil)	SOWW16	1000
NSi8241W1-Q1SWWR	8	3	1	150	High	-55 to 125 °C	3	SOP16 (600mil)	SOWW16	1000
NSi8242W0-Q1SWWR	8	2	2	150	Low	-55 to 125 °C	3	SOP16 (600mil)	SOWW16	1000
NSi8242W1-Q1SWWR	8	2	2	150	High	-55 to 125 °C	3	SOP16 (600mil)	SOWW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.  
All devices are AEC-Q100 qualified.



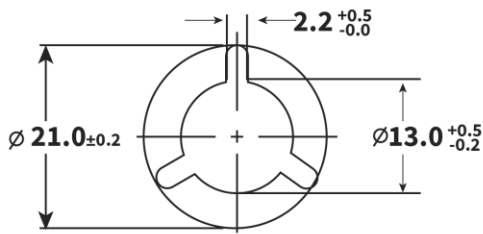
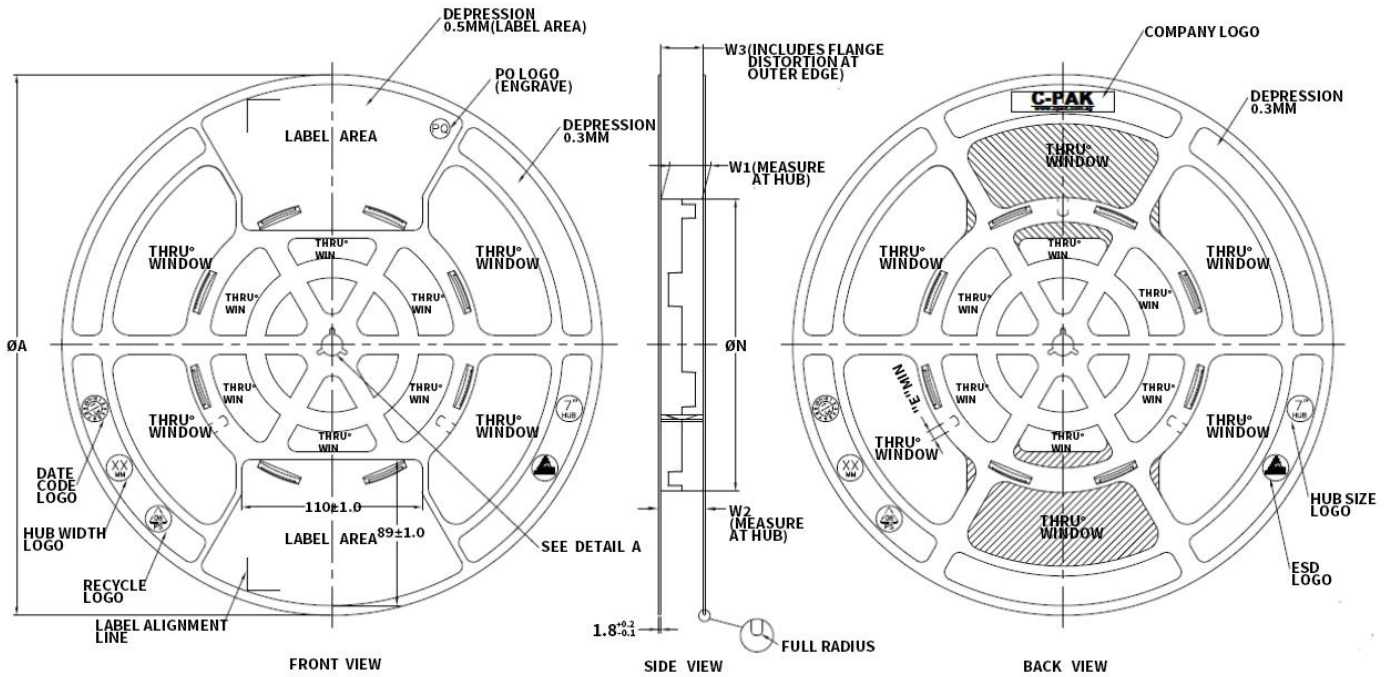
**Part Number Rule:**



**11. Documentation Support**

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolator selection guide</i>
NSi824x	tbd	tbd	tbd	tbd

### 12. Tape and Reel Information

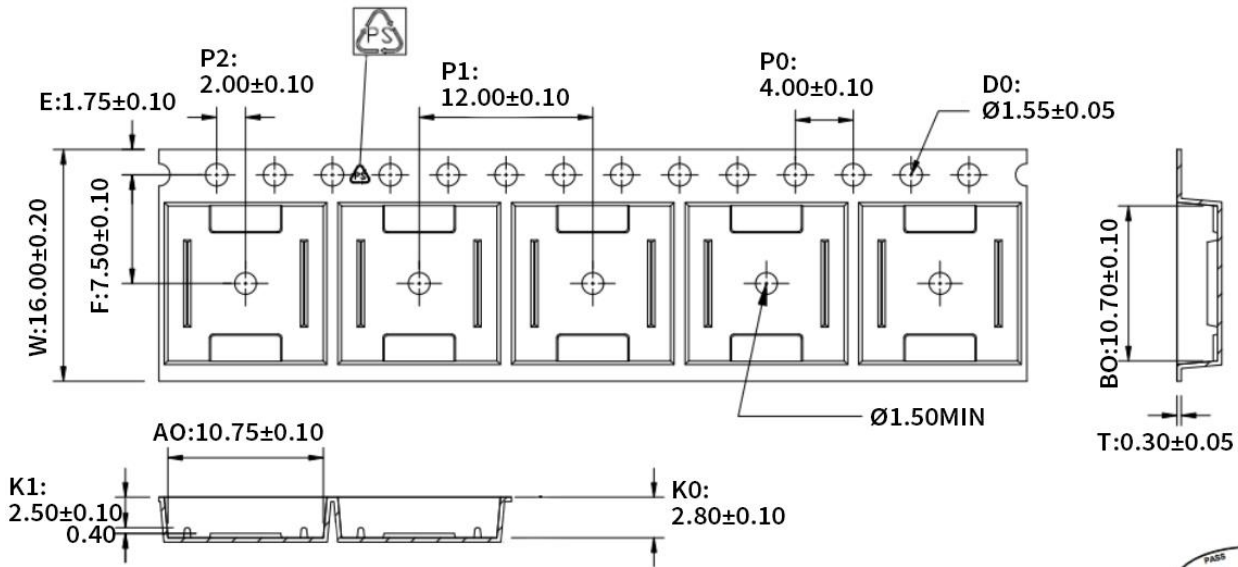


**ARBOR HOLE  
DETAIL A  
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	$\phi A \pm 2.0$	$\phi N \pm 2.0$	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4		5.5
16MM	330	178	16.4 <sup>+2.0</sup> <sub>-0.0</sub>	22.4		5.5
24MM	330	178	24.4 <sup>+2.0</sup> <sub>-0.0</sub>	30.4		5.5
32MM	330	178	32.4 <sup>+2.0</sup> <sub>-0.0</sub>	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 <sup>12</sup>	ANTISTATIC	ALL TYPES
B	10 <sup>6</sup> TO 10 <sup>11</sup>	STATIC DISSIPATIVE	BLACK ONLY
C	10 <sup>5</sup> & BELOW 10 <sup>5</sup>	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10 <sup>9</sup> TO 10 <sup>11</sup>	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness:  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122 )
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:  $10^5 \sim 10^{10} \Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

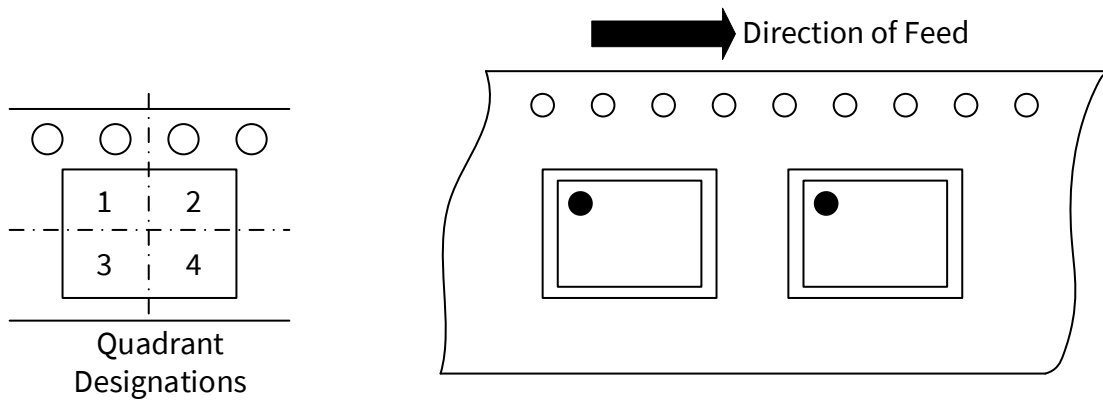


Figure 12.2 Tape Information of SOP16(300mil)

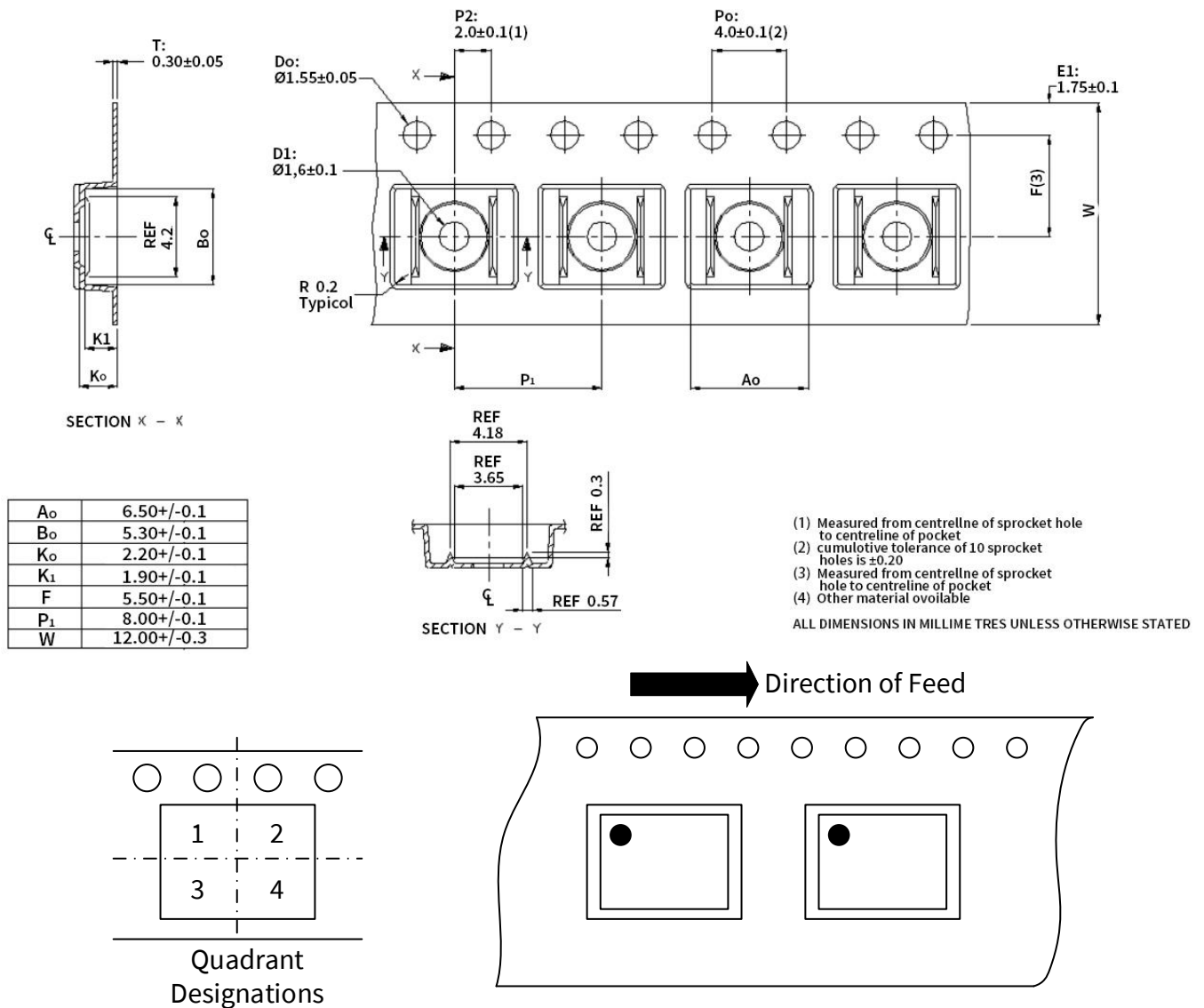
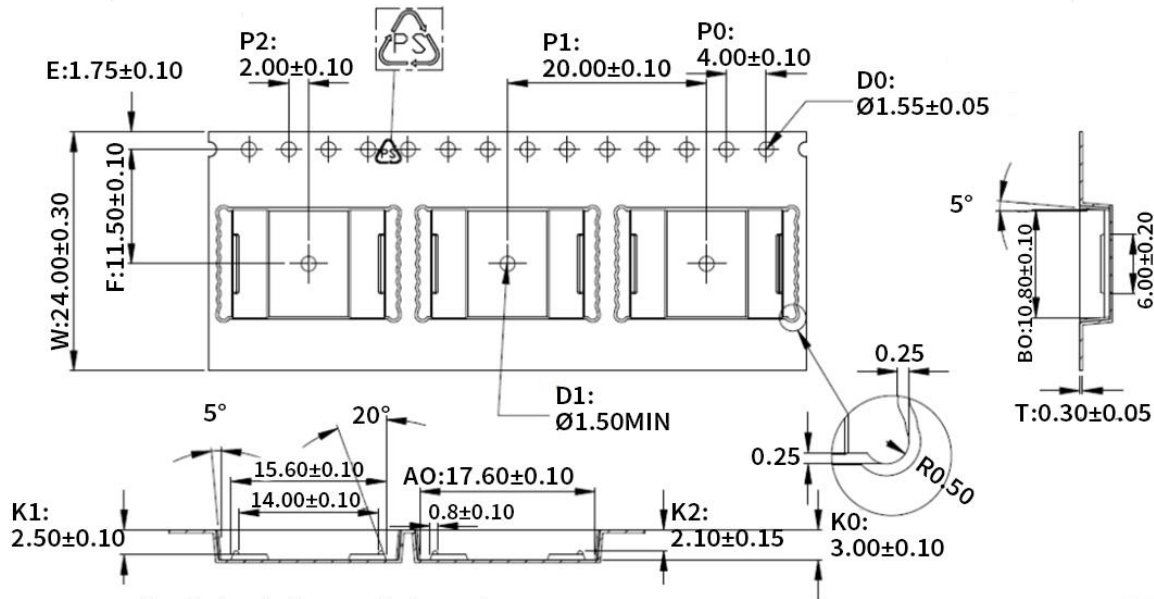


Figure 12.3 Tape Information of SSOP16



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness:  $0.30 \pm 0.05$ mm.
6. Packing length per 19" reel: 246.0 Meters. (Rewind 1:13)
7. Component load per 13" reel: 5000 pcs.
8. Surface resistivity:  $10^5 \sim 10^{10} \Omega/\square$

W	24.00±0.30
A0	17.60±0.10
B0	10.80±0.10
K0	3.00±0.10
K1	2.50±0.10

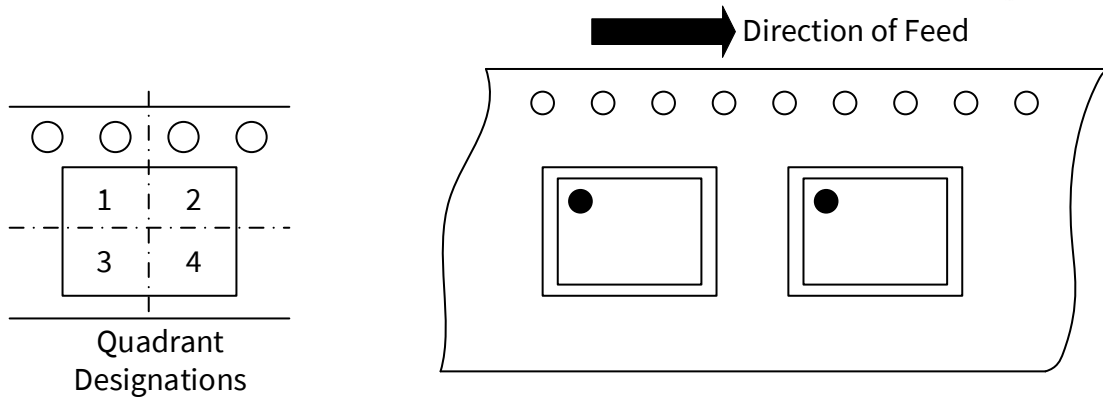


Figure 12.4 Tape Information of SOP16(600mil)

### 13. Revision History

Revision	Description	Date
1.0	Initial version	2021/7/16
1.1	Update Package Board Layout Example. Update Package information and Tape and Reel information.	2022/5/10
1.2	Delete "Isolation barrier life: >60 years". Change DTI to 28, Change Min Storage Temperature to -65, add Junction Temperature. Add SOWW16 package.	2022/8/26

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