

High Efficiency Thyristor

$$V_{RRM} = 1200 \text{ V}$$

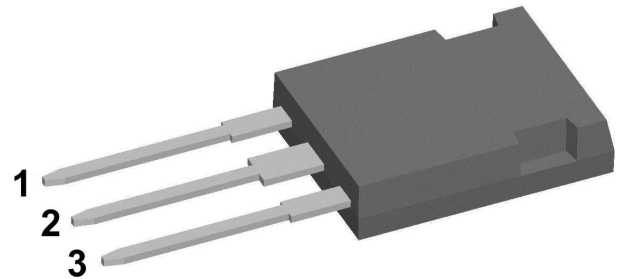
$$I_{TAV} = 80 \text{ A}$$

$$V_T = 1.38 \text{ V}$$

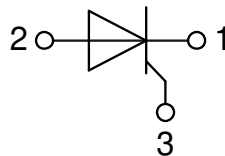
Single Thyristor

Part number

CLA80E1200HF



Backside: anode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: PLUS247

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Disclaimer Notice

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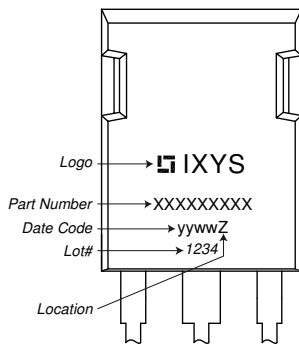


Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1200	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1200 V$	$T_{VJ} = 25^{\circ}C$		50	μA
		$V_{R/D} = 1200 V$	$T_{VJ} = 125^{\circ}C$		5	mA
V_T	forward voltage drop	$I_T = 80 A$	$T_{VJ} = 25^{\circ}C$		1.40	V
		$I_T = 160 A$			1.77	V
		$I_T = 80 A$	$T_{VJ} = 125^{\circ}C$		1.38	V
		$I_T = 160 A$			1.87	V
I_{TAV}	average forward current	$T_C = 115^{\circ}C$	$T_{VJ} = 150^{\circ}C$		80	A
$I_{T(RMS)}$	RMS forward current	180° sine			126	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.88	V
r_T	slope resistance				6.3	m Ω
R_{thJC}	thermal resistance junction to case				0.2	K/W
R_{thCH}	thermal resistance case to heatsink			0.3		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		620	W
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		900	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		970	A
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		765	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		825	A
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		4.05	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		3.92	kA ² s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		2.93	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		2.83	kA ² s
C_J	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		36	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			5	W
P_{GAV}	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C; f = 50 \text{ Hz}$ repetitive, $I_T = 240 A$			150	A/ μs
		$t_p = 200 \mu s; di_G/dt = 0.3 A/\mu s;$ $I_G = 0.3 A; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 80 A$			500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty; \text{ method 1 (linear voltage rise)}$	$T_{VJ} = 150^{\circ}C$		1000	V/ μs
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.5	V
			$T_{VJ} = -40^{\circ}C$		1.6	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		38	mA
			$T_{VJ} = -40^{\circ}C$		80	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				5	mA
I_L	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		150	mA
		$I_G = 0.3 A; di_G/dt = 0.3 A/\mu s$				
I_H	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		100	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0.3 A; di_G/dt = 0.3 A/\mu s$				
t_q	turn-off time	$V_R = 100 V; I_T = 80 A; V = \frac{2}{3} V_{DRM}$ $di/dt = 20 A/\mu s \quad dv/dt = 20 V/\mu s \quad t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		150	μs



Package PLUS247		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			70	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		150	°C
Weight				6		g
F_C	mounting force with clip		20		120	N
$d_{Spp/App}$	creepage distance on surface / striking distance through air	terminal to terminal	5.5			mm
$d_{Spb/Apb}$		terminal to backside	5.5			mm

Product Marking



Part description

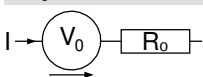
- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- A = (up to 1200V)
- 80 = Current Rating [A]
- E = Single Thyristor
- 1200 = Reverse Voltage [V]
- HF = PLUS247 (3)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA80E1200HF	CLA80E1200HF	Tube	30	508680

Equivalent Circuits for Simulation

** on die level*

$T_{VJ} = 150^{\circ}C$

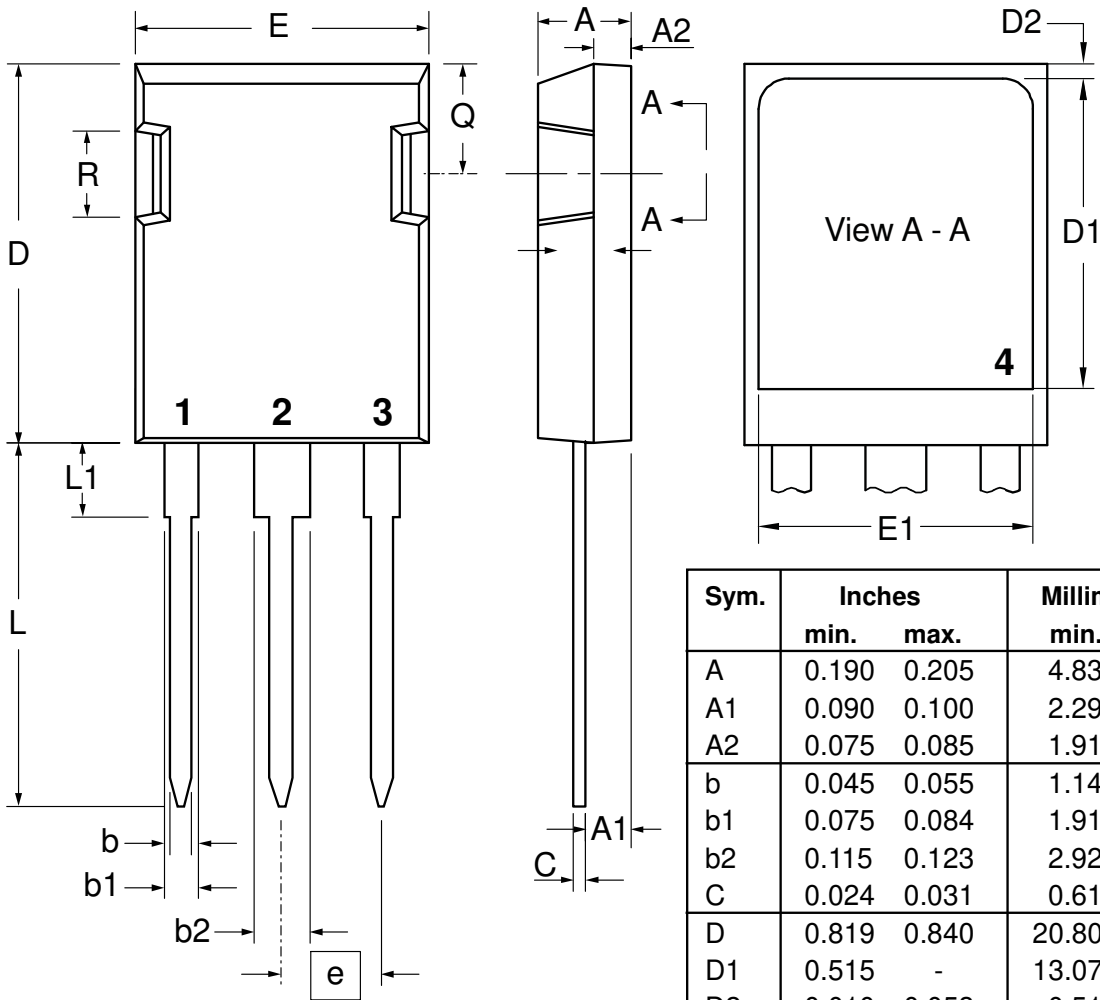


Thyristor

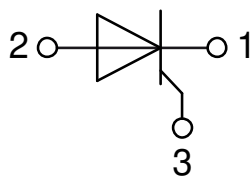
$V_{0\ max}$	threshold voltage	0.88	V
$R_{0\ max}$	slope resistance *	3.8	mΩ



Outlines PLUS247



Sym.	Inches		Millimeter	
	min.	max.	min.	max.
A	0.190	0.205	4.83	5.21
A1	0.090	0.100	2.29	2.54
A2	0.075	0.085	1.91	2.16
b	0.045	0.055	1.14	1.40
b1	0.075	0.084	1.91	2.13
b2	0.115	0.123	2.92	3.12
C	0.024	0.031	0.61	0.80
D	0.819	0.840	20.80	21.34
D1	0.515	-	13.07	-
D2	0.010	0.053	0.51	1.35
E	0.620	0.635	15.75	16.13
E1	0.530	-	13.45	-
e	0.215 BSC		5.45 BSC	
L	0.780	0.800	19.81	20.32
L1	0.150	0.170	3.81	4.32
Q	0.220	0.244	5.59	6.20
R	0.170	0.190	4.32	4.83



Thyristor

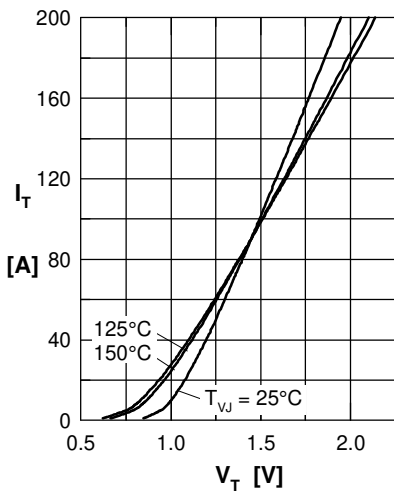


Fig. 1 Forward characteristics

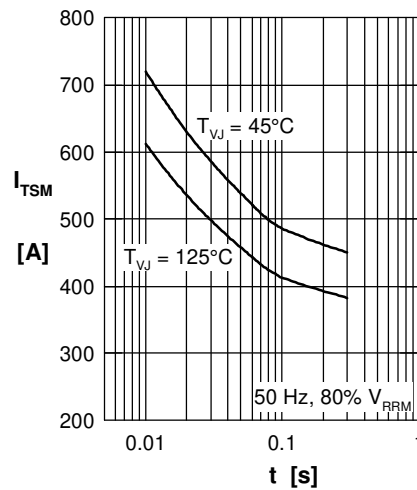


Fig. 2 Surge overload current

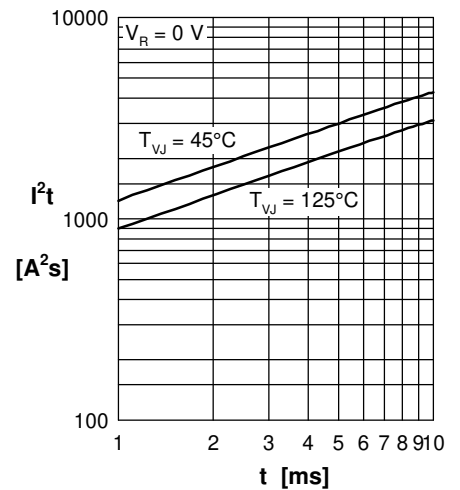


Fig. 3 I^2t versus time (1-10 ms)

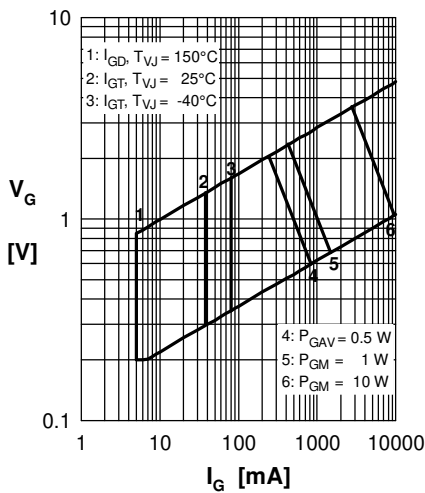


Fig. 4 Gate trigger characteristics

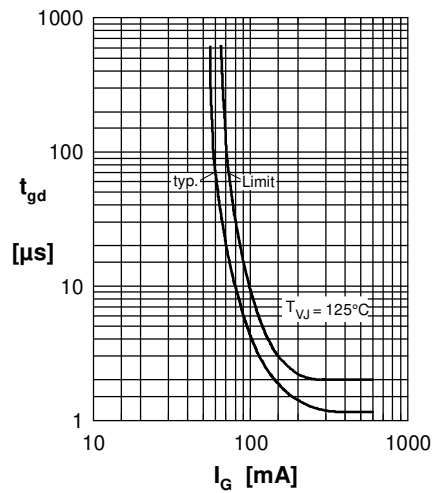


Fig. 5 Gate controlled delay time

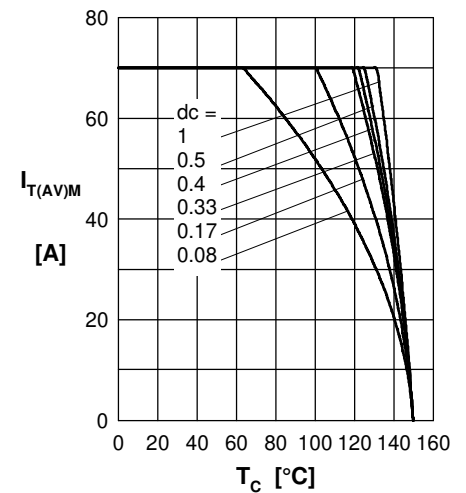


Fig. 6 Max. forward current at case temperature

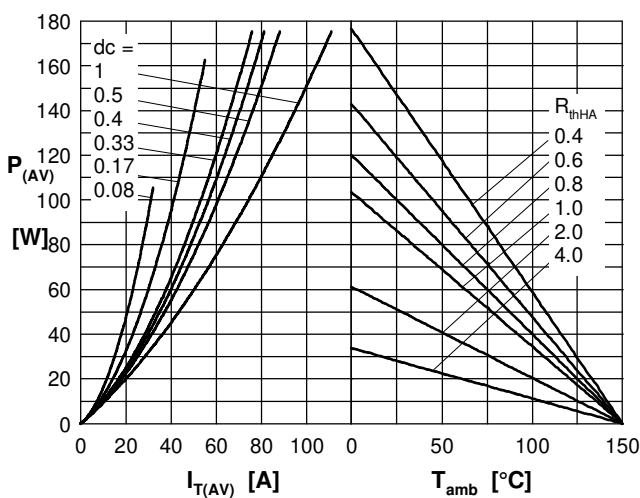


Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature

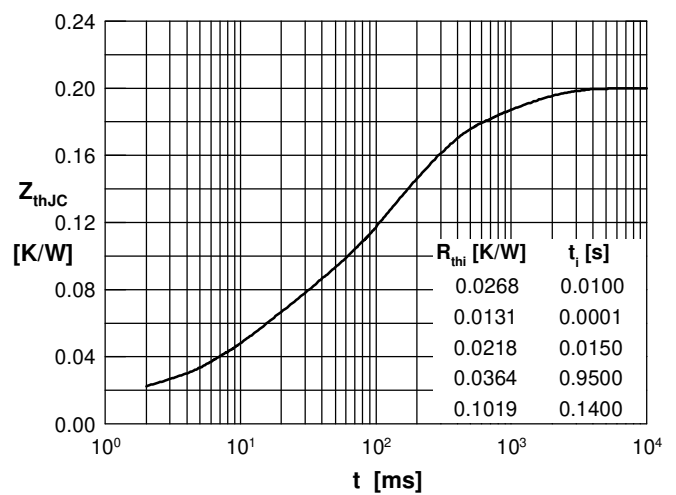


Fig. 8 Transient thermal impedance