

MT29F32G08ABAAAWP-ITZ

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Data Sheet

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Orderable Part Information

Status	Production	Alternative Part	N/A
FBGA Code	N/A	SPD Data	N/A
MBQual Data	N/A	Shipping Media	N/A

Specs

Density	32Gb	Status	Production
RoHS	Yes	Width	x8
Voltage	3.3V	Package	TSOP
Pin Count	48-pin	MT/s	
I/O	Common		

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FAQs

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Date	What was added
03/2014	Datasheet: 32/64/128/256Gb Async/Sync NAND (M73A)
09/2013	IBIS: NAND 32/64/128/256Gb SLC (RevA) M73A

FAQs

- » Do you support small block devices?
- » How much ECC do I need to support your devices?
- » I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bit/byte errors in data I read back from the NAND device.
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Title & Description	Secure	ID	Updated
HSpice: NAND 32/64/128/256Gb SLC (Rev A) M73A: Rev.2.0		M73A	09/2010
IBIS: NAND 32/64/128/256Gb SLC (Rev A) M73A: Rev.2.1		M73A	09/2013

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- [+](#) Do you support small block devices?
- [+](#) How much ECC do I need to support your devices?
- [+](#) I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bit/byte errors in data I read back from the NAND device.

- [+](#) How do I achieve greater PROGRAM/READ throughput for the NAND device?
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- [+](#) What is the impedance tolerance of the driver in match-impedance mode relative to the expected value base on the perfect reference resistor connected to ZQ pin?
- [+](#) Does thermal information change for IT parts?
- [+](#) My design was based on a specification stating the JTAG was relative to VDD (1.8V), but now we've discovered that JTAG is actually relative to VDDQ (1.5V). It's a fairly significant board spin to change this; what do I risk by leaving the design as-is? I assume that the specification is still for VDDQ + 0.3V = 1.8V, but with CMOS parts there's no way I can guarantee that it won't swing past that on transitions.
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