2N6193

PNP Silicon Switching Transistor

Rev. V3

Features

- JAN, JANTX, JANTXV, JANS, and JANSR 100K rads (si) per MIL-PRF-19500/561
- TO-39 (TO-205AD) Package

Electrical Characteristics (T_A = +25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Collector - Emitter Breakdown Voltage	I_C = -50 mA dc	$V_{(BR)CEO}$	V dc	-100	—
Collector - Emitter Cutoff Current	V_{CE} = -100 V dc	I_{CEO}	µA dc	—	-100
Collector - Emitter Cutoff Current	V_{BE} = +1.5 V dc; V_{CE} = -90 V dc	I_{CEX1}	µA dc		-10
Collector - Base Cutoff Current	V_{CB} = -100 V dc	I_{CBO}	µA dc	—	-10
Emitter - Base Cutoff Current	V_{EB} = -6.0 V dc	I_{EBO}	µA dc	—	-100
Forward Current Transfer Ratio	V_{CE} = -2.0 V dc; I_C = -0.5 A dc V_{CE} = -2.0 V dc; I_C = -2.0 A dc V_{CE} = -2.0 V dc; I_C = -5.0 A dc	h_{FE}	-	60 60 40	240
Collector - Emitter Saturation Voltage	I_C = -2.0 A dc, I_B = -0.2 A dc I_C = -5.0 A dc, I_B = -0.5 A dc	$V_{CE(SAT)1}$ $V_{CE(SAT)2}$	V dc	—	-0.7 -1.2
Emitter - Base Saturation Voltage	I_C = -2.0 A dc, I_B = -0.2 A dc I_C = -5.0 A dc, I_B = -0.5 A dc	$V_{BE(SAT)1}$ $V_{BE(SAT)1}$	V dc	—	-1.2 -1.8
Collector - Emitter Cutoff Current	T_A = +150°C V_{CE} = -90 V dc; V_{BE} = +1.5 V dc	I_{CEX2}	µA dc		-15
Forward - Current Transfer Ratio	T_A = -55°C V_{CE} = -2.0 V dc; I_C = -2.0 A dc	h_{FE4}		12	
Dynamic Characteristics					
Small-Signal Short-Circuit Forward - Current Transfer Ratio	V_{CE} = -10 V dc; I_C = -0.5 A dc; f = 10 MHz	$\lvert h_{fe} \rvert$	-	3	15
Output Capacitance	V_{CB} = -10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}	pF	—	300
Input Capacitance	V_{BE} = -2.0 Vdc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}	pF	—	1250
Switching Characteristics					
Delay Time	See figure 11 of MIL-PRF-19500/561	t_d	ns	—	100
Rise Time	See figure 11 of MIL-PRF-19500/561	t_r	ns	—	100
Storage Time	See figure 12 of MIL-PRF-19500/561	t_s	µs	—	2.0
Fall Time	See figure 12 of MIL-PRF-19500/561	t_f	ns	—	200

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Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)

Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	-100 V dc
Collector - Base Voltage	V_{CBO}	-100 V dc
Emitter - Base Voltage	V_{EBO}	-6.0 V dc
Base Current	I_B	-1.0 A dc
Collector Current	I_C	-5.0 A dc
Total Power Dissipation @ T_A = +25°C (1) @ T_C = +25°C (2)	P_T	1.0 W 17.5 W
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to +200°C

(1) See figure 6 of MIL-PRF-19500/561
(2) See figure 7 and 8 of MIL-PRF-19500/561

Thermal Characteristics

Characteristics	Symbol	Max. Value
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	175°C/W

Safe Operating Area	
DC Tests:	T_C = +25°C; I Cycle; t ≥ 0.5 s
Test 1:	V_{CE} = -2.0 V dc; I_C = -5.0 A dc
Test 2:	V_{CE} = -90 V dc; I_C = -55 mA dc

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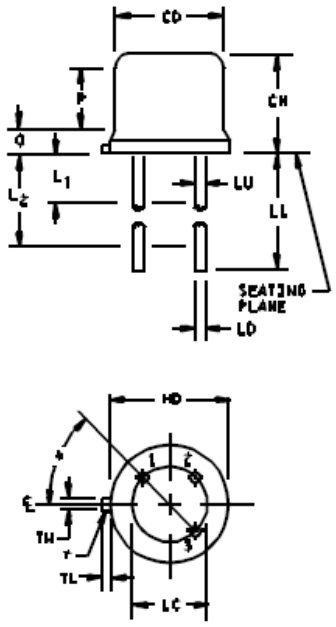
Outline Drawing (TO-39)

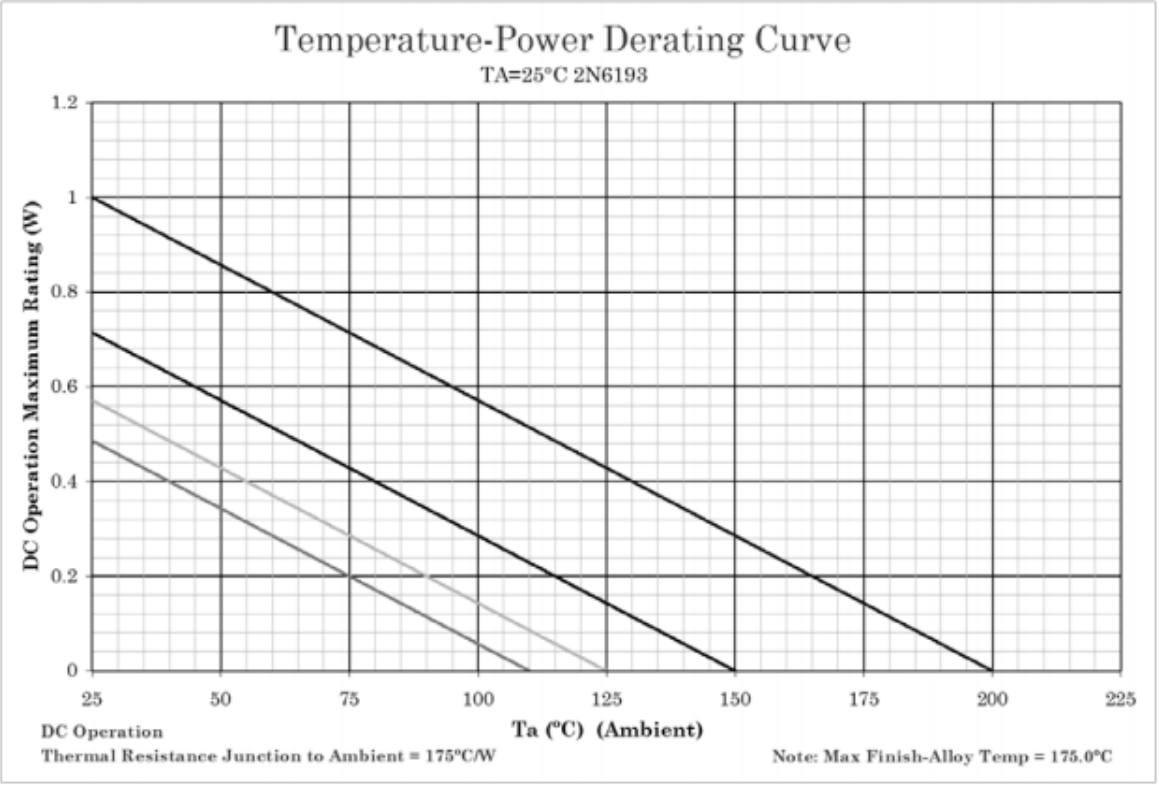


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.355	7.75	9.02	
CH	.240	.260	6.10	6.60	
HD	.355	.370	9.02	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7
LL	.500	.750	12.70	19.05	7
LU	.016	.019	0.41	0.48	7
L1		.050		1.27	7
L2	.250		6.35		7
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	10
P	.100		2.54		5
Q		.040		1.02	4
R		.010		0.25	11
α	45° TP		45° TP		6
Notes	1, 2, 8, 9				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum.
8. Lead designation, depending on device type, shall be as follows: 1 Emitter, 2 Base, and 3 Collector
9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

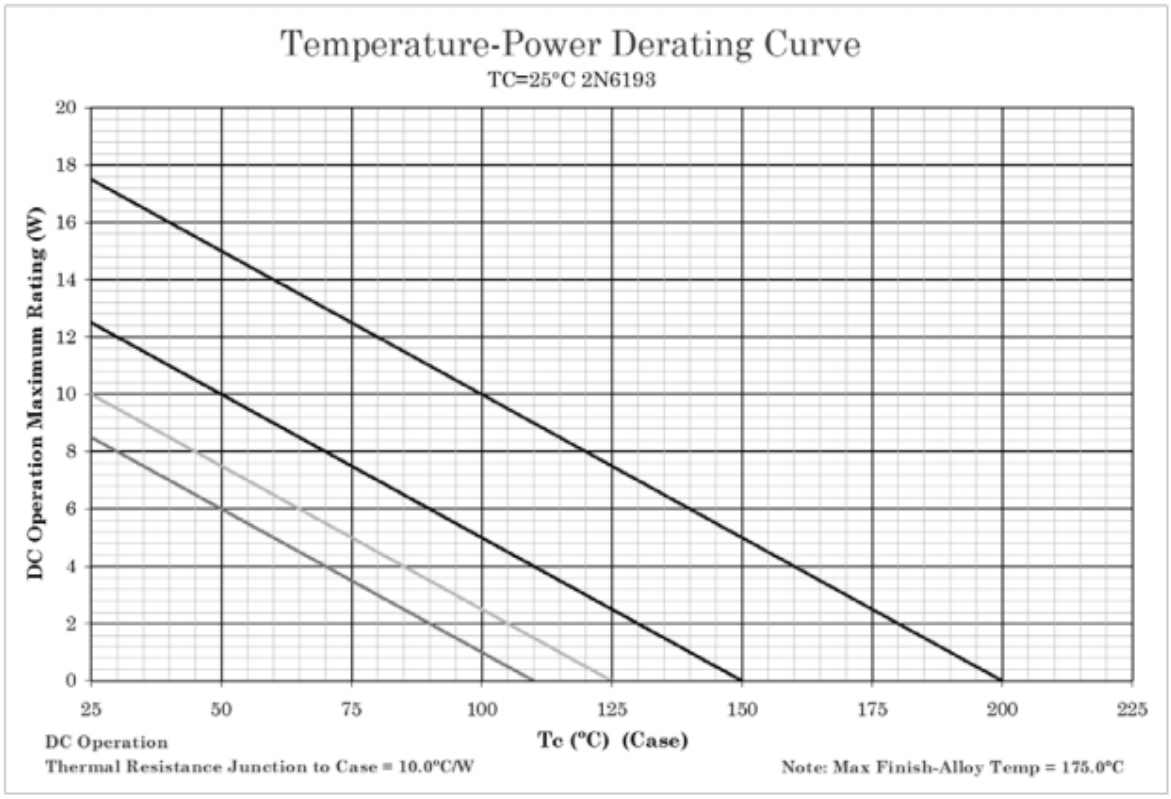
FIGURE 1. Physical dimensions (TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

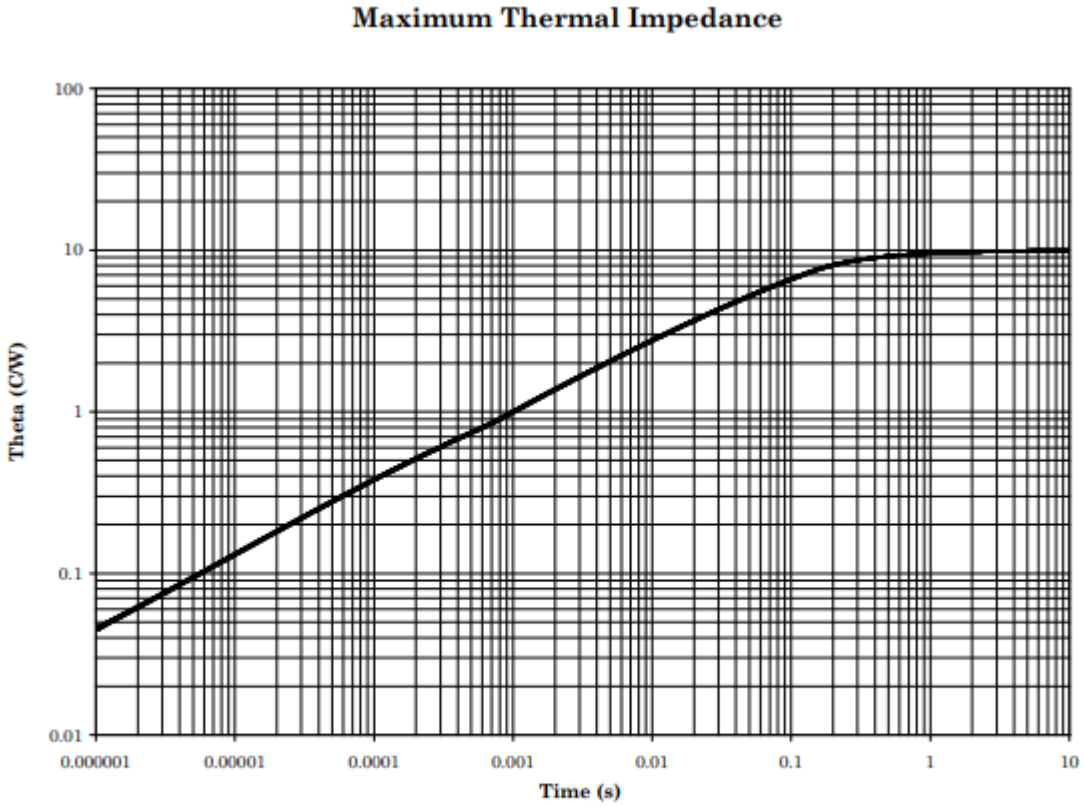
FIGURE 6. Temperature-power derating for 2N6193 $R_{\theta JA}$ (TO-39 Kovar).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Temperature-power derating for 2N6193 $R_{\theta JC}$ (TO-39 Kovar).



T_C = 25°C, thermal resistance $R_{\theta JC}$ = 10°C/W.

FIGURE 9. Thermal impedance graph ($R_{\theta JC}$) for 2N6193 (TO-39 Kovar).