# Three-Phase Sensorless Fan Driver IC

## FEATURES AND BENEFITS

- AEC-Q100 qualified
- Speed curve configuration via EEPROM
- $I^2C$ serial port
- Sinusoidal modulation for reduced audible noise and low vibration
- Sensorless (no Hall sensors required)
- Low $R_{DS(ON)}$ power MOSFETs
- 3.3 V / 20 mA linear regulator
- PWM or analog speed input
- FG speed output
- Slew rate control
- Lock detection
- Soft start
- Low power standby mode
- Overcurrent protection
- Overvoltage protection

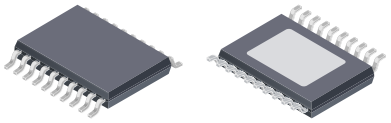
## DESCRIPTION

The A5947-B three phase motor driver IC incorporates sensorless sinusoidal drive to minimize vibration for a wide variety of fan applications. Sensorless control eliminates the requirement for Hall sensors.

A flexible closed-loop speed control system is integrated into the IC. EEPROM is used to tailor the common functions of the fan speed curve to a specific application. This eliminates the requirement for a microprocessor-based system and minimizes programming requirements.

The A5947-B is available in a 20-lead TSSOP with exposed thermal pad (suffix LP).

## PACKAGE:



*Not to scale*

20-lead TSSOP
with exposed thermal pad
(LP package)

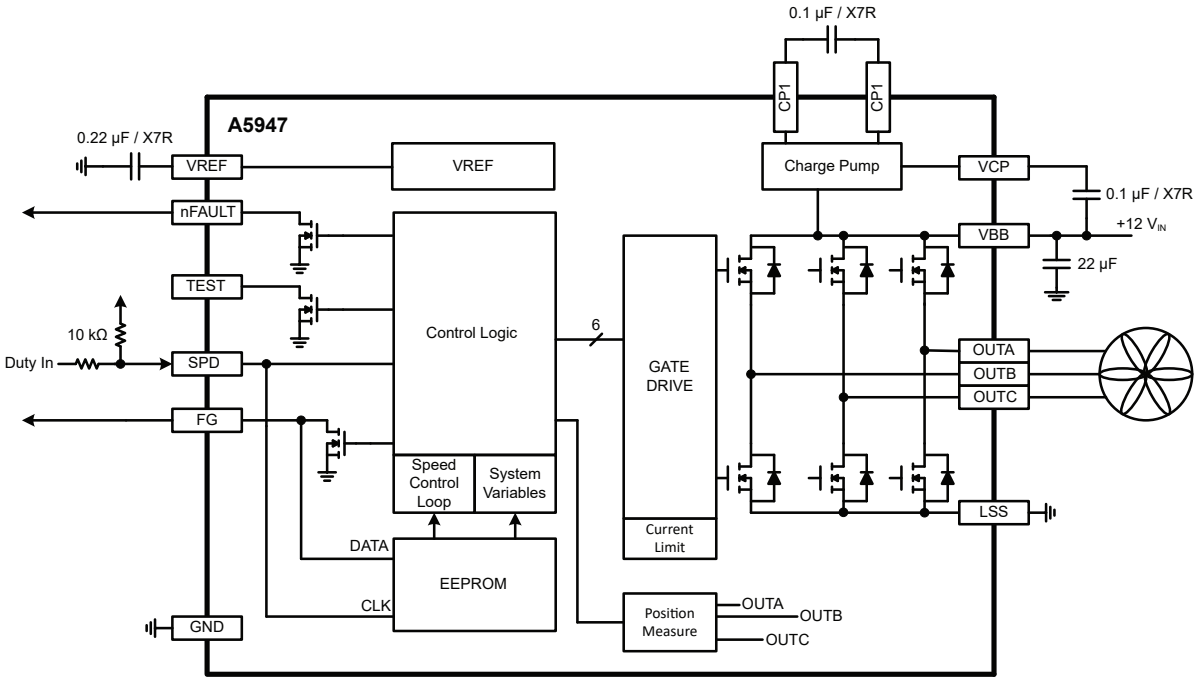



**Figure 1: Typical Application**

## SELECTION GUIDE

| Part Number | Operating Temperature Range ($T_A$) (°C) | Packaging | Packing |
|---|---|---|---|
| A5947KLPTR-B-T | –40 to 125 | 20-lead TSSOP with exposed power pad | 4000 pieces per 13-inch reel |

## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{BB}$ | | –0.7 to 40 | V |
| Logic Input Voltage Range | $V_{IN}$ | SPD | –0.3 to 6 | V |
| Logic Output | $V_O$ | FG, nFAULT, TEST | –0.3 to 6 | V |
| Output Current | $I_{OUT}$ | | 3.6 | A |
| Output Voltage | $V_{OUT}$ | OUTA, OUTB, OUTC | $V_{BB}$ + 1 | V |
| VCP | $V_{CP}$ | | $V_{BB}$ – 0.3 to $V_{BB}$ + 8 | V |
| CP1 | $V_{CP1}$ | | –0.3 to $V_{BB}$ + 0.3 | V |
| CP2 | $V_{CP2}$ | | $V_{BB}$ – 0.3 to $V_{CP}$ + 0.3 | V |
| Maximum EEPROM write cycles | $EEPROM_{W(MAX)}$ | | 1000 | cycles |
| Junction Temperature | $T_J$ | | 150 | °C |
| Storage Temperature Range | $T_{stg}$ | | –55 to 150 | °C |
| Operating Temperature Range | $T_A$ | Range K | –40 to 125 | °C |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Test Conditions* | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | 20-lead TSSOP (package LP), on 2-sided PCB 1-in.$^2$ copper | 34 | °C/W |

*Additional thermal information available on the Allegro website.

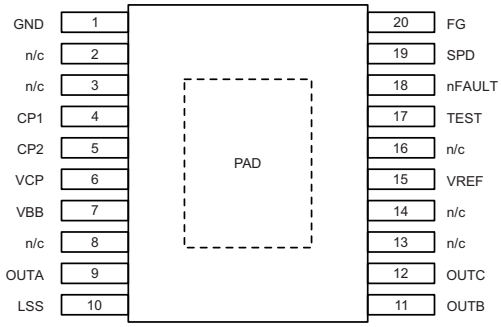
## Table of Contents





Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## PINOUT DIAGRAM AND TERMINAL LIST TABLE




**LP Package Pinouts**

### Terminal List Table

| Terminal Number LP Package | Name | Function |
|---|---|---|
| 1 | GND | Ground |
| 2,3 | n/c | No connect |
| 4 | CP1 | Charge pump capacitor |
| 5 | CP2 | Charge pump capacitor |
| 6 | VCP | Charge pump capacitor |
| 7 | VBB | Input supply |
| 8 | n/c | No connect |
| 9 | OUTA | Motor terminal |
| 10 | LSS | Low side source connection |
| 11 | OUTB | Motor terminal |
| 12 | OUTC | Motor terminal |
| 13,14 | n/c | No connect |
| 15 | VREF | Reference voltage output |
| 16 | n/c | No connect |
| 17 | TEST | Logic output signal |
| 18 | nFAULT | Logic output signal |
| 19 | SPD | Logic input – speed demand |
| 20 | FG | Logic output signal |
| – | PAD | Exposed pad for enhanced thermal dissipation |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**ELECTRICAL CHARACTERISTICS [1]:** Valid for $T_A$ = –40°C to 125°C; $V_{BB}$ = 4 to 40 V, unless noted otherwise

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| VBB Supply Current | $I_{BB}$ | Active mode (PWM duty < DC_ON) | – | 13.5 | 15 | mA |
| | $I_{BBS}$ | $V_{BB}$ = 34 V, standby mode | – | 10 | 40 | µA |
| Reference Voltage | $V_{REF}$ | I = 0 to 20 mA, $V_{BB}$ = 6 to 40 V | 3.15 | 3.3 | 3.45 | V |
| Charge Pump | $V_{CP}$ | Relative to $V_{BB}$, $V_{BB}$ = 8 V | 6.5 | 7.2 | 7.7 | V |
| | | Relative to $V_{BB}$, $V_{BB}$ = 4 V | 3.5 | 3.7 | – | V |
| **POWER DRIVER** | | | | | | |
| Total Driver On-Resistance (Sink + Source) | $R_{DS(ON)}$ | I = 1.5 A, $T_J$ = 25°C, $V_{BB}$ = 12 V | – | 510 | – | mΩ |
| | | I = 1.5 A, $T_J$ = 125°C, $V_{BB}$ = 12 V | – | 760 | 860 | mΩ |
| | | I = 1.5 A, $T_J$ = 25°C, $V_{BB}$ = 4 V | – | 680 | – | mΩ |
| | | I = 1.5 A, $T_J$ = 125°C, $V_{BB}$ = 4 V | – | 950 | 1200 | mΩ |
| Source Driver On-Resistance | $R_{DS(ON)SRC}$ | $T_J$ = 125°C, $V_{BB}$ = 12 V | – | 380 | – | mΩ |
| Sink Driver On-Resistance | $R_{DS(ON)SNK}$ | $T_J$ = 125°C, $V_{BB}$ = 12 V | – | 380 | – | mΩ |
| Motor PWM Frequency | $f_{PWM}$ | $T_A$ = 25°C to 125°C | 23.52 | 24.5 | 25.48 | kHz |
| | | $T_A$ = –40°C to 125°C | 23.03 | – | 25.97 | kHz |
| **SPEED CONTROL** | | | | | | |
| PWM Input Frequency Range | $f_{PWMIN}$ | | 34 | – | 65000 | Hz |
| Duty Cycle On Threshold | $DC_{ON}$ | Relative to target | –0.5 | – | 0.5 | % |
| Duty Cycle Off Threshold | $DC_{OFF}$ | Relative to target | –0.5 | – | 0.5 | % |
| SPD Standby Threshold (Analog) | $V_{SPDTH}$ | | 0.43 | 0.7 | 1 | V |
| SPD On Threshold | $V_{SPDON}$ | $DC_{ON}$ = 10% | 210 | 240 | 270 | mV |
| SPD Off Threshold | $V_{SPDOFF}$ | $DC_{OFF}$ = 8% | 160 | 190 | 220 | mV |
| SPD Max | $V_{SPDMAX}$ | | – | 2.49 | – | V |
| SPD ADC Resolution | $V_{SPDLSB}$ | | – | 4.892 | – | mV |
| SPD ADC Accuracy | $SPD_{ACC}$ | $V_{BB}$ = 12 V, $V_{SPD}$ = 0.2 V to $V_{SPDMAX}$ | –10 | – | 10 | LSB |
| Speed Setpoint | $f_{SPD}$ | Duty cycle input; $T_A$ = 25°C to 125°C | –5 | – | 5 | % |
| | | Duty cycle input; $T_A$ = –40°C to 125°C | –7 | – | 7 | % |

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

*Continued on next page...*



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**ELECTRICAL CHARACTERISTICS [1] (continued):** Valid for $T_A$ = –40°C to 125°C; $V_{BB}$ = 4 to 40 V, unless noted otherwise

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PROTECTION CIRCUITS** | | | | | | |
| Lock Timing | $t_{LOCK}$ | Relative to target | –5 | – | 5 | % |
| VBB Undervoltage Threshold | $V_{BBUVLO}$ | UVLO = 0, $V_{BB}$ rising | 3.7 | 3.85 | 4 | V |
| | | UVLO = 1, $V_{BB}$ rising | 8.4 | 8.65 | 9.02 | V |
| VBB Undervoltage Hysteresis | $V_{BBHYS}$ | UVLO = 0 | 160 | 300 | 480 | mV |
| | | UVLO = 1 | 1.8 | 2 | 2.2 | V |
| Overcurrent Limit | $I_{OCL}$ | $V_{BB}$ = 8 V | 2.5 | 3 | 3.5 | A |
| Overcurrent Protection | $I_{OCP}$ | | 3.94 | 7 | – | A |
| VBB Overvoltage | $V_{BBOV}$ | VBBOV = 0, $V_{BB}$ rising | 18.2 | 19 | 19.8 | V |
| | | VBBOV = 1, $V_{BB}$ rising | 36.8 | 37.5 | 39.3 | V |
| VBB Overvoltage Hystersis | $V_{BBOVHYS}$ | | 1.5 | 2 | 2.5 | V |
| VREF UVLO | $V_{REFUVLO}$ | $V_{REF}$ rising | 2.9 | 3 | 3.15 | V |
| VREF UVLO Hystersis | $V_{REFHYS}$ | | 150 | 250 | 350 | mV |
| VREF Overcurrent Limit | $V_{REFOCL}$ | $V_{BB}$ = 12 V | 30 | 65 | 120 | mA |
| VCP UVLO | $V_{CPUVLO}$ | $V_{CP}$ rising | 2.5 | 2.75 | 3.0 | V |
| VCP UVLO HYS | $V_{CPUVLOHYS}$ | | – | 110 | – | mV |
| Thermal Shutdown Temperature | $T_{JTSD}$ | Temperature increasing | 150 | 165 | 180 | °C |
| Thermal Shutdown Hysteresis | $\Delta T_J$ | Recovery = $T_{JTSD} - \Delta T_J$ | – | 20 | – | °C |
| **LOGIC/INPUT OUTPUT/I²C** | | | | | | |
| Logic Input Current (SPD, FG) | $I_{IN}$ | $V_{IN}$ = 0 to 5.5 V | –5 | <1 | 5 | µA |
| Logic Input Low Level | $V_{IL}$ | | 0 | – | 0.8 | V |
| Logic Input High Level | $V_{IH}$ | | 2 | – | 5.5 | V |
| Logic Input Hysteresis | $V_{HYS}$ | | 200 | 300 | 600 | mV |
| Output Saturation Voltage (FG, RD) | $V_{SAT}$ | I = 5 mA | – | – | 0.3 | V |
| Output Leakage | $I_{OUT}$ | V = 5.5 V, switch OFF | – | – | 5 | µA |
| **I²C TIMING** | | | | | | |
| SCL Clock Frequency | $f_{CLK}$ | | 3 | – | 400 | kHz |
| Bus Free-Time Between Stop/Start | $t_{BUF}$ | | 1.3 | – | – | µs |
| Hold Time Start Condition | $t_{HD:STA}$ | | 0.6 | – | – | µs |
| Setup Time for Start Condition | $t_{SU:STA}$ | | 0.6 | – | – | µs |
| SCL Low Time | $t_{LOW}$ | | 1.3 | – | – | µs |
| SCL High Time | $t_{HIGH}$ | | 0.6 | – | – | µs |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | – | – | ns |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | – | 900 | ns |
| Setup Time for Stop Condition | $t_{SU:STO}$ | | 0.6 | – | – | µs |

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## FUNCTIONAL DESCRIPTION

### Basic Operation

The A5947 targets fan applications to meet the objectives of minimal vibration, high efficiency, and the ability to customize the IC to the speed control specification.

In typical systems, an MCU is required to meet each application specification. The A5947 integrates the basic closed-loop speed control function, thus allowing elimination of the cost, PCB space, and programming requirements of a custom MCU.

For each specific application, the EEPROM settings can be created with the Allegro EVB and software.

The speed of the fan is typically controlled by variable duty cycle PWM input. The duty cycle is measured and converted to a 9-bit number. This 9-bit "demand" is translated to a PWM duty cycle applied to the motor windings, effectively a percentage of the power supply voltage.

Protection features include lock detection with restart, overcurrent limit, overvoltage protection, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

Standby mode can be achieved by holding SPD pin low for longer than the programmed lock off-time.

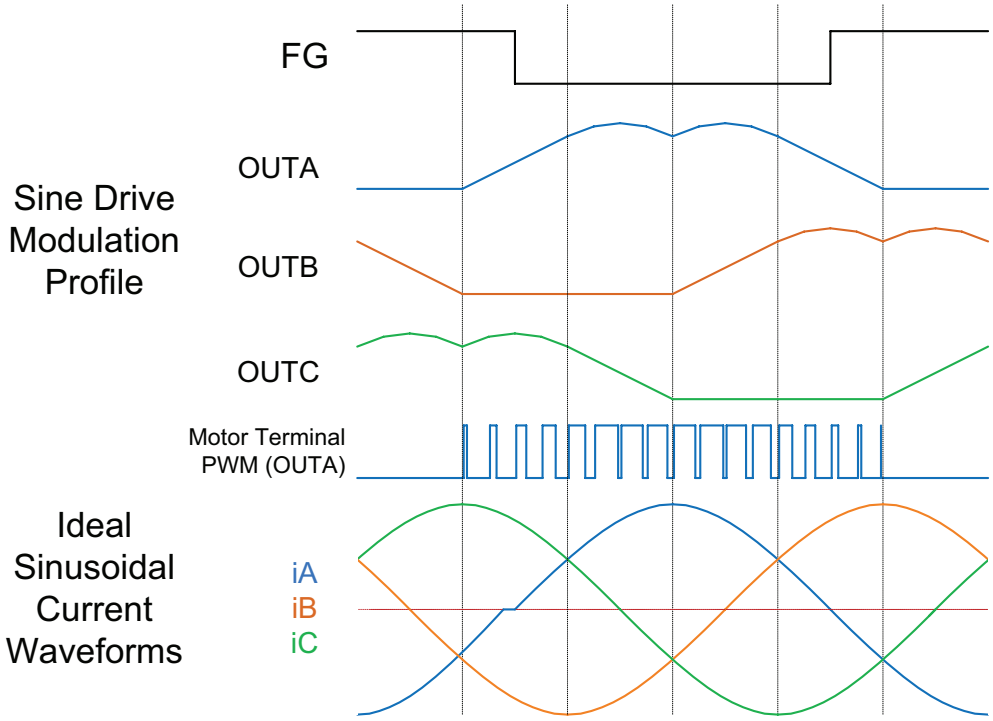



**Figure 2: Sinusoidal Drive Sequence**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**FG.** Open-drain output, represents the speed of the motor for normal operation. The electrical frequency of the motor may be different than FG output.

$$f_{ELEC} = f_{FGOUT} \times NumberOfPolePairs / 2$$
$$f_{FGOUT} = f_{ELEC} \times 2 / NumberOfPolePairs$$
$$RPM = f_{ELEC} \times 60 / NumberOfPolePairs$$
$$RPM = 30 \times f_{FGOUT}$$

Additionally, the FG pin serves as the data line, (SDA) for I²C communication.

**SPD.** Speed demand input. The demand can be in the form of duty cycle, analog voltage, or direct I²C command.

An EEPROM setting will determine choice of duty or analog input. Additionally, the SPD pin serves as the clock line (SCL) for I²C communication.

*Analog control.* Voltage applied to SPD pin will set speed demand. An internal 9-bit A/D converter will translate the input to a speed demand.

$$Applied\ Duty\ (\%) = Code / 511$$
$$Code = V_{IN(SPD)} / 4.89\ mV + 2 \text{ where code} = [0 \ldots 511]$$

**TEST.** Open drain output, low when motor off, high at end of open loop startup.

**nFAULT.** An active low output to represent the following fault conditions: VBB undervoltage, VBB overvoltage, thermal shutdown, VCP undervoltage, rotor lock, and output VDS fault (OCP).

**OCL.** Overcurrent limit. When the OCL level is reached, the PWM on pulses will be terminated early to prevent further increase of current.

**SLEW.** The motor output slew rate (dv/dt) can be reduced by adjustment of EEPROM variable SLEW.

| SLEW | | Nominal (ns) |
|---|---|---|
| MSB | LSB | |
| 0 | 0 | 100 |
| 0 | 1 | 150 |

**OCP.** Overcurrent protection, VDS monitor. To protect from short-to-ground, shorted load, or short-to-battery conditions for the motor lines, the voltage across the power outputs is monitored at all times when the MOSFET is turned on. There will be a short blank time before the motor outputs are disabled if the overcurrent protection limit $I_{OCP}$ is exceeded. The fault is latched off. EEPROM bit OCPOPT will select option to reset latch with choice of lock timeout or PWM on/off command.

Note: During the shorted event, the absolute maximum ratings may be exceeded for the blank time.

**OVP.** The A5947 outputs can be disabled if power supply voltage exceeds programmed threshold. With OVPOPT = 1, the outputs will remain disabled for $t_{LOCK}$ to allow motor to coast down to slower speed. After $t_{LOCK}$, a normal startup will resume operation assuming $V_{BB}$ has fallen below the hysteresis level.

| VBBOV | VBBOVDIS | OVPOPT | OVPTH | OVP Function |
|---|---|---|---|---|
| X | 1 | 1 | Outputs continue to run with $V_{BB} > V_{BBOV}$ | Disabled |
| 0 | X | 0 | 19 V | Disable outputs when $V_{BB} > V_{BBOV}$ |
| 0 | 0 | 1 | 19 V | Latch off for $t_{LOCK}$ |
| 1 | X | 0 | 38 V | Disable outputs when $V_{BB} > V_{BBOV}$ |
| 1 | 0 | 1 | 38 V | Latch off for $t_{LOCK}$ |

**Standby Mode.** A low power mode is activated if SPD pin is held low. Standby Mode will turn off all circuitry including charge pump and VREF. Upon power up, the A5947 will immediately wake up. If SPD remains low for the programmed lock time, standby mode will be activated. Standby mode can be disabled via EEPROM bit.

**Lock Detect.** The A5947 will turn off for the programmed time ($t_{LOCK}$) when the rotor is in a locked condition. A normal startup occurs after the lock timeout. EEPROM variable RETRY provides an option to count the number of lock events and prevent restart attempts after the count is exceeded. To resume operation after retry count is exceeded, PWM must be cycled OFF→ON. Lock event count can also be triggered by thermal shutdown events, OVP, or OCP events.

**Thermal Shutdown (TSD).** The A5947 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the upper threshold $T_{JTSD}$, the outputs will be disabled, and a lock timeout will be triggered. Device temperature must fall below the hysteresis level, $\Delta T_J$, to allow a normal restart sequence.

**EEPROM Security.** EEPROM can be password protected to prevent readback of the stored configuration. The IC will be shipped without password protection. Sequence to protect IC:

1. Power up.
2. Write 16-bit number to EEPROM register 7 per normal I²C EEPROM sequence.
3. Remember this password.
4. Power down.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

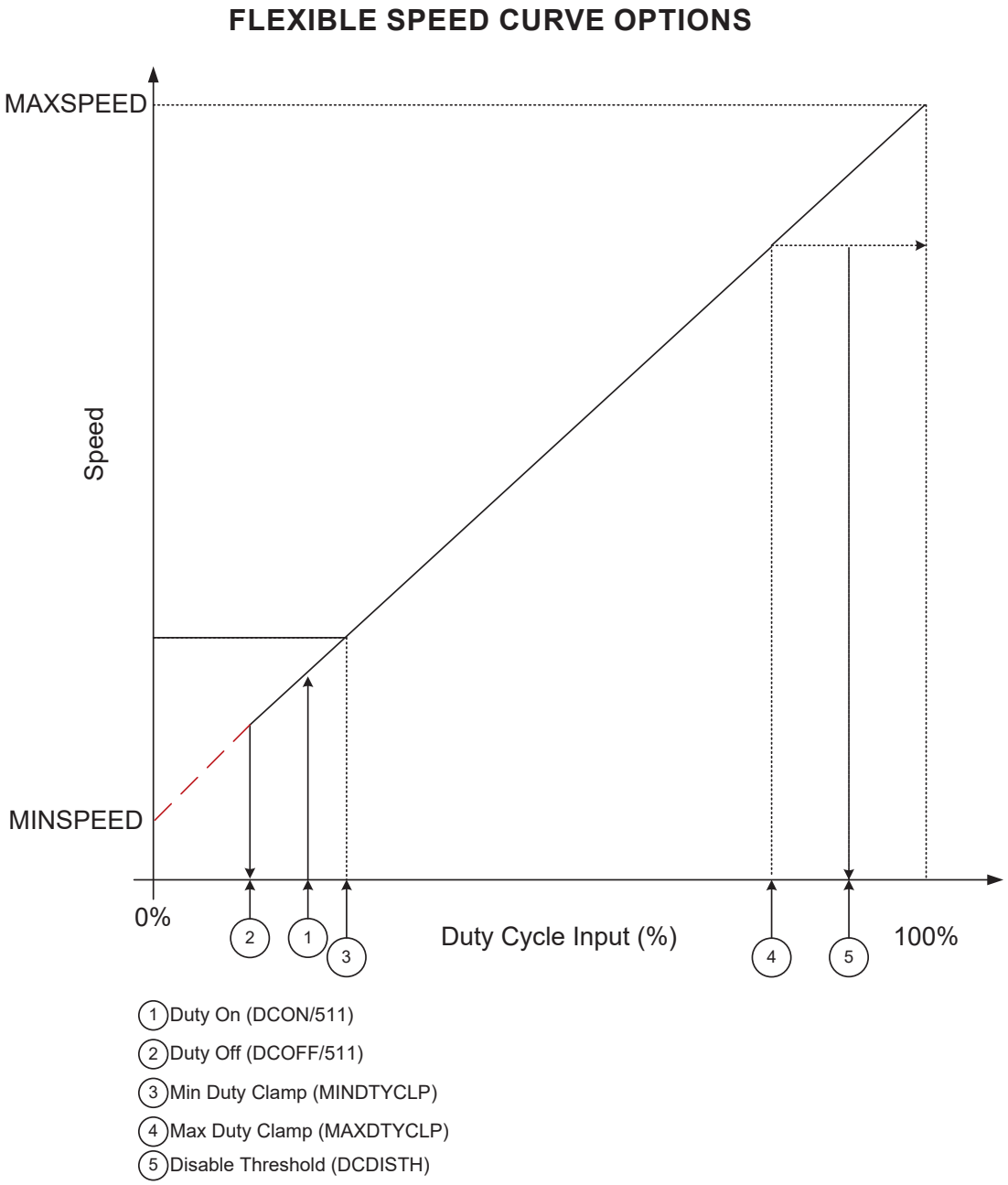



**Figure 3: Slope is set by selection of 100% speed, (MAXSPEED), and y-intercept (MINSPEED).**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

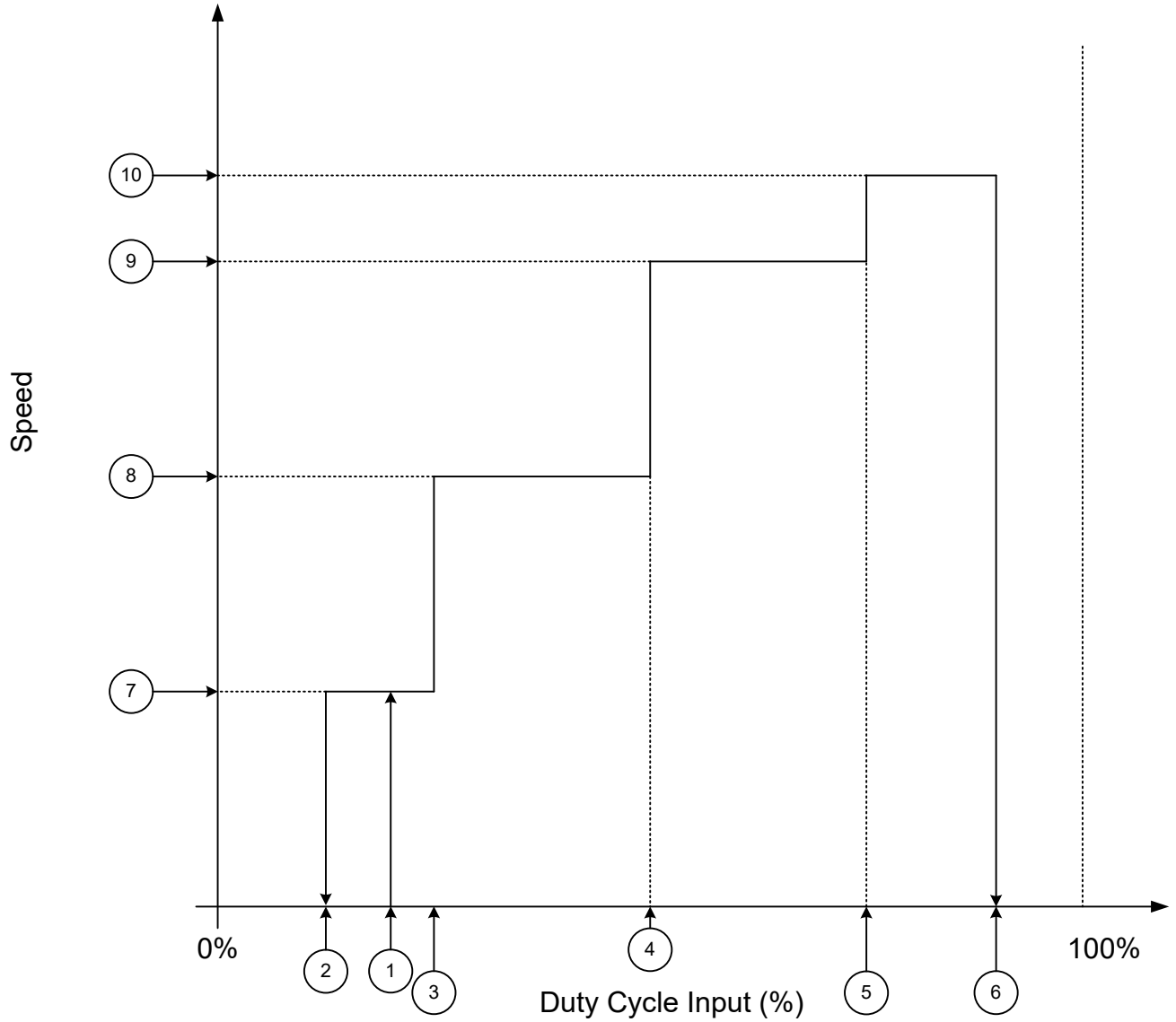
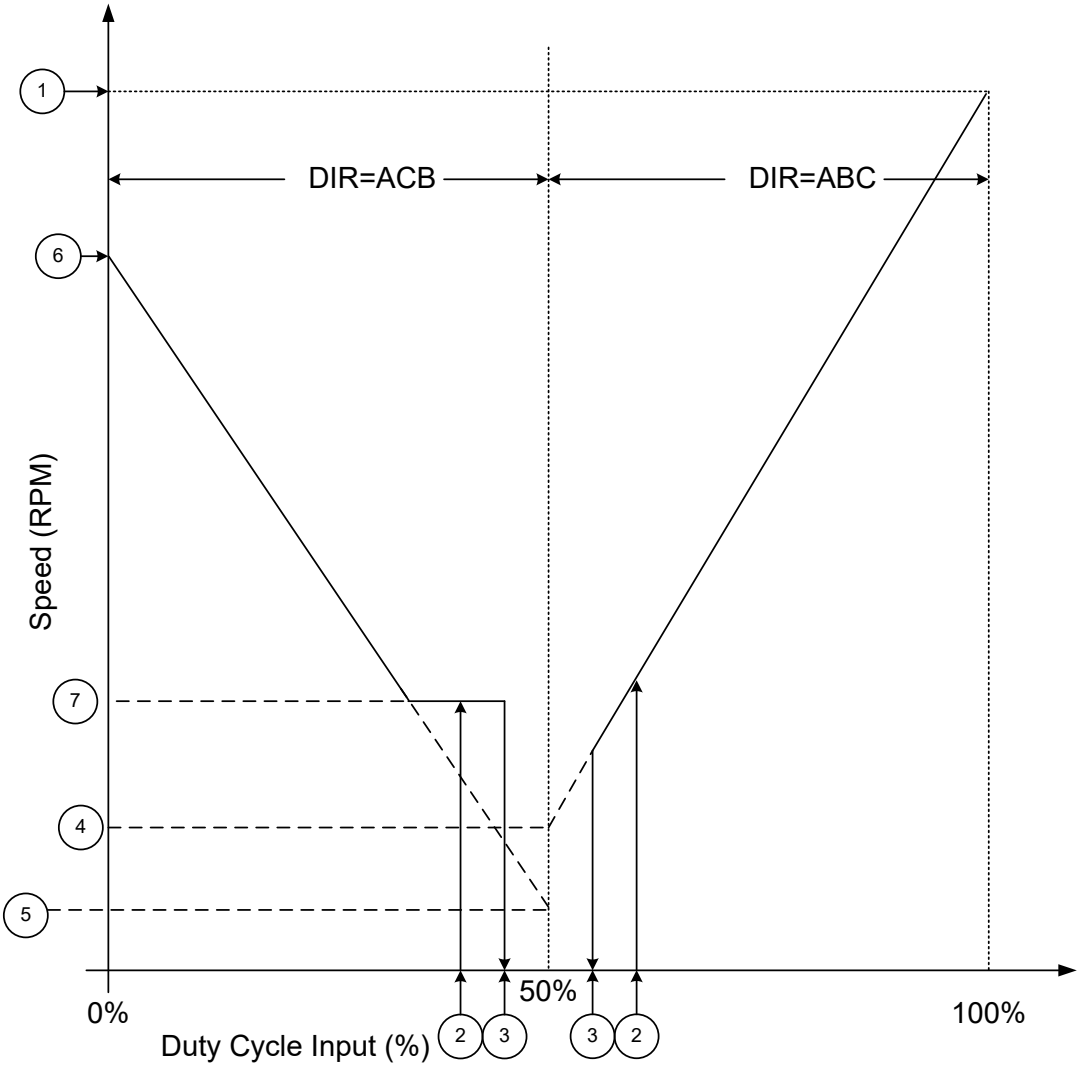



**Figure 4: Staircase Curves**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com




1 Maximum Speed (calculated from Slope of line AND Offset)
2 DCON
3 DCOFF
4 MINSPD1
5 MINSPD2
6 Maximum Speed2 (calculated from Slope of line AND Offset)
7 MINDTYCLP2

**Figure 5: Direction Change Based on 50% Reference**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## EEPROM MAP

| ADDR | REG | Bits | Name | Description | Default Setting | Default Value |
|---|---|---|---|---|---|---|
| 0 | 64 | 15:0 | Reserved | Allegro reserved | n/a | |
| 1 | 65 | 15:0 | Reserved | Allegro reserved | n/a | |
| 2 | 66 | 15:0 | Reserved | Allegro reserved | n/a | |
| 3 | 67 | 15:0 | Reserved | Allegro reserved | n/a | |
| 4 | 68 | 15:0 | CAS | Customer Code | n/a | |
| 5 | 69 | 15:0 | Reserved | Allegro reserved | n/a | |
| 6 | 70 | 15:0 | Extra | For customer use | n/a | |
| 7 | 71 | 15:0 | PASSWORD | Password | n/a | |
| 8 | 72 | 3:0 | MAXDTYCLP | Range = 100% to 76.5%, LSB = 1.56% | 100% | 0 |
| | | 9:4 | MINDTYCLP | Range = 0 to 50% LSB = 0.8% | 0% | 0 |
| | | 13:10 | DCDISTH | Range = 100% to 78.2%, LSB = 1.56%<br>DCDISTH(%) = 100% – (code – 1) × 1.56% | Disabled | 0 |
| | | 15:14 | DCDISHYS | 0.8% / 1.6% / 2.4% / 3.2% | 0.8% | 0 |
| 9 | 73 | 8:0 | STRTDMD | Range = 0 to VBBRNG, LSB = VBBRNG / 511 | 1.41 V | 38 |
| | | 15:9 | DMDPOST | Range=0 to 100%, LSB = 0.8% | 87.4% | 111 |
| 10 | 74 | 7:0 | TCOAST | Coast time for brake or dir change | 3 seconds | 30 |
| | | 15:8 | OPNLPMAX | Max speed limit for open loop mode | 15104 rpm | 59 |
| 11 | 75 | 7:0 | ACCELT | Range = 0 to 10.2 seconds, LSB = 40 ms | 760 ms | 19 |
| | | 15:8 | ACCEL | Range = 0 to 99.6 Hz/s LSB = 0.41 | 37.5 Hz/s | 96 |
| 12 | 76 | 7:0 | DCON | Range = 0 to 100% LSB = 0.4% | 9.8% | 25 |
| | | 10:8 | DCHYS | Range = 0.6 to 6.1% LSB = 0.8% | 2.9% | 3 |
| 13 | 77 | 3:0 | DMDRMPAL | Range = 3.8 to 63.8 ms/count, LSB = 4.0 | 23.8 ms/count | 5 |
| | | 7:4 | DMDRMPAH | Range = 2.0 to 32/count, LSB = 2.0 | 5.8 ms/count | 2 |
| | | 11:8 | DMDRMPDL | Range = 3.8 to 63.8 ms/count, LSB = 4.0 | 27.8 ms/count | 6 |
| | | 15:12 | DMDRMPDH | Range = 3.8 to 63.8 ms/count, LSB = 4.0 | 27.8 ms/count | 6 |
| 14 | 78 | 6:0 | KP | Closed Loop Kp | 16 | 16 |
| | | 7 | PIGAIN | 0:low Speed, 1:high Speed | 0 | 0 |
| | | 15:8 | KI | Closed Loop | 12 | 12 |
| 15 | 79 | 7:0 | MAXSPD | Maximum Electrical Frequency | 509 Hz | 24 |
| | | 15:8 | TLOCK | 0 to 25.4 seconds, 255 = latchoff | 5 seconds | 50 |
| 16 | 80 | 13:0 | SPDSLP1 | Calculated Slope of Speed Curve | 10000 rpm Maxspeed | 1252 |
| 17 | 81 | 11:0 | MINSPEED | Range = 0 to 4095, res = 1 rpm | 0 rpm | 0 |
| | | 15:12 | TRAPDTY | Duty to switch to trap drive LSB = 6.25% | Sine Only | 0 |
| 18 | 82 | 0 | CL | Speed Control Mode 0 = OpenLoop, 1 = Closed | Open | 0 |
| | | 1 | DIR | 0 = A→C→B, 1 = A→B→C | A→C→B | 0 |
| | | 2 | UVLO | 0 = Low (3.85 V), 1 = High (8.65 V) | High | 1 |
| | | 3 | SPDSEL | Speed Control Select 0 = PWM Duty, 1 = Analog | PWM | 0 |
| | | 6:4 | PP | Pole Pair = PP+1 | 2 Pole-Pair | 1 |
| | | 8:7 | ALIGN | 0:3 → 500 ms / 1 second / 1.5 seconds / 2 seconds | 1 second | 1 |
| | | 9 | OVPOPT | 0: disable, 1: lock detect | Lock Detect | 1 |
| | | 10 | SLEW | Output dv/dt select | 100 ns | 0 |
| | | 11 | Unused | Must Set to 0 | n/a | 0 |
| | | 13:12 | BEMFHYS | Bemf Hys Level for Startup | 40 mV | 1 |
| | | 14 | SOWAUTO | Initial Value of Window | 21 degrees | 1 |
| | | 15 | OCPOPT | 0 = Reset after Tlock, 1= After PWM on/off | Tlock | 0 |

*Continued on next page...*



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## EEPROM MAP (continued)

| ADDR | REG | Bits | Name | Description | Default Setting | Default Value |
|---|---|---|---|---|---|---|
| 19 | 83 | 0 | STBYDIS | Standby Mode 0 = Enable, 1 = Disable | Disabled | 1 |
| | | 1 | PWMF | Motor PWM Selection | 24 kHz | 0 |
| | | 2 | DTYIN | 0: Low F (34hz), 1: High F | Low | 0 |
| | | 4:3 | BEMFILT | Time Filter | 4 µs | 0 |
| | | 5 | TCENB | Temperature Compensation 0: Off, 1: On | Disabled | 0 |
| | | 6 | WINDMILL | 0: Resynchronize, 1: brake until stop | Resynchronize | 0 |
| | | 7 | POSTCOAST | 0 = 500 ms, 1 = 100 ms | 500 ms | 0 |
| | | 9:8 | DITHDT | Dither time (ms per step) | 1.3 | 0 |
| | | 11:10 | DITHSTP | Dither number of steps | 8 | 0 |
| | | 12 | DITHENB | 0 = Disabled, 1 = Enable dither function | Disabled | 0 |
| | | 13 | VBBOVDIS | 0 = Enable, 1 = Disable | Enabled | 0 |
| | | 14 | VBBOV | 0 = 19 V, 1 = 38 V | 19 V | 0 |
| | | 15 | VBBRNG | 0 = 19 V, 1 = 38 V | 19 V | 0 |
| 20 | 84 | 0 | DTYINV | 0 = Normal, 1 = Invert | Normal | 0 |
| | | 1 | Reserved | Allegro Reserved – Set to One | 1 | 1 |
| | | 2 | STAIR | 1 = Enable Staircase | Disabled | 0 |
| | | 3 | DIR50 | 1: Enable Direction change based on 50% duty | Disabled | 0 |
| | | 4 | BRKOFF | 0 = coast, 1 = Brake | Disabled | 0 |
| | | 6:5 | STRT | 0 = Align, 1 = One cycle, 2 = IPD-ZT, 3 = IPD-T | One Cycle | 1 |
| | | 7 | IPDTOPT | 0 = Slow Decay, 1 = Fast Decay | Slow | 0 |
| | | 8 | Reserved | | Set to 1 | 1 |
| | | 14:9 | DUTYC | Range = 1.37 to 100%, LSB = 1.56% | 60.86% | 38 |
| 21 | 85 | 7:0 | SPEEDA | Range = 0 to 8160, RES 32 rpm | 2016 rpm | 63 |
| | | 15:8 | SPEEDB | Range = 0 to 8160, RES 32 rpm | 3008 rpm | 94 |
| 22 | 86 | 7:0 | SPEEDC | Range = 0 to 8160, RES 32 rpm | 4000 rpm | 125 |
| | | 15:8 | SPEEDD | Range = 0 to 8160, RES 32 rpm | 4992 rpm | 156 |
| 23 | 87 | 5:0 | DUTYA | Range = 1.37 to 100%, LSB = 1.56% | 20.16% | 12 |
| | | 13:8 | DUTYB | Range = 1.37 to 100%, LSB = 1.56% | 40.51% | 25 |
| 24 | 88 | 11:0 | MINSPD2 | Range=0 to 4095, res = 1 rpm (DIR50 mode) | 0 | 0 |
| | | 15:12 | RETRY | Number of retry attempts when rotor locked (0 = function disabled) | Disabled | 0 |
| 25 | 89 | 13:0 | SPDSLP2 | Calculated Slope of Speed Curve (DIR50 and dual slope mode) | 10000 rpm Maxspeed | 1252 |
| 26 | 90 | 5:0 | MINDTYCLP2 | Range = 0 to 50%, LSB = 0.8% (DIR50) | 0 | 0 |
| | | 13:6 | SLPSWDTY | Slope Switch Duty for dual slope mode | Disabled | 0 |
| | | 15:14 | Unused | | n/a | |
| 27 | 91 | 15:0 | SLPSWRPM | Slope Switch rpm for dual slope mode | 0 | 0 |
| 28 | 92 | 15:0 | Reserved | Allegro Reserved - Locked | n/a | n/a |
| 29 | 93 | 7:0 | IPDRMP | Duty Ramp for IPD-T | 10 ms | 9 |
| | | 15:8 | STRTF | Frequency for 1-cycle startup Mode | 1 Hz | 16 |
| 30 | 94 | 15:0 | Reserved | Allegro Reserved – Must be Set to Zero | 0 | 0 |
| 31 | 95 | 15:0 | Reserved | Allegro Reserved - Locked | n/a | n/a |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## SERIAL PORT CONTROL OPTION

Normally the IC is controlled by duty cycle input and uses the EEPROM data that is stored to create the speed curve profile. However, it is possible to use direct serial port control to avoid programming EEPROM.

When using direct control, the input duty cycle command is replaced by writing a 9-bit number to register 165.

Example:

REGADDR[data]: (in decimal)

165[511] → Duty = 100%

165[102] → Duty = 102 / 511 = 20%

Upon power up, the IC defaults to duty cycle input mode. To use serial port mode, the internal registers should be programmed before turning the part on. The sequence to use serial port mode is:

1. Drive FG and SPD pins low *
2. Power-up IC
3. Program registers for parameter setting that correspond to each of the EEPROM memory locations.
   A. REGADDR = 64 + EEPROM ADDR.
   B. Program register addresses 72 to 94 corresponding to EEPROM addresses 8 to 30.
   C. It may be helpful to use the GUI text file to help define the hex data for each of the EEPROM addresses.
4. Write to register 165 to start motor

* Note: If SPD is not driven low before power up, motor will try to start immediately as the default high value will demand 100% on signal.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

### I²C Control Registers

| REG | Bits | | Function | Description |
|---|---|---|---|---|
| 165 | [8:0] | r/w | Speed Demand Input | Duty (%) = code / 511 |
| 128 | [8:0] | r | Duty applied | Actual demand to the motor windings |
| 138 | [7:0] | r | Die temp | Temp °C = 3 + (CODE – 133) / 2 |
| 144 | [15:0] | r/w | Number of startup failures | Cleared by writing zero or powerup |
| 145 | [15:0] | r/w | Number of startup attempts | Cleared by writing zero or powerup |
| 147 | [9:0] | | Fault Status | |
| | 0 | r | Low-side VDS A | |
| | 1 | r | Low-side VDS B | |
| | 2 | r | Low-side VDS C | |
| | 3 | r | High-side VDS A | |
| | 4 | r | High-side VDS B | |
| | 5 | r | High-side VDS C | |
| | 6 | r | TSD | |
| | 7 | r | Charge Pump UVLO | |
| | 8 | r | VBB UVLO | |
| | 9 | r | VBB Overvoltage | |
| 148 | [15:0] | | Lock detect criteria | |
| | 0 | r | Switch Over Error | |
| | 1 | r | Too Slow | |
| | 2 | r | Too Fast | |
| | 3 | r | Out of Sync | |
| | 4 | r | Bad Acceleration | |
| | 5 | r | Windmill Error | |
| | 6 | r | Max Phase Advance | |
| | 14:7 | | Unused | |
| | 15 | w | Clear | Write 1 to clear the latched faults |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Serial Port

The A5947 uses standard fast mode I²C serial port format to program the EEPROM or to control the IC speed serially. The serial port can be used for startup configuration, fault readback, direction control, or input duty request. The SPD pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running, the FG may pull then data line low while trying to initialize into serial port mode. Once an I²C command is received, the SPD input is ignored, and the motor will turn off as if a PWM duty command of 0% was sent.

The A5947 7-bit slave address is 0x55.

## I²C Timing Diagrams

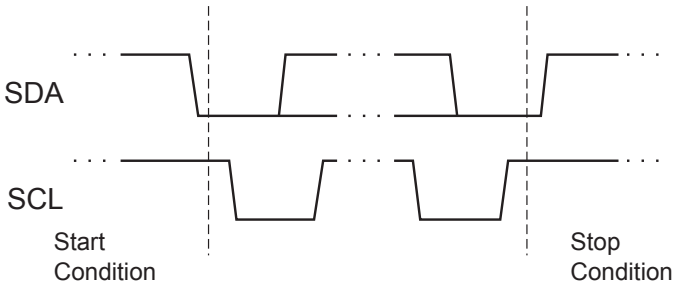



**Figure 6: Start and Stop Conditions**

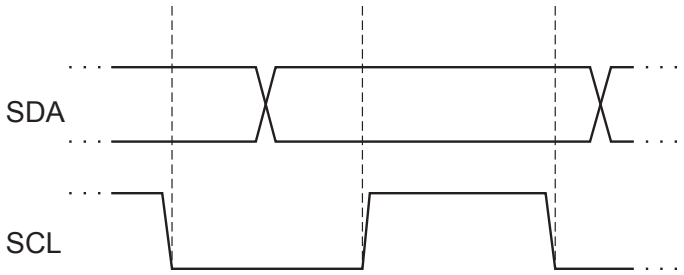



**Figure 7: Clock and Data Bit Synchronization**

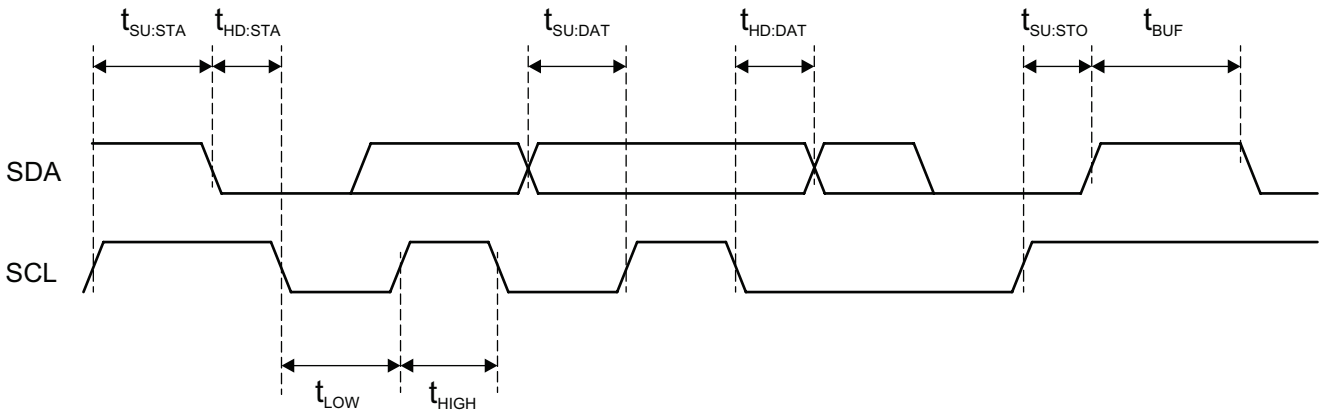



**Figure 8: I²C-Compatible Timing Requirements**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Write Command

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address
4. 2 data bytes, MSB first
5. Stop Condition

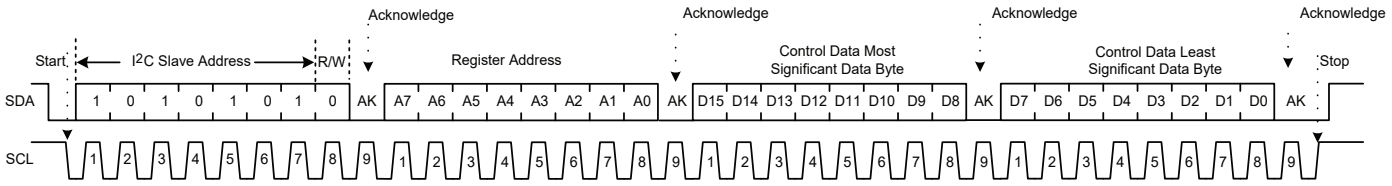



**Figure 9: Write Command**

## Read Command

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address to be read
4. Stop Condition
5. Start Condition
6. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 1
7. Read 2 data bytes
8. Stop Condition

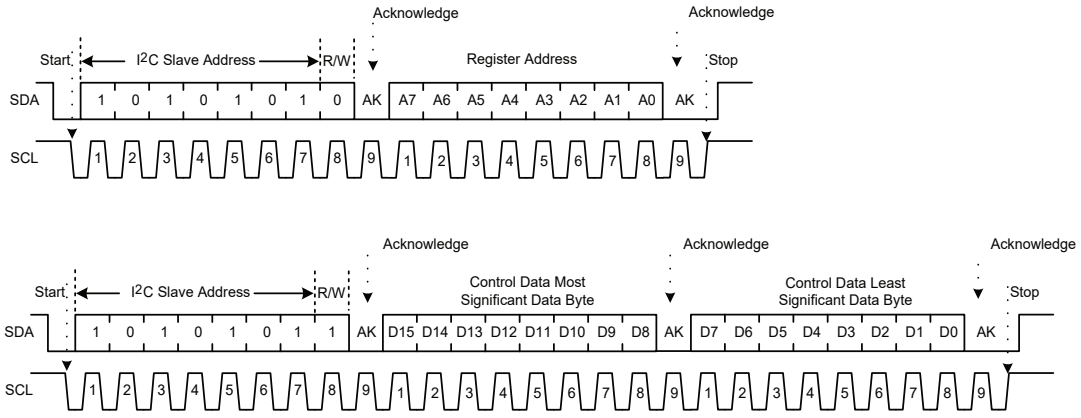



**Figure 10: Read Command**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Programming EEPROM

The A5947 contains 32 words of 16-bit length. The EEPROM is controlled with the following I²C registers. Refer to application note for EEPROM definition.

**Table 1: EEPROM Control – Register 161 (Used to control programming of EEPROM)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RD | WR | ER | EN |

| Bit | Name | Description |
|---|---|---|
| 0 | EN | Set EEPROM voltage required for writing or erasing |
| 1 | ER | Sets mode to erase |
| 2 | WR | Sets mode to write |
| 3 | RD | Sets mode to read |
| 15:4 | n/a | Do not use; always set to zero during programming process |

**Table 2: EEPROM Address – Register 162 (Used to set the EEPROM address to be altered)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | eeADDRESS | | | | |

| Bit | Name | Description |
|---|---|---|
| 4:0 | eeADDRESS | Used to specify EEPROM address to be changed. |
| 15:5 | n/a | Do not use; always set to zero during programming process |

**Table 3: EEPROM DataIn – Register 163 (Used to set the EEPROM new data to be programmed)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| eeDATAin | | | | | | | | | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 15:0 | eeDATAin | Used to specify the new EEPROM data to be changed |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 4: DataOUT – Register 164 (Used for read operations)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| eeDATAout | | | | | | | | | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 15:0 | eeDATAout | Used to readback EEPROM data from address defined in register 162 |

There are 3 basic commands: Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 12 ms per word.

Each word must be written individually.

Example #1: Write EEPROM address 5 to 261 (0x0105)

1) Erase the word

| | | |
|---|---|---|
| | I²C Write REGADDR[Data] | ; comment |
| a. | 162[5] | ; set EEPROM address to erase |
| b. | 163[0] | ; set 0000 as Data In |
| c. | 161[3] | ; set control to Erase and Voltage High |
| d. | Wait 12 ms | ; requires 12 ms High Voltage Pulse to Write |

2) Write the new data

| | | |
|---|---|---|
| a. | 162[5] | ; set EEPROM address to write |
| b. | 163[261] | ; set Data In = 261 |
| c. | 161[5] | ; set control to Write and Set Voltage High |
| d. | Wait 12 ms | ; requires 12 ms High Voltage Pulse to Write |

Example #2: Read EEPROM address 5 to confirm correct data properly programmed

1) Read the word

| | | |
|---|---|---|
| a. | 5[I²C Read] | ; set EEPROM address to read |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## PIN DIAGRAMS

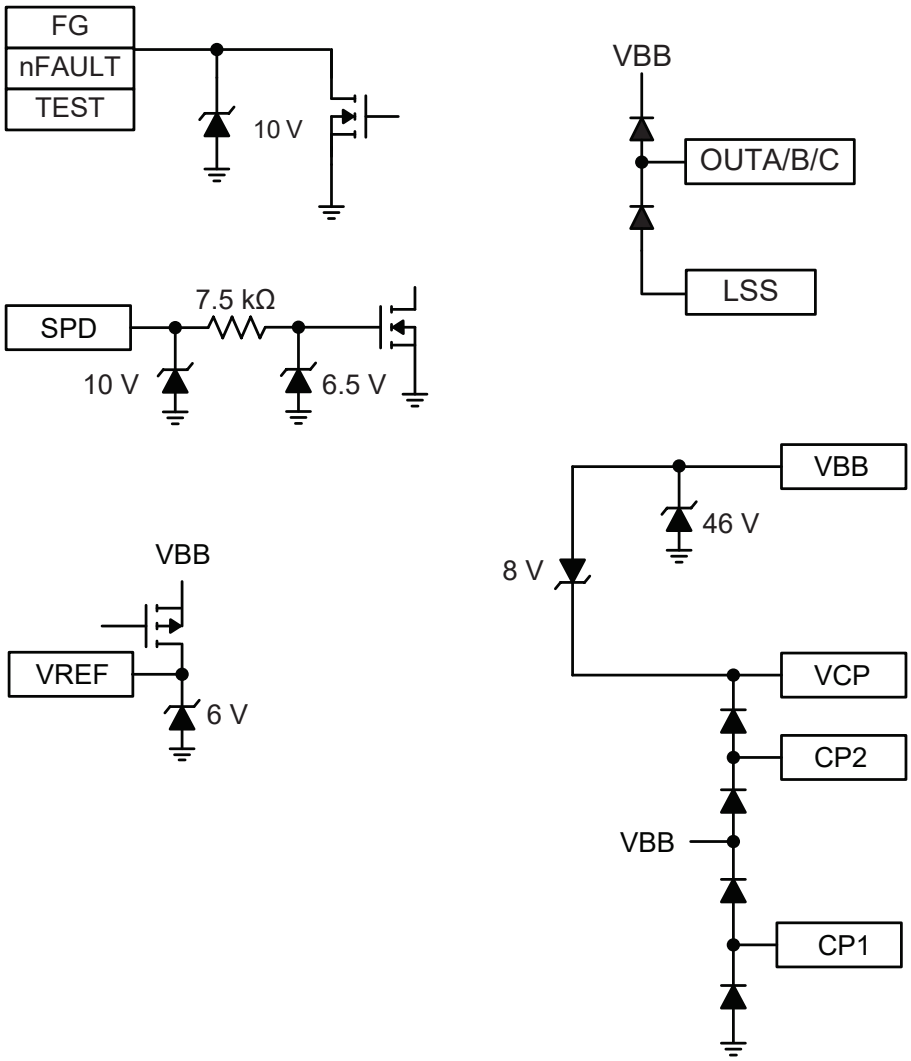



**Figure 11: Pin Diagrams**

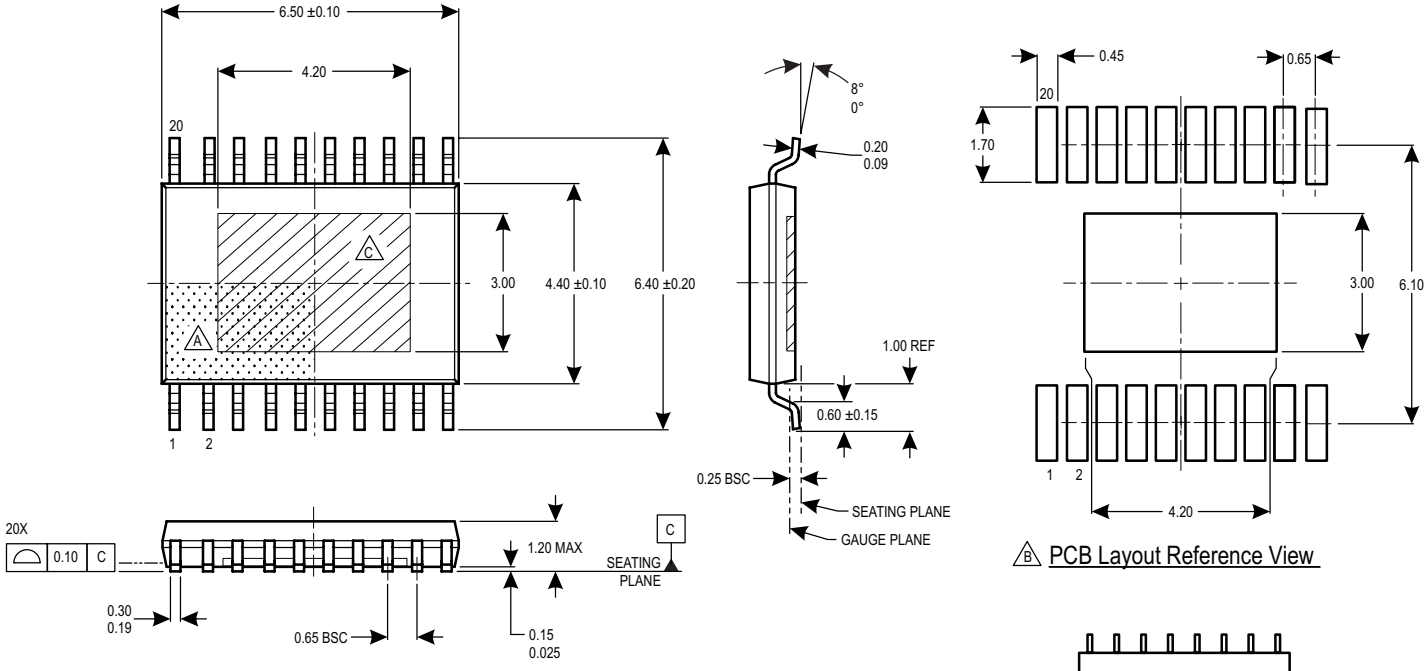


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## PACKAGE OUTLINE DRAWING

**For Reference Only – Not for Tooling Use**

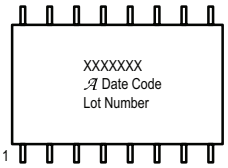
(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown







B PCB Layout Reference View




D Standard Branding Reference View

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

**Figure 12: Package LP, 20-Lead TSSOP with Exposed Pad**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Revision History

| Number | Date | Description |
|---|---|---|
| – | May 13, 2021 | Initial release |
| 1 | July 23, 2021 | Removed ET package |
| 2 | April 7, 2022 | Updated Motor PWM Frequency and Speed Setpoint (page 4); updated package drawing (page 20) |

Copyright 2022, Allegro MicroSystems.
Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.
Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.
The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.
Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:
www.allegromicro.com



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com