



**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

# 8-Mbit (512K × 16) Static RAM

## Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V–2.25 V
- Pin compatible with CY62157DV18 and CY62157DV20
- Ultra low standby power
  - Typical Standby current: 2  $\mu$ A
  - Maximum Standby current: 8  $\mu$ A
- Ultra low active power
  - Typical active current: 6 mA at  $f = 1$  MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) package

## Functional Description

The CY62157EV18 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power

consumption when addresses are not toggling. The device can also be put into **standby mode** when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when:

- Deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both **Byte High Enable** and **Byte Low Enable** are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH) or
- Write operation is active ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW).

Write to the device by taking Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Read from the device by taking Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See the [Truth Table on page 13](#) for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

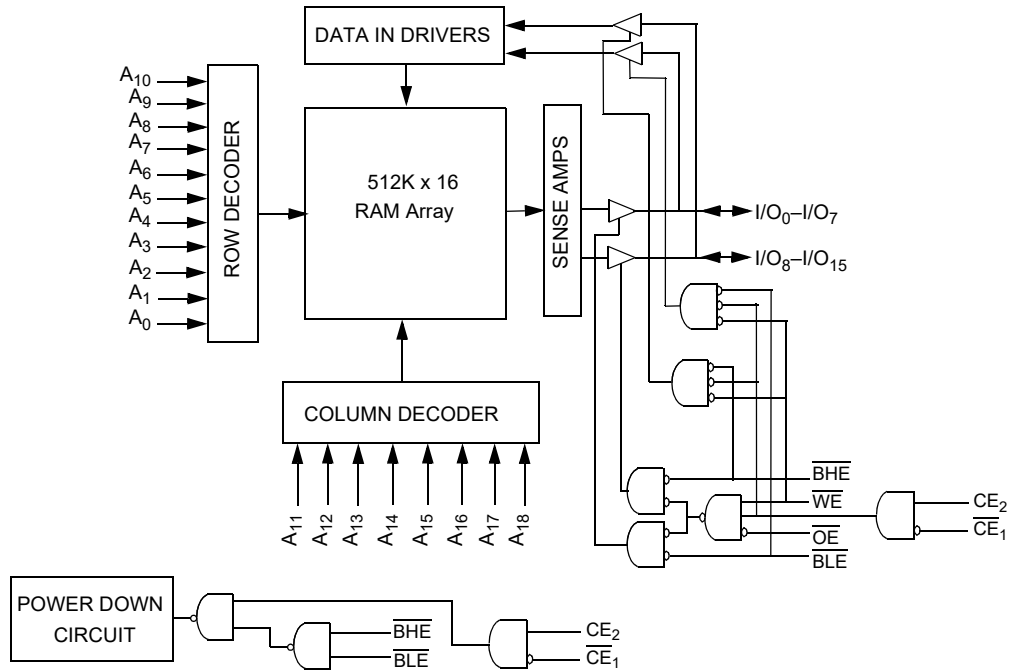
## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> , (mA)				Standby, I <sub>SB2</sub> ( $\mu$ A)	
	f = 1MHz		f = f <sub>max</sub>							
	Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY62157EV18	1.65	1.8	2.25	55	6	7	18	25	2	8

### Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

**Logic Block Diagram**

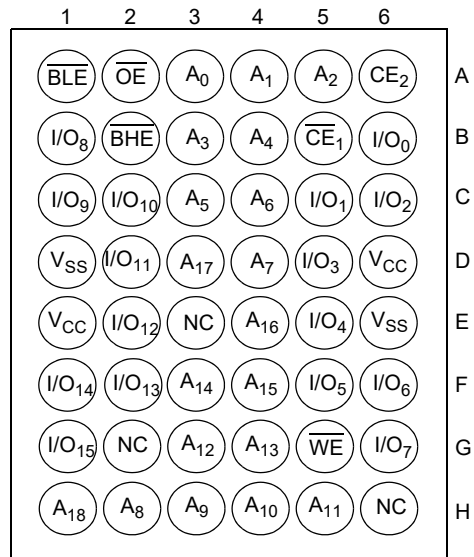


## Contents

<b>Pin Configuration</b> .....	<b>4</b>	<b>Package Diagram</b> .....	<b>15</b>
<b>Maximum Ratings</b> .....	<b>5</b>	<b>Acronyms</b> .....	<b>16</b>
<b>Operating Range</b> .....	<b>5</b>	<b>Document Conventions</b> .....	<b>16</b>
<b>Electrical Characteristics</b> .....	<b>5</b>	Units of Measure .....	16
<b>Capacitance</b> .....	<b>6</b>	<b>Document History Page</b> .....	<b>17</b>
<b>Thermal Resistance</b> .....	<b>6</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>21</b>
<b>AC Test Loads and Waveforms</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	21
<b>Data Retention Characteristics</b> .....	<b>7</b>	Products .....	21
<b>Data Retention Waveform</b> .....	<b>7</b>	PSoC® Solutions .....	21
<b>Switching Characteristics</b> .....	<b>8</b>	Cypress Developer Community .....	21
<b>Switching Waveforms</b> .....	<b>9</b>	Technical Support .....	21
<b>Truth Table</b> .....	<b>13</b>		
<b>Ordering Information</b> .....	<b>14</b>		
Ordering Code Definitions .....	14		

## Pin Configuration

Figure 1. 48-ball VFBGA pinout (Top View) [2]



**Note**

2. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature with power applied ..... -55 °C to + 125 °C

Supply voltage to ground potential ..... -0.2 V to 2.45 V ( $V_{CCmax} + 0.2$  V)

DC voltage applied to outputs in High-Z state <sup>[3, 4]</sup> ..... -0.2 V to 2.45 V ( $V_{CCmax} + 0.2$  V)

DC input voltage <sup>[3, 4]</sup> ..... -0.2 V to 2.45 V ( $V_{CCmax} + 0.2$  V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (in accordance with MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[5]</sup>
CY62157EV18LL	Industrial	-40 °C to +85 °C	1.65 V to 2.25 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ <sup>[6]</sup>	Max	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -0.1$ mA, $V_{CC} = 1.65$ V	1.4	–	–	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 0.1$ mA, $V_{CC} = 1.65$ V	–	–	0.2	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 1.65$ V to 2.25 V	1.4	–	$V_{CC} + 0.2$ V	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 1.65$ V to 2.25 V	-0.2	–	0.4	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	–	+1	$\mu$ A
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , output disabled	-1	–	+1	$\mu$ A
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$ , $V_{CC} = V_{CC(max)}$ , $I_{OUT} = 0$ mA CMOS levels	–	18	25	mA
		$f = 1$ MHz	–	6	7	mA
$I_{SB1}$ <sup>[7]</sup>	Automatic CE power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (address and data only), $f = 0$ (OE, WE, BHE and BLE), $V_{CC} = V_{CC(max)}$ .	–	2	8	$\mu$ A
$I_{SB2}$ <sup>[7]</sup>	Automatic CE power down current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = V_{CC(max)}$ .	–	2	8	$\mu$ A

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.5$  V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100  $\mu$ s ramp time from 0 to  $V_{CC}$  (min) and 200  $\mu$ s wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Chip enable ( $\overline{CE}$ ) and byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.

### Capacitance

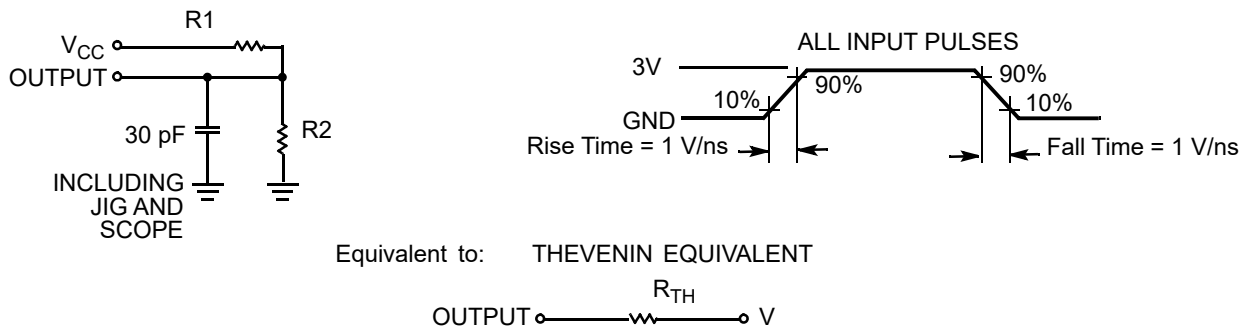
Parameter <sup>[8]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

Parameter <sup>[8]</sup>	Description	Test Conditions	BGA	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	36.92	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		13.55	°C/W

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	Value	Unit
R1	13500	Ω
R2	10800	Ω
R <sub>TH</sub>	6000	Ω
V <sub>TH</sub>	0.80	V

**Note**

8. Tested initially and after any design or process changes that may affect these parameters.

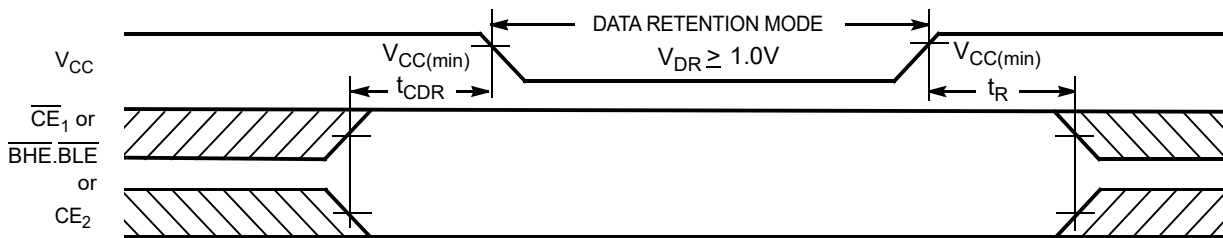
### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[9]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	–	V
$I_{CCDR}$ <sup>[10]</sup>	Data retention current	$1.2\text{ V} \leq V_{CC} \leq V_{CC(max)}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ , $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	5	9	$\mu\text{A}$
$t_{CDR}$ <sup>[11]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[12]</sup>	Operation recovery time		55	–	–	ns

### Data Retention Waveform

Figure 3. Data Retention Waveform<sup>[13]</sup>



**Notes**

- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
- 10. Chip enable ( $\overline{CE}$ ) and byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.
- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
- 13.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .



## Switching Characteristics

Over the Operating Range

Parameter <sup>[14, 15]</sup>	Description	55 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	55	–	ns
$t_{AA}$	Address to data valid	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[16]</sup>	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[16, 17]</sup>	–	18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low-Z <sup>[16]</sup>	10	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to High-Z <sup>[16, 17]</sup>	–	18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to power up	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to power down	–	55	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
$t_{LZBE}$ <sup>[18]</sup>	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z <sup>[16]</sup>	10	–	ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z <sup>[16, 17]</sup>	–	18	ns
<b>Write Cycle</b> <sup>[19, 20]</sup>				
$t_{WC}$	Write cycle time	55	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	40	–	ns
$t_{AW}$	Address setup to write end	40	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	40	–	ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to write end	40	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[16, 17]</sup>	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[16]</sup>	10	–	ns

### Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 2 on page 6](#).
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the output enters a high impedance state.
18. If both byte enables are toggled together, this value is 10 ns.
19. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
20. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [21, 22]

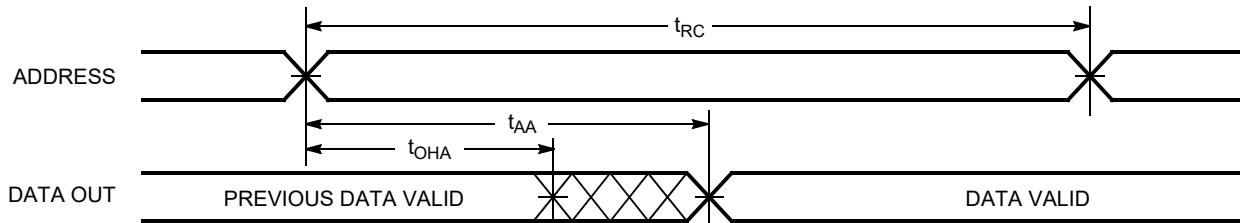
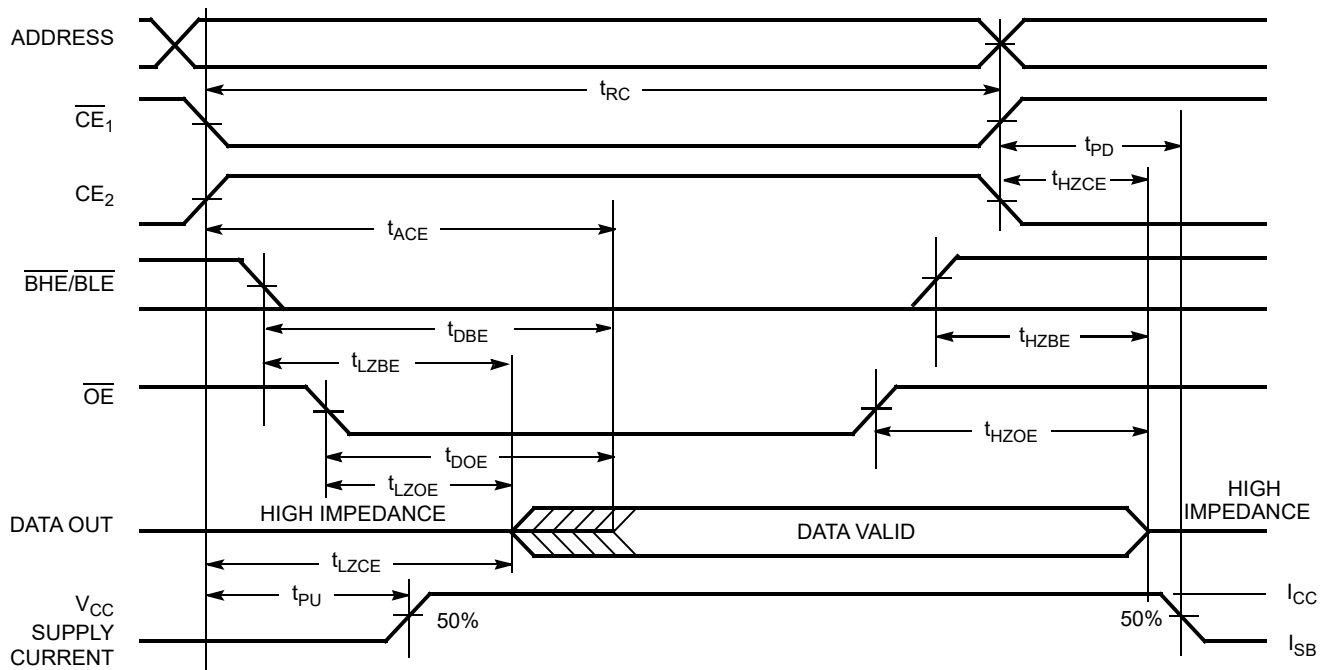


Figure 5. Read Cycle 2 ( $\overline{OE}$  Controlled) [22, 23]



**Notes**

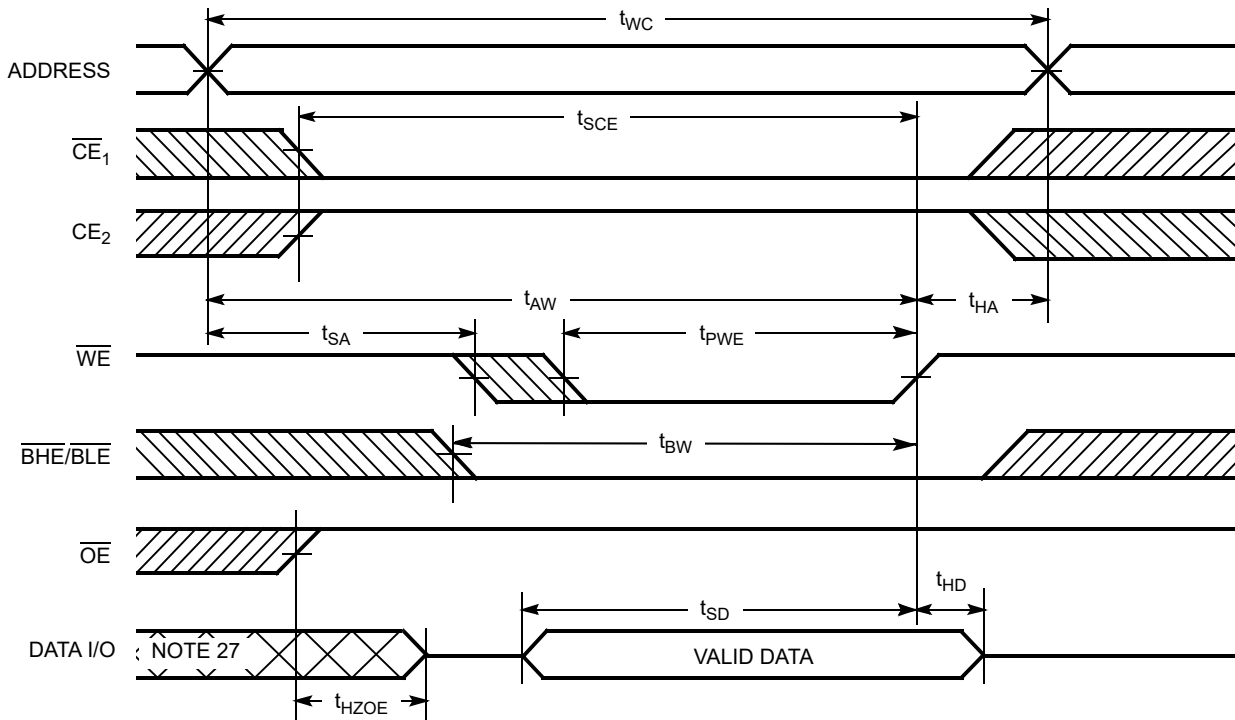
21. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ .

22.  $\overline{WE}$  is HIGH for read cycle.

23. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle 1 ( $\overline{WE}$  Controlled) [24, 25, 26]



Notes

24. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

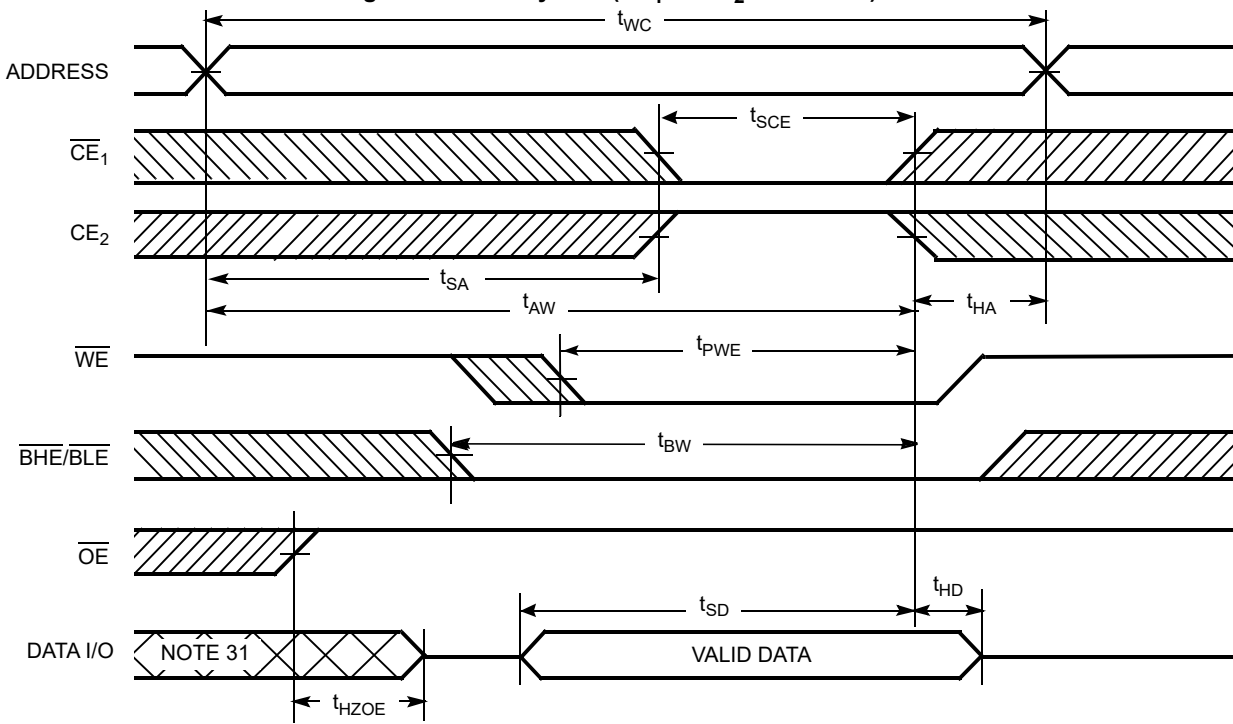
25. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

26. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

27. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [28, 29, 30]



Notes

28. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

29. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

30. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

31. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [32, 33]

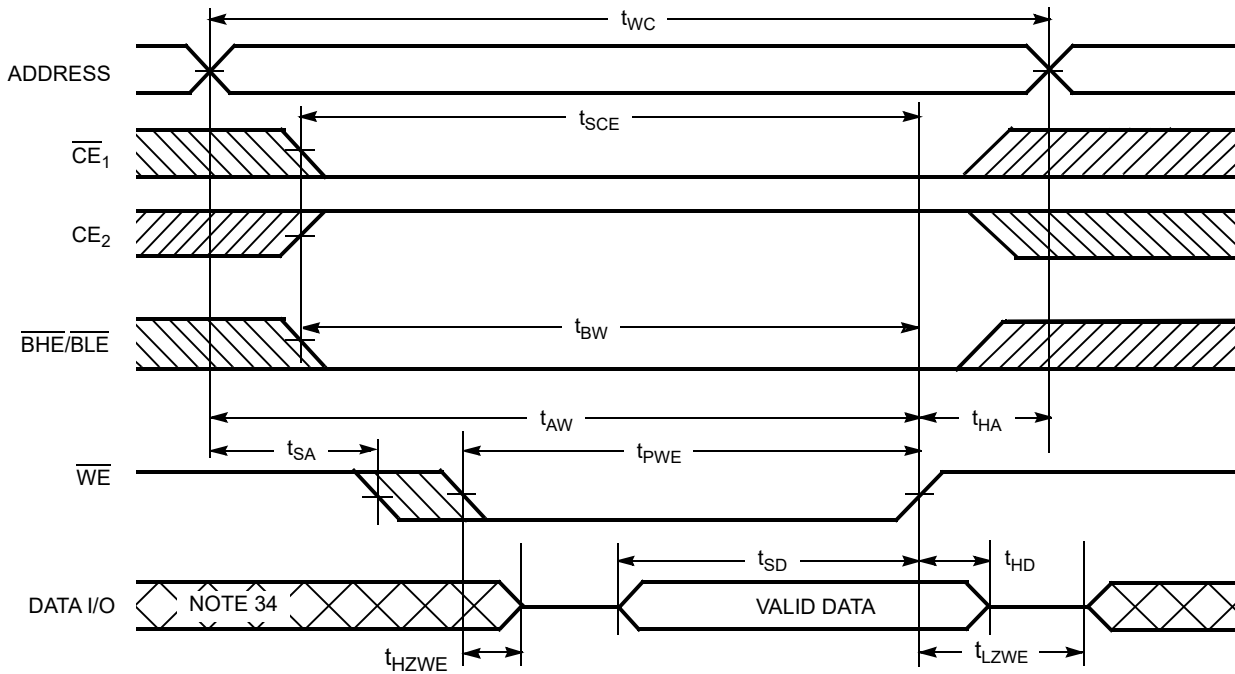
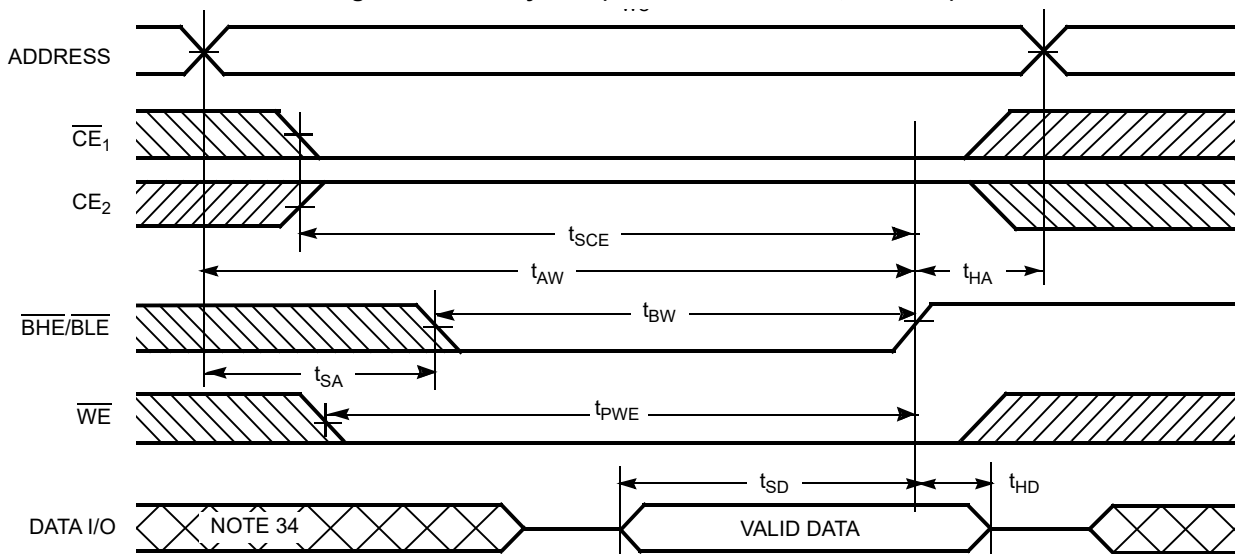


Figure 9. Write Cycle 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW) [32]



Notes

32. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

33. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

34. During this period, the I/Os are in output state and input signals must not be applied.

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	$\chi^{[35]}$	X	X	$\chi^{[35]}$	$\chi^{[35]}$	High-Z	Deselect/Power down	Standby ( $I_{SB}$ )
$\chi^{[35]}$	L	X	X	$\chi^{[35]}$	$\chi^{[35]}$	High-Z	Deselect/Power down	Standby ( $I_{SB}$ )
$\chi^{[35]}$	$\chi^{[35]}$	X	X	H	H	High-Z	Deselect/Power down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data out ( $I/O_0$ – $I/O_7$ ); High-Z ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	High-Z ( $I/O_0$ – $I/O_7$ ); Data out ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	L	H	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data in ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data in ( $I/O_0$ – $I/O_7$ ); High-Z ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	High-Z ( $I/O_0$ – $I/O_7$ ); Data in ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )

**Note**

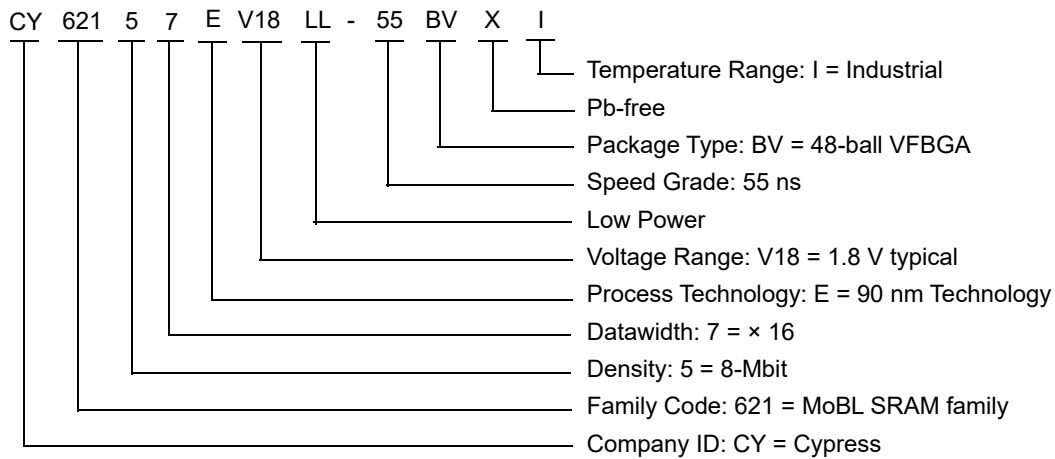
35. The 'X' (Don't care) state for the Chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62157EV18LL-55BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

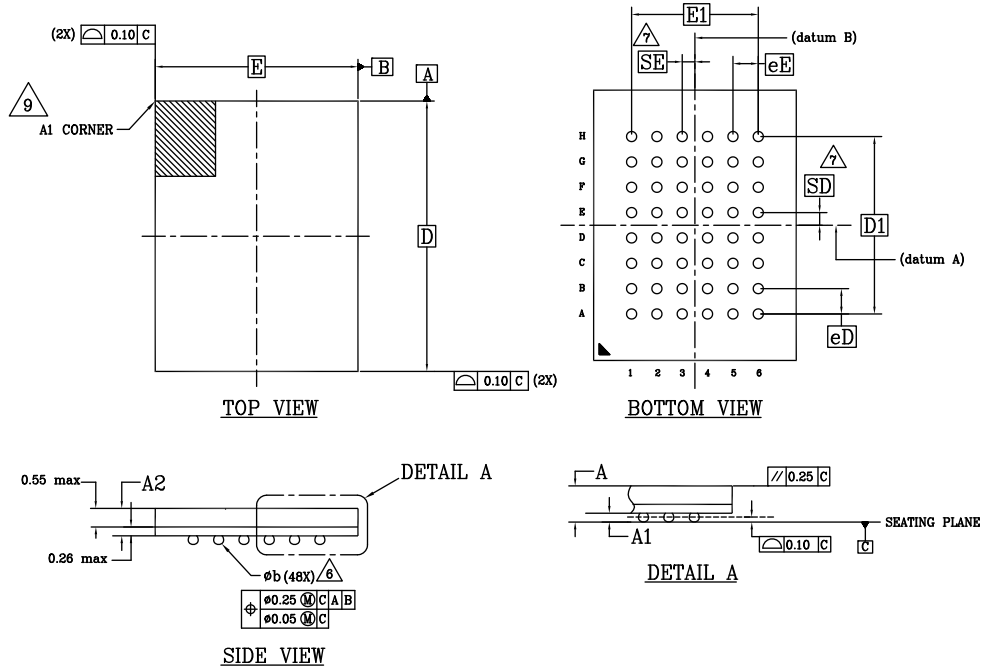
Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



Package Diagram

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1,00
A1	0,16	-	-
A2	-	-	0,81
D	8,00 BSC		
E	6,00 BSC		
D1	5,25 BSC		
E1	3,75 BSC		
MD	8		
ME	6		
n	48		
$\phi$ b	0,25	0,30	0,35
eE	0,75 BSC		
eD	0,75 BSC		
SD	0,375 BSC		
SE	0,375 BSC		

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- $\square$  REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION, SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- $\triangle$  DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- $\triangle$  "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- \*\* INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- $\triangle$  A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 \*1



## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
$\mu\text{A}$	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
$\Omega$	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62157EV18 MoBL, 8-Mbit (512K × 16) Static RAM			
Document Number: 38-05490			
Rev.	ECN No.	Submission Date	Description of Change
**	202862	01/27/2004	New data sheet.
*A	291272	11/19/2004	<p>Changed status from Advance Information to Preliminary.</p> <p>Updated <a href="#">Features</a>: Updated description.</p> <p>Updated <a href="#">Operating Range</a>: Updated Note 5 (Replaced “100 μs wait time” with “200 μs wait time”).</p> <p>Updated <a href="#">Data Retention Characteristics</a>: Changed maximum value of I<sub>CCDR</sub> parameter from 4 μA to 4.5 μA.</p> <p>Updated <a href="#">Switching Characteristics</a>:            Changed minimum value of t<sub>OHA</sub> parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bins.            Changed maximum value of t<sub>DOE</sub> parameter from 15 ns to 18 ns corresponding to 35 ns speed bin.            Changed maximum value of t<sub>HZOE</sub> parameter from 12 ns to 15 ns corresponding to 35 ns speed bin.            Changed maximum value of t<sub>HZOE</sub> parameter from 15 ns to 18 ns corresponding to 45 ns speed bin.            Changed maximum value of t<sub>HZCE</sub> parameter from 12 ns to 18 ns corresponding to 35 ns speed bin.            Changed maximum value of t<sub>HZCE</sub> parameter from 15 ns to 22 ns corresponding to 45 ns speed bin.            Changed maximum value of t<sub>HZBE</sub> parameter from 12 ns to 15 ns corresponding to 35 ns speed bin.            Changed maximum value of t<sub>HZBE</sub> parameter from 15 ns to 18 ns corresponding to 45 ns speed bin.            Changed minimum value of t<sub>SCE</sub> parameter from 25 ns to 30 ns corresponding to 35 ns speed bin.            Changed minimum value of t<sub>SCE</sub> parameter from 40 ns to 35 ns corresponding to 45 ns speed bin.            Changed minimum value of t<sub>AW</sub> parameter from 25 ns to 30 ns corresponding to 35 ns speed bin.            Changed minimum value of t<sub>AW</sub> parameter from 40 ns to 35 ns corresponding to 45 ns speed bin.            Changed minimum value of t<sub>BW</sub> parameter from 25 ns to 30 ns corresponding to 35 ns speed bin.            Changed minimum value of t<sub>BW</sub> parameter from 40 ns to 35 ns corresponding to 45 ns speed bin.            Changed minimum value of t<sub>SD</sub> parameter from 15 ns to 18 ns corresponding to 35 ns speed bin.            Changed minimum value of t<sub>SD</sub> parameter from 20 ns to 22 ns corresponding to 45 ns speed bin.            Changed maximum value of t<sub>HZWE</sub> parameter from 12 ns to 15 ns corresponding to 35 ns speed bin.            Changed maximum value of t<sub>HZWE</sub> parameter from 15 ns to 18 ns corresponding to 45 ns speed bin.</p> <p>Updated <a href="#">Ordering Information</a>: Updated part numbers.</p>

Document History Page (continued)

Document Title: CY62157EV18 MoBL, 8-Mbit (512K × 16) Static RAM			
Document Number: 38-05490			
Rev.	ECN No.	Submission Date	Description of Change
*B	444306	04/13/2006	<p>Changed status from Preliminary to Final.</p> <p>Removed 35 ns Speed Bin related information in all instances across the document.</p> <p>Removed "L" from the part numbers across the document.</p> <p>Updated <a href="#">Pin Configuration</a>:</p> <p>Updated <a href="#">Figure 1</a> (Changed ball E3 from DNU to NC).</p> <p>Removed Note "DNU pins have to be left floating or tied to Vss to ensure proper application." and its reference.</p> <p>Updated <a href="#">Maximum Ratings</a>:</p> <p>Updated ratings corresponding to "Supply Voltage to Ground Potential", "DC Voltage Applied to Outputs in High Z State", "DC Input Voltage" (Replaced "2.4 V" with "2.45 V").</p> <p>Updated <a href="#">Electrical Characteristics</a>:</p> <p>Changed typical value of I<sub>CC</sub> parameter from 16 mA to 18 mA corresponding to Test Condition "f = f<sub>MAX</sub> = 1/t<sub>RC</sub>".</p> <p>Changed maximum value of I<sub>CC</sub> parameter from 28 mA to 25 mA corresponding to Test Condition "f = f<sub>MAX</sub> = 1/t<sub>RC</sub>".</p> <p>Changed maximum value of I<sub>CC</sub> parameter from 2.3 mA to 3 mA corresponding to Test Condition "f = 1 MHz".</p> <p>Changed typical value of I<sub>SB1</sub> parameter from 0.9 µA to 2 µA.</p> <p>Changed maximum value of I<sub>SB1</sub> parameter from 4.5 µA to 8 µA.</p> <p>Changed typical value of I<sub>SB2</sub> parameter from 0.9 µA to 2 µA.</p> <p>Changed maximum value of I<sub>SB2</sub> parameter from 4.5 µA to 8 µA.</p> <p>Updated <a href="#">Thermal Resistance</a>:</p> <p>Updated values of <math>\Theta_{JA}</math>, <math>\Theta_{JC}</math> parameters corresponding to BGA package.</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a>:</p> <p>Updated <a href="#">Figure 2</a> (Changed Test Load Capacitance from 50 pF to 30 pF).</p> <p>Updated <a href="#">Data Retention Characteristics</a>:</p> <p>Added 1 µA as typical value for I<sub>CCDR</sub> parameter.</p> <p>Changed maximum value of I<sub>CCDR</sub> parameter from 4.5 µA to 3 µA.</p> <p>Changed minimum value of t<sub>R</sub> parameter from 100 µs to t<sub>RC</sub> ns.</p> <p>Updated <a href="#">Switching Characteristics</a>:</p> <p>Changed minimum value of t<sub>LZOE</sub> parameter from 3 ns to 5 ns.</p> <p>Changed minimum value of t<sub>LZCE</sub> parameter from 6 ns to 10 ns.</p> <p>Changed maximum value of t<sub>HZCE</sub> parameter from 22 ns to 18 ns.</p> <p>Changed minimum value of t<sub>LZBE</sub> parameter from 6 ns to 5 ns.</p> <p>Changed minimum value of t<sub>PWE</sub> parameter from 30 ns to 35 ns.</p> <p>Changed minimum value of t<sub>SD</sub> parameter from 22 ns to 25 ns.</p> <p>Changed minimum value of t<sub>LZWE</sub> parameter from 6 ns to 10 ns.</p> <p>Added Note 18 and referred the same note in t<sub>LZBE</sub> parameter.</p> <p>Updated <a href="#">Ordering Information</a>:</p> <p>Updated part numbers.</p> <p>Removed "Package Name" column.</p> <p>Added "Package Diagram" column.</p> <p>Updated <a href="#">Package Diagram</a>:</p> <p>spec 51-85150 – Changed revision from *B to *D.</p> <p>Updated to new template.</p>
*C	571786	12/01/2006	<p>Removed 45 ns Speed Bin related information in all instances across the document.</p> <p>Added 55 ns Speed Bin related information in all instances across the document.</p> <p>Updated <a href="#">Ordering Information</a>:</p> <p>Updated part numbers.</p>
*D	908120	04/04/2007	<p>Updated <a href="#">Electrical Characteristics</a>:</p> <p>Added Note 7 and referred the same note in I<sub>SB2</sub> parameter.</p> <p>Updated <a href="#">Switching Characteristics</a>:</p> <p>Added Note 15 and referred the same note in "Parameter" column.</p>

Document History Page (continued)

Document Title: CY62157EV18 MoBL, 8-Mbit (512K × 16) Static RAM			
Document Number: 38-05490			
Rev.	ECN No.	Submission Date	Description of Change
*E	2934396	06/03/2010	Updated <a href="#">Switching Characteristics</a> : Added Note 35 and referred the same note in "X" under $\overline{CE}_1$ and $CE_2$ columns. Updated <a href="#">Package Diagram</a> : spec 51-85150 – Changed revision from *D to *E. Updated to new template.
*F	3110053	12/14/2010	Changed Table Footnotes to Notes. Updated <a href="#">Ordering Information</a> : No change in part numbers. Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> : spec 51-85150 – Changed revision from *E to *F.
*G	3243545	04/28/2011	Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template. Completing Sunset Review.
*H	3295175	06/29/2011	Updated <a href="#">Electrical Characteristics</a> : Updated Note 7. Referred Note 7 in $I_{SB1}$ parameter. Updated <a href="#">Data Retention Characteristics</a> : Added Note 10 and referred the same note in $I_{CCDR}$ parameter. Updated <a href="#">Truth Table</a> : Updated Note 35.
*I	4102022	08/22/2013	Updated <a href="#">Switching Characteristics</a> : Updated Note 15. Updated <a href="#">Package Diagram</a> : spec 51-85150 – Changed revision from *F to *H. Updated to new template.
*J	4384935	05/20/2014	Updated <a href="#">Switching Characteristics</a> : Added Note 20 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 33 and referred the same note in <a href="#">Figure 8</a> . Completing Sunset Review.
*K	4576526	11/21/2014	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end.
*L	5759379	06/01/2017	Updated <a href="#">Thermal Resistance</a> values. Updated to new template. Completing Sunset Review.
*M	6819840	02/28/2020	Updated <a href="#">Features</a> : Updated description. Updated <a href="#">Product Portfolio</a> : Updated all values of "Operating $I_{CC}$ " corresponding to "f = 1 MHz". Updated <a href="#">Electrical Characteristics</a> : Updated all values of $I_{CC}$ parameter corresponding to "55 ns" and "f = 1 MHz". Updated <a href="#">Thermal Resistance</a> : Updated values of $\Theta_{JA}$ , $\Theta_{JC}$ parameters corresponding to BGA package. Updated <a href="#">Data Retention Characteristics</a> : Updated details in "Conditions" column and updated all values of $I_{CCDR}$ parameter. Updated <a href="#">Package Diagram</a> : spec 51-85150 – Changed revision from *H to *I. Updated to new template.

**Document History Page** (continued)

Document Title: CY62157EV18 MoBL, 8-Mbit (512K × 16) Static RAM			
Document Number: 38-05490			
Rev.	ECN No.	Submission Date	Description of Change
*N	7023434	11/13/2020	Updated <a href="#">Switching Characteristics</a> : Changed minimum value of $t_{WC}$ parameter from 45 ns to 55 ns. Changed minimum value of $t_{SCE}$ parameter from 35 ns to 40 ns. Changed minimum value of $t_{AW}$ parameter from 35 ns to 40 ns. Changed minimum value of $t_{PWE}$ parameter from 35 ns to 40 ns. Changed minimum value of $t_{BW}$ parameter from 35 ns to 40 ns. Changed maximum value of $t_{HZWE}$ parameter from 18 ns to 20 ns.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

Arm® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

#### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

#### Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

#### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2004–2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.