

AS5171

High-Resolution On-Axis Magnetic Angular Position Sensor

General Description

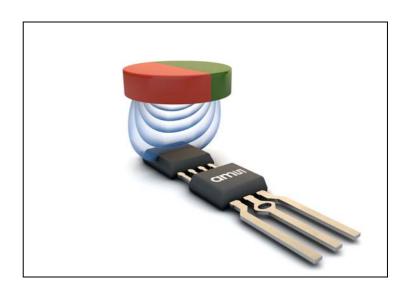
The AS5171 is a high-resolution angular position sensor for precise absolute angle measurement. The AS5171 is available with an analog output interface (AS5171A) or a digital output interface (AS5171B).

Based on a Hall sensor technology, this device measures the orthogonal component of the flux density (Bz) over a full-turn rotation and compensates for external stray magnetic fields with a robust architecture based on a 14-bit sensor array and analog front-end (AFE). A sub-range can be programmed to achieve the best resolution for the application. To measure the angle, only a simple two-pole magnet rotating over the center of the package is required. The magnet may be placed above or below the device. The absolute angle measurement provides an instant indication of the magnet's angular position. The AS5171 operates at a supply voltage of 5V, and the supply and output pins are protected against overvoltage up to +20V. In addition the supply pins are protected against reverse polarity up to -20V.

The AS5171A and AS5171B are available in a SIP package (System in Package). The package has integrated the AS5171 sensor die together with the decoupling capacitors necessary to pass system level ESD and EMC requirements. No additional components and PCB on the sensor side is needed. The product is defined as SEooC (Safety Element out of Context) according ISO26262.

Ordering Information and Content Guide appear at end of datasheet.

Figure 1:
Typical Arrangement of AS5171 and a Magnet





Key Benefits and Features

The benefits and features of this device are listed below:

Figure 2: Added Value of Using AS5171

| Benefits | Features |
|---|---|
| Resolve small angular excursion with high accuracy | 12-bit resolution @90° minimum arc |
| Accurate angle measurement | Low output noise, low inherent INL |
| Higher durability and lower system costs (no shield needed) | Magnetic stray field immunity |
| Enabler for safety critical applications | Functional safety, diagnostics, dual redundant chip version |
| Suitable for automotive applications | AEC-Q100 Grade 0 qualified |
| SIP Package (sensor + decoupling capacitors for ESD/EMC) | System cost reduction – no PCB and additional components are needed |

Applications

The AS5171 is ideal for automotive applications like:

- Brake and Gas Pedals
- Throttle Valve and Tumble Flaps
- Steering Angle Sensors
- Chassis Ride
- EGR
- Fuel-Level Measurement Systems
- 2/4WD Switch
- Contactless Potentiometers

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Block Diagram

The functional blocks of the AS5171A and AS5171B are shown below:

Figure 3: Functional Blocks of the AS5171A

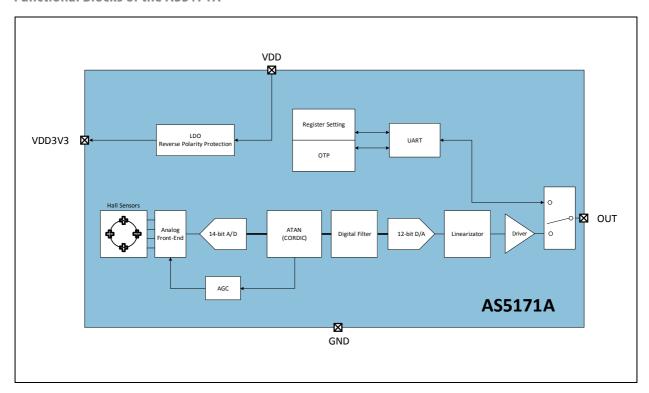
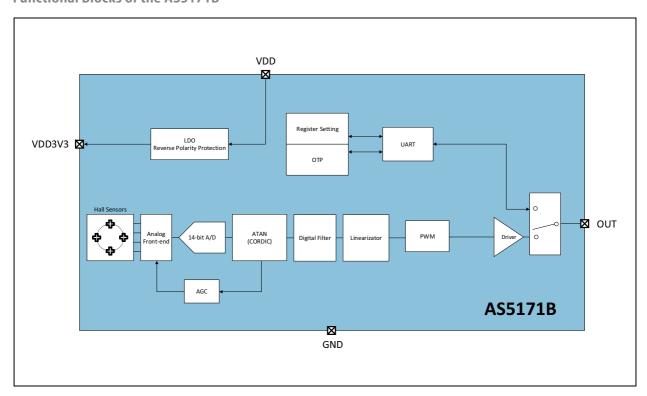


Figure 4: Functional Blocks of the AS5171B



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Pin Assignments

Figure 5: AS5171A/B Pin Assignment (Top View, SIP)

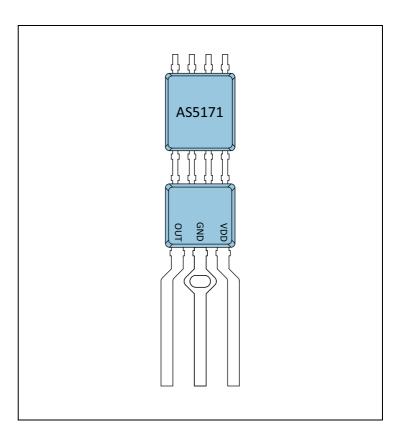


Figure 6: AS5171A/B Pin Description

| Pin # | Pin Name | Pin Type | Description | Comments |
|-------|----------|---|------------------|--|
| SIP | | | | |
| 1 | VDD | Supply | Positive supply | 5V supply – 100nF capacitor in SIP Body |
| - | TP1 | n.a. | Test pin | |
| - | TP2 | n.a. | Test pin | |
| - | TP3 | n.a. | Test pin | |
| 3 | OUT | Analog output (AS5171A) Digital output (AS5171B) | Output interface | 4.7nF capacitor in SIP Body |
| - | TP4 | n.a. | Test pin | |
| - | VDD3V3 | Supply | | 3.3V on-chip low-dropout (LDO) output. 100nF capacitor in SIP Body |
| 2 | GND | Supply | Ground | Connected to ground |

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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Comments |
|-------------------------------------|--|-------------|------------------------|---------|---|
| | Electri | cal Param | eters | | |
| VDD | DC Supply Voltage at VDD pin | -20 | 20 | V | Not operational |
| VOUT | External DC voltage at OUT pin | -0.3 | 20 | V | Permanent |
| VDIFF | DC voltage difference between VDD and OUT | -20 | 20 | V | |
| VREGOUT | DC voltage at the VDD3V3 pin | -0.3 | 5.0 | V | |
| I _{SCR} | Input Current (latch-up immunity) | -100 | 100 | mA | AEC-Q100-004 |
| | Continuous Power | Dissipati | on (T _{AMB} = | 70°C) | |
| P _T | Continuous power dissipation | | 66 | | Calculated with IDDmax=12mA; VDD=5.5V |
| | Electro | static Disc | harge | | |
| ESD _{HBM on} Chip level | Electrostatic discharge HBM | <u> </u> | -2 | kV | AEC-Q100-002 |
| ESD _{HBM} system | Electrostatic discharge HBM on VDD, Out and GND (outer connects) | ± | -4 | kV | AEC-Q100-002 |
| | Temperature Rang | es and Sto | orage Cond | litions | |
| T _{AMB} | Operating temperature range | -40 | 150 | °C | Ambient temperature |
| TaProg | Programming temperature | 5 45 | | °C | Programming@ Room temperature (25°C ± 20°C) |
| T _{STRG} | Storage temperature range | -55 | 150 | °C | |

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| Symbol | Parameter | Min | Max | Units | Comments |
|-------------------|----------------------------------|-----|-----|-------|--|
| T _{BODY} | Package body temperature | | 260 | °C | The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn) |
| RH _{NC} | Relative humidity non-condensing | 5 | 85 | % | |
| MSL | Moisture sensitivity level | | 3 | | Represents a maximum floor life time of 168 hours |

System Electrical and Timing Characteristics

All in this datasheet defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Overall condition: T_{AMB} = -40°C to 150°C, VDD=4.5V to 5.5V; Components spec; unless otherwise noted

Figure 8: Operating Conditions

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|--------|----------------------------|---|-----|------|-----|------|
| VDD | Positive supply voltage | | 4.5 | 5.0 | 5.5 | V |
| VREG | Regulated voltage | VDD3V3 should not be loaded by any external DC current | 3.3 | 3.45 | 3.6 | V |
| IDD_A | Supply current AS5171A | AGC=255 (no magnet placed); no output load; no short circiut | 4 | | 12 | mA |
| IDD_B | Supply current AS5171B | AGC=255 (no magnet placed); no output load; no short circiut | 4 | | 10 | mA |
| ISTART | Supply current at start-up | VREG = 2.25V | 2.5 | 5 | 10 | mA |
| TSUP | Start-up time | Functional mode | | | 10 | ms |

 T_{AMB} = -40°C to 150°C, VDD = 4.5 – 5.5V (5Voperation), Magnetic Characterization; unless otherwise noted

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Figure 9: Electrical System Characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------|-------------------------------------|--|------|-----|-----|------|
| CRES | Core resolution | | | | 14 | bit |
| ARES | Analog resolution (AS5171A) | Range > 90° | | | 12 | bit |
| DRES | Digital resolution (AS5171B) | | | | 12 | bit |
| INLopt | Integral non-linearity (optimum) | Best aligned reference magnet ⁽¹⁾ at 25°C over full turn 360° | -0.5 | | 0.5 | deg |
| INLtemp | Integral non-linearity (optimum) | Best aligned reference magnet ⁽¹⁾ over temperature -40°C to 150°C over full turn 360° | -0.9 | | 0.9 | deg |
| INL | Integral non-linearity | Best aligned reference magnet ⁽¹⁾ over temperature -40°C to 150°C over full turn 360° and displacement | -1.4 | | 1.4 | deg |
| ON | Output noise peak to peak | Static conditions - filter on | | | 1 | LSB |
| ST | Sampling time | | | 125 | | μs |

Note(s):

1. Reference magnet: NdFeB, 6 mm diameter, 2.5 mm thickness

Figure 10:
Power Management – Supply Monitor - Timing

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------|-------------------------------------|---|-----|-----|-----|------|
| VDDUVTH | VDD undervoltage upper threshold | | 3.5 | 4.0 | 4.5 | ٧ |
| VDDUVTL | VDD undervoltage lower threshold | | 3.0 | 3.5 | 4.0 | ٧ |
| VDDUH | VDD undervoltage hysteresis | | 300 | 500 | 900 | mV |
| UVDT | VDD undervoltage detection time | Time devices detects undervoltage VDD< VDDUVTH | 10 | 50 | 250 | μs |
| UVRT | Undervoltage recovery time | Time device return into normal mode from failure band VDD > VDDUVTH | 10 | 50 | 250 | μs |
| VDDOVTH | VDD overvoltage upper threshold | | 6.0 | 6.5 | 7.0 | V |

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| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------|-----------------------------------|---|-----|------|------|------|
| VDDOVTL | VDD overvoltage lower threshold | | 5.5 | 6.0 | 6.5 | V |
| VDDOH | VDD overvoltage hysteresis | | 300 | 500 | 900 | ٧ |
| OVDT | VDD overvoltage detection time | Time devices detects overvoltage VDD> VDDOVTL | 500 | 1000 | 2000 | μs |
| OVRT | VDD overvoltage recovery time | Time device return into normal mode from failure band VDD < VDDOVTL | 500 | 1000 | 2000 | μs |
| TDETWD | WatchDog error detection time | Time device detects oscillator failure till output is in failure band | | | 12 | ms |

 $T_{AMB} = -40 ^{\circ} C$ to 150 $^{\circ} C$, VDD = 4.5V to 5.5V, unless otherwise noted.

Two-pole cylindrical diametrically magnetized source:

Figure 11: Magnetic Characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------------------|--|---|-----|-----|-----|------|
| Bz | Orthogonal magnetic field strength | Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25 mm MFER = 0 | 30 | | 70 | mT |
| BzE | Orthogonal magnetic field strength – extended mode | Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25mm MFER = 1 | 10 | | 90 | mT |
| Disp ⁽¹⁾ | Displacement radius | Offset between defined device center and magnet axis. Dependent on the selected magnet. | | 0.5 | | mm |

Note(s):

1. Reference magnet: NdFeB, 6 mm diameter, 2.5 mm thickness

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Figure 12: Electrical and Timing Characteristics Analog Output (AS5171A)

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------------------|---|---|-------|-----|------|------|
| INLOS | INL output stage | | -6 | | +6 | LSB |
| DNLOS | DNL output stage | | -5 | | +5 | LSB |
| RERR ⁽¹⁾ | Ratiometricity error | Between 4% and 96% of VDD | -0.5% | | 0.5% | VDD |
| BVPU | Output voltage broken VDD with pull-up resistor | Pull-up resistor must be in the specified range (see Figure 32) | 96 | | 100 | %VDD |
| BGPD | Output voltage broken ground with pull-down resistor | Pull-down resistor must be in the specified range (see Figure 32) | 0 | | 4 | %VDD |
| OSSCG | Output short-circuit current GND | OUT = GND | -20 | -10 | -5 | mA |
| OSSCV | Output short-circuit current VDD | OUT = VDD | 5 | 10 | 20 | mA |
| OSSDT | Output short-circuit detection time | OUT = GND or OUT = VDD | 20 | 200 | 600 | μs |
| OSSRT | Output short-circuit recovery time | | 2 | 5 | 20 | ms |
| OLCH | Output level clamping high | Output current at OUT pin -3 mA | 96 | | | %VDD |
| OLCL | Output level clamping low | Output current at OUT pin 3 mA | | | 4 | %VDD |
| OSPSR | Output stage positive step response (driver only) | From 0 to 90%VDD, measured at OUT pin, with RPUOUT = 4.7kΩ, CLOAD = 1nF, VDD = 5V | | | 250 | μs |
| OSNSR | Output stage negative step response (driver only) | From VDD to 10%VDD, measured at OUT pin, with RPUOUT = $4.7k\Omega$, CLOAD = $1nF$, VDD = $5V$ | | | 250 | μs |
| OSTD | Output stage temperature drift | of value at mid code, info parameter not tested in production | -0.2 | | 0.2 | % |

Note(s):

- For each code the ratiometricity error is defined as follows: VOUTRATE=((VOUTact - (VOUTtyp*(VDDact/ VDDtyp)))/VDDtyp)*100 Where:
 - VOUTact is the actual output voltage
 - VOUTtyp is the typical output voltage
 - VDDact is the actual supply voltage
 - VDDtyp is the typical supply voltage

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Figure 13: Electrical and Timing Characteristics PWM Output (AS5171B)

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|----------|--|--|-------|------|-------|----------------------|
| PWMSSOCG | Short-circuit output current | OUT = GND | -20 | -10 | -5 | mA |
| PWMSSOCV | Short-circuit output current | OUT = VDD | 5 | 10 | 20 | mA |
| PWMSSDT | PWM short-circuit detection time | OUT = GND or OUT = VDD | | | 5 | % PWM clock cycle |
| PWMSSRT | PWM short circuit recovery time | | | 6 | | % PWM clock cycle |
| ВКРWMVOH | PWM output voltage high in broken condition | Broken VDD or broken GND, OUT = high, PWMVOH=VDD-VOUT RPU = $10k\Omega$ or RPD = $10k\Omega$ | 0 | | 0.4 | V |
| BKPWMVOL | PWM output voltage low in broken condition | Broken VDD or broken GND, OUT = low, RPU = $10k\Omega$ or RPD = $10k\Omega$ | 0 | | 0.4 | V |
| PWMF7 | PWM frequency | PWMFR = 111 | 112.5 | 125 | 137.5 | Hz |
| PWMF6 | PWM frequency | PWMFR = 110 | 180 | 200 | 220 | Hz |
| PWMF5 | PWM frequency | PWMFR = 101 | 225 | 250 | 275 | Hz |
| PWMF4 | PWM frequency | PWMFR = 100 | 360 | 400 | 440 | Hz |
| PWMF3 | PWM frequency | PWMFR = 011 | 450 | 500 | 550 | Hz |
| PWMF2 | PWM frequency | PWMFR = 010 | 720 | 800 | 880 | Hz |
| PWMF1 | PWM frequency | PWMFR = 001 | 900 | 1000 | 1100 | Hz |
| PWMF0 | PWM frequency | PWMFR = 000 | 1800 | 2000 | 2200 | Hz |
| PWMVOH | PWM output voltage level high | IOUT = 5 mA, PWMVOH = VDD - VOUT | 0 | | 0.4 | V |
| PWMVOL | PWM output voltage level high | IOUT = 5 mA | 0 | | 0.4 | V |
| PWMSRF | PMM slew rate fast | Between 25% and 75% of VDD, RPUOUT = $4.7k\Omega$, CLOUT1 = $4.7nF$, PWMSR = 0 | 1 | 2 | 4 | V/µs |

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| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|--------|--------------------|--|-----|-----|-----|------|
| PWMSRS | PMM slew rate slow | Between 25% and 75% of VDD, RPUOUT = $4.7k\Omega$, CLOUT1 = $4.7nF$, PWMSR = 1 | 0.5 | 1 | 2 | V/µs |

Figure 14: Electrical and Timing Characteristics UART Interface

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|--------------------------|--------------------------------|------------|---------|-----|------|------|
| UARTVIH | UART high level input voltage | | 70 | | | %VDD |
| UARTVIL | UART low level input voltage | | | | 30 | %VDD |
| UARTVOH | UART high level output voltage | | VDD-0.5 | | | V |
| UARTVOL | UART low level output voltage | | | | 0.5 | V |
| UARTBRLIM ⁽¹⁾ | UART baud rate | | 2400 | | 9600 | Baud |

Note(s):

1. Typ. error 1%. Indirect tested.

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Detailed Description

The AS5171 is a Hall-based rotary magnetic position sensor using a CMOS technology. The lateral Hall sensor array converts the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals coming from the Hall sensors are first amplified and filtered before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the CORDIC block (Coordinate-Rotation Digital Computer) to compute the angule and magnitude of the magnetic field vector. The sensor and analog front-end (AFE) section works in a closed loop alongside an AGC to compensate for temperature and magnetic field variations. The calculated magnetic field strength (MAG), the automatic gain control (AGC) and the angle can be read through the output pin (OUT) in UART mode.

The magnetic field coordinates provided by the CORDIC block are fed to a digital filter which reduces noise. A linearization block generates the transfer function, including linearization. The AS5171 is available with two different output interfaces: analog ratiometric (AS5171A) or digital PWM (AS5171B).

The output of the AS5171 can be programmed to define a starting position (zero angle) and a stop position (maximum angle). An embedded linearization algorithm allows reducing the system INL error due, for example, to mechanical misalignment, magnet imperfections, etc.

The AS5171 can be programmed through the OUTpin with a UART interface which allows writing an on-chip non-volatile memory (OTP) where the specific settings are stored. The AS5171 can be programmed by the **ams** programming tool, both at the component and board level.

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Register Description

The register description for AS5171A/B are explained below:

- Descriptions and Settings with Analog are supported by AS5171A
- Descriptions and Settings with PWM are supported by AS5171B

Figure 15: Non-Volatile Memory Register Description

| Address | Bit Position | Field | Description | |
|---------|--------------|---------|--|--|
| 0x0A | 7:0 | CUSTID0 | Customer ID byte 0 | |
| 0x0B | 7:0 | CUSTID1 | Customer ID byte 1 | |
| 0x0C | 7:0 | CUSTID2 | Customer ID byte 2 | |
| 0x0D | 7:0 | CUSTID3 | Customer ID byte 3 | |
| | 0 | PWMINV | PWM inverted | |
| | 1 | PWMSR | PWM slew rate (0 = PWM slew rate fast PWMSRF, 1 = PWM slew rate slow PWMSRS) | |
| 0x0E | 3:2 | DIGOS | Digital output stage (00 = PWM push-pull 01 = PWM pull-down 10 = PWM pull-up) It applies to the AS5171B only | |
| | 6:4 | RBKDEB | Analog read-back debouncing | |
| | 7 | n.a. | Not used | |
| | 0 | FBS | Failure band selection (0 = lower failure band, 1 = upper failure band) | |
| 0x0F | 2:1 | HYST | Hysteresis across the brake point | |
| | 4:3 | QUAD | Quadrant selection | |
| | 7:5 | PWMFR | PWM frequency selection | |
| | 1:0 | PWMRTH | PWM rising threshold tbd | |
| 0x10 | 3:2 | PWMFTH | PWM falling threshold tbd | |
| | 7:4 | n.a. | Not used | |
| | 4:0 | n.a. | Not used | |
| 0x11 | 5 | n.a. | Not used | |
| UAT I | 6 | n.a. | Not used | |
| | 7 | n.a. | Not used | |

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| Address | Bit Position | Field | Description | |
|---------|--------------|----------|--|--|
| 0x12 | 3:0 n.a | | No use. Default 0 | |
| 0.12 | 6:4 | n.a | No use. Default 0 | |
| 0x13 | 3:0 | n.a | No use. Default 0 | |
| 0.00.15 | 6:4 | n.a | No use. Default 0 | |
| 0x14 | 7:0 | CLMDII | Clamping level high | |
| 0x15 | 3:0 | CLMPH | Reg 0x14[0] =LSB Reg 0x15[3]=MSN | |
| SAL S | 7:4 | CLMPL | Clamping level low Reg 0x15[4] =LSB | |
| 0x16 | 7:0 | CLIVIPL | Reg 0x16[7]=MSN | |
| 0x17 | 7:0 | | Post processing offset | |
| 0x18 | 7:0 | PPOFFSET | Reg 0x17[0] =LSB Reg 0x19[3]=MSB | |
| 0x19 | 3:0 | | עבא מצו בו בו בו אום | |
| 0.19 | 7:4 | | Post processing gain | |
| 0x1A | 7:0 | PPGAIN | Reg 0x19[4] =LSB | |
| 0x1B | 4:0 | | Reg 0x1B[3]=MSB | |
| OXID | 7:5 | | Break point | |
| 0x1C | 7:0 | ВР | Reg 0x1B[5] =LSB Reg 0x1D[2]=MSB | |
| | 2:0 | | neg 0x1D[2]=NISB | |
| | 3 | MFER | Magnetic field extended range $(1 = Bz, 0 = BzE)$ | |
| 0x1D | 4 | AER | Angle extended range (set to 1 if the maximum angle excursion is smaller than 22 degree) | |
| | 6:5 | FILTER | Post processing filter | |
| | 7 | CUSLOCK | Customer settings lock | |
| 0x1E | 7:0 | SIGN | Signature | |

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Figure 16: Volatile Memory Register Description

| Address | Bit Position | Field | R/W | Description |
|---------|--------------|-------------|---------------------------|--|
| 0x22 | 7:0 | DAC12IN | R/W | Input word of the 12-bit output DAC |
| | 3:0 | DACIZIN | R/W | (Reg0x23[3] = MSB, Reg0x22[0] = LSB) |
| | 4 | DAC12INSEL | R/W | DAC 12 input buffer selection |
| 0x23 | 5 | DSPRN | R/W | Digital signal processing reset |
| | 6 | GLOAD | GLOAD R/W Enable of gload | |
| | 7 | - | - | Not used |
| 0x32 | 7:0 | ANGLECORDIC | R | Angle of the CORDIC output block. |
| 0x33 | 5:0 | ANGLLCONDIC | n | (Reg0x33[5] = MSB, Reg0x32[0] = LSB) |
| 0,33 | 7:6 | - | - | Not used |
| 0x34 | 7:0 | MAG | R | CORDIC magnitude |
| 0x35 | 7:0 | AGC | R | AGC value |
| 0x36 | 7:0 | ANGLEFILTER | R | Angle of the digital filter output block |
| 0x37 | 3:0 | ANGLEFILIER | n n | (Reg0x37[3] = MSB, Reg0x36[0] = LSB) |
| 0x37 | 7:4 | - | - | Not used |

Figure 17: Special Functions

| Address | Bit Position | Field | Description | | |
|---------|--------------|---------|--------------------------------|--|--|
| 0x60 | 7:0 | P2F | Pass-to-Function, see UART | | |
| 0x61 | 7:0 | 1 21 | Tass to Function, see OAIT | | |
| 0x62 | 7:0 | BURNOTP | Permanently burn OTP, see UART | | |
| 0x63 | 7:0 | BORNOTI | Termanently built on, see oakt | | |

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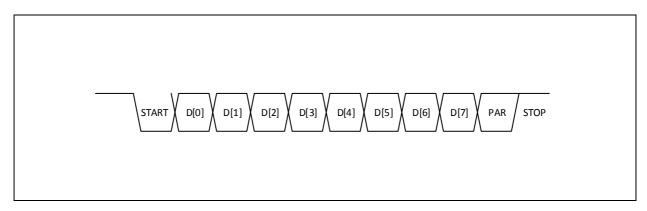


UART Interface

The AS5171 is equipped with a UART interface, which allows reading and writing the registers as well as permanently programming the non-volatile memory (OTP). By default (factory setting, customer_ lock = 0) the AS5171 is in the so-called *Communication Mode* and the UART is connected at the output pin (OUT). In this mode, the device is in open-drain mode and therefore a pull-up resistor has to be connected on the output.

The UART interface allows reading and writing two consecutive addresses. The standard UART sequence consists of four frames. Each frame begins with a start bit (START), which is followed by 8 data bits (D[0:7]), one parity bit (PAR), and a stop bit (STOP), as shown in Figure 18.

Figure 18: UART Frame



The PAR bit is even parity calculated over the data bits (D[0:7]). Each frame is transferred from LSB to MSB.

The four frames are shown in Figure 19.

Figure 19: UART Frame Sequence

| Frame Number | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|--------------|-------|---------|------|------|------|------|------|------|
| 1 | | 0x55 | | | | | | |
| 2 | R/W | ADDRESS | | | | | | |
| 3 | DATA1 | | | | | | | |
| 4 | DATA2 | | | | | | | |

The first frame is the synchronization frame and consists of D[0:7] = 0x55 followed by the parity bit (PAR=0) and the stop bit. This frame synchronizes the baud rate between the AS5171 and the host microcontroller.

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The second frame contains the read/write command (D[7] = 0 Write, D[7] = 1 Read) and the address of the register (D[6:0] = ADDRESS).

The content of the third and fourth frames (DATA1 and DATA2) will be written to or read from the location specified by ADDRESS and ADDRESS+1, respectively.

Figure 20 and Figure 21 show examples of read and write.

Figure 20: Example of Write (Reg[0x22] = 0x18, Reg[0x23] = 0xA2)

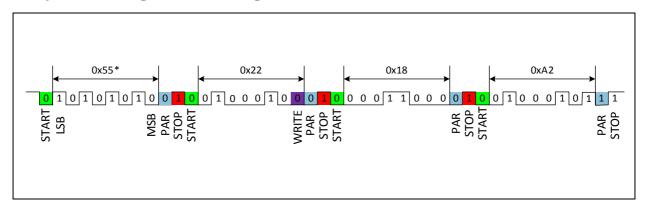
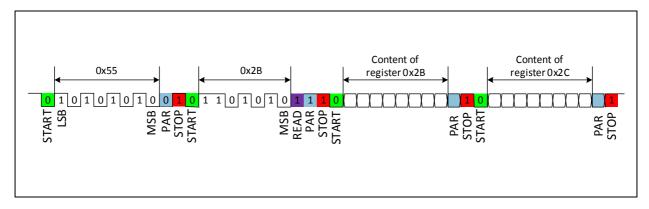


Figure 21: Example of Read (Reg[0x2B], Reg[0x2C])



Exiting Communication Mode

Communication mode is exited and operational mode is entered with a Pass-to-function (P2F) command, by writing to the virtual registers 0x60 and 0x61:

P2F: write(0x60) = 0x70, write(0x61) = 0x51

No more commands can be sent after sending this command, because the device is permanently placed in operational mode.

Programming OTP Registers

The BURNOTP command writes the OTP registers with their programmed values. The command is issued by writing to virtual registers 0x62 and 0x63:

BURNOTP: write(0x62) = 0x70, write(0x63) = 0x51.

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Customer ID

A specific identifier chosen by the user can be stored in the non-volatile memory. This identifier consists of 4 bytes and can be stored in the locations CUSTID0, CUSTID1, CUSTID2, and CUSTID3.

Output Linear Transfer Function

A linear transfer function controls the state of the output in response to the absolute orientation of the external magnet. The parameters which control this function are shown in Figure 22.

To calculate this settings into the corresponding sensor settings, **ams** provides a programming tool, specific DLL or the complete source code. For more information, please contact **ams**.

Figure 22: Transfer Function Control Parameters

| Symbol | Parameter | Resolution [bit] |
|--------|-----------------------------------|------------------|
| T1 | Mechanical angle starting point | 14 |
| T2 | Mechanical angle stop point | 14 |
| OT1 | Output at the starting point (T1) | 12 |
| OT2 | Output at the stop point (T2) | 12 |
| CLMPL | Clamping level low | 12 |
| CLMPH | Clamping level high | 12 |
| ВР | Breakpoint | 14 |

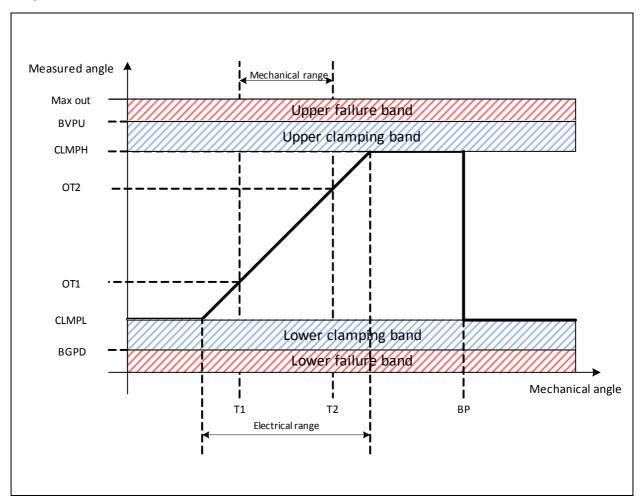
As shown in the Figure 23, the parameters T1, T2, OT1, and OT2 define the input-to-output linear transfer function. The dedicated programmer for the AS5171 uses the parameters from Figure 22 to generate the corresponding settings CLMPL, CLMPH, PPOFFSET, PPGAIN and BP (see Figure 23).

The clamping level parameters CLMPL and CLMPH define the absolute minimum and maximum level of the output. Both clamping levels can be set with the 12 LSBs out of the 12-bit output resolution. CLMPL and CLMPH must always be set outside of the lower and upper diagnostic failure band defined by the output broken wire voltage (see Figure 23: BGPD and BVPU).

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Figure 23: Output Transfer Function



The breakpoint BP sets the discontinuity point where the output jumps from one clamping level to the other. It is strongly recommended to set the breakpoint at the maximum distance from the start and stop position (T1 and T2). To handle the case of a full turn, a hysteresis function across the breakpoint can be used to avoid sudden jumps between the lower and upper clamping level.

Figure 24: Hysteresis Setting

| HYST | Hysteresis LSBs |
|------|-----------------|
| 00 | 0 |
| 01 | 56 |
| 10 | 91 |
| 11 | 137 |

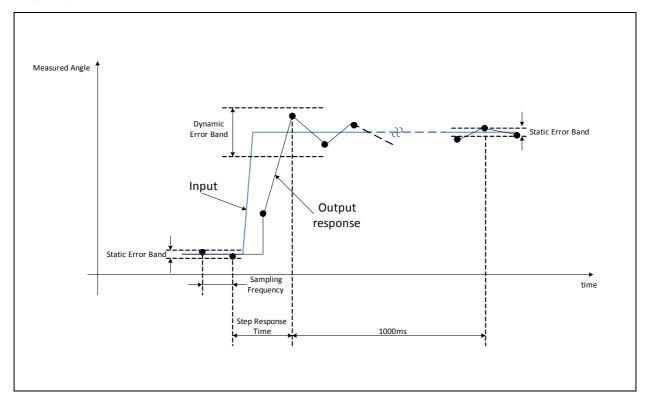
The hysteresis LSB is based on the core resolution (14-bit).

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The AS5171 features a programmable digital filter. As shown in Figure 25 in a static condition (no change of the input), the static error band is ± 0.5 LSB (at 12-bit resolution). Whenever an input step occurs, the output (measured angle) follows the input (mechanical angle) entering a certain error band within the step response time. From the time when the output is within the static error band the output takes 1000 ms to settle to the static error band achieving again ± 0.5 LSB output noise. The filter is not usable in 360° range, if the Hysteresis setting is on.

Figure 25: Step Response



It is possible to optimize the step response time versus the dynamic error band with the FILTER setting.

Figure 26: FILTER Setting

| FILTER | Dynamic Error Band [LSB] | Step Response Time [µs] |
|--------|--------------------------|----------------------------|
| 00 | Filter off | Not applicable |
| 01 | 23 | 5 CORDIC cycles |

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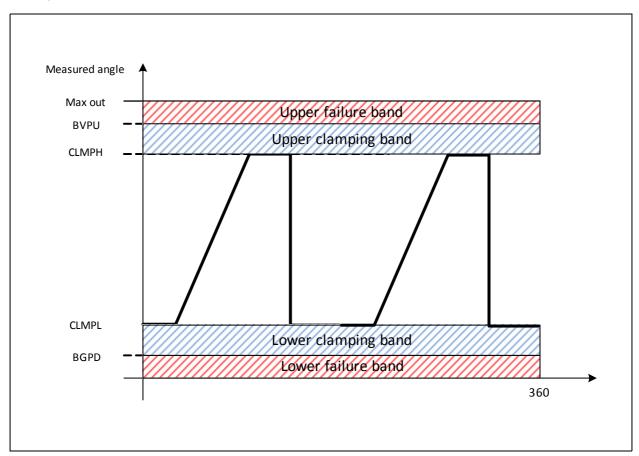
Multiple Quadrants

The multiple quadrants option allows repeating the same output control parameters up to 4 times over the full turn rotation as shown in the Figure 28, Figure 29, and Figure 30. The QUAD parameter sets the number of quadrants, as shown in the Figure 27.

Figure 27: Number of Quadrants

| QUADEN | Number of Quadrants | | |
|--------|---------------------|--|--|
| 00 | Single | | |
| 01 | Double | | |
| 10 | Triple | | |
| 11 | Quadruple | | |

Figure 28: Dual Quadrant Mode



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Figure 29: Triple Quadrant Mode

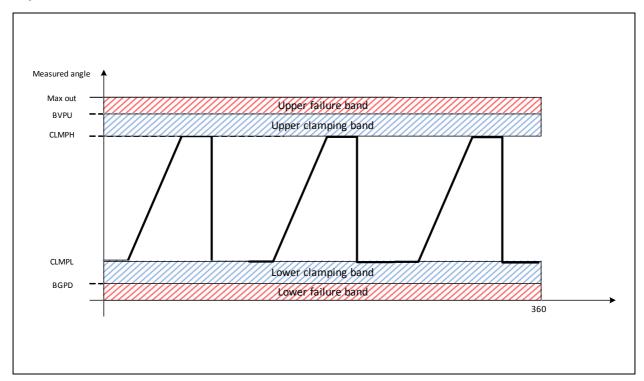
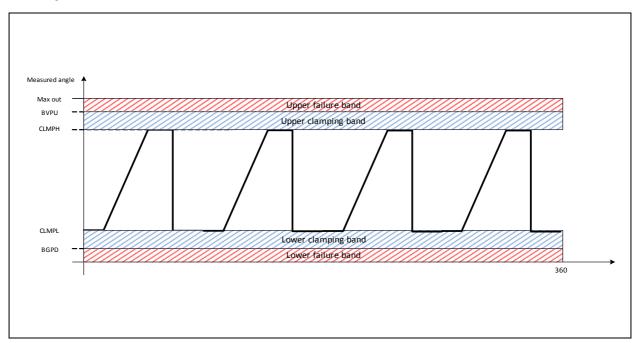


Figure 30: Quadruple Quadrant Mode



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Extended Magnetic Input Range

The magnetic input field range can be boosted with the MFER bit. The extended magnetic field allows increasing the maximum air gap between the AS5171 and the magnet.

Analog Output (AS5171A)

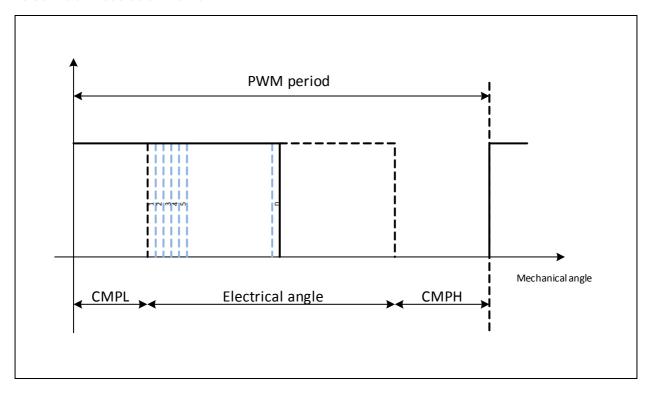
The AS5171A provides a linear analog ratiometric output signal. The output buffer features a push-pull analog output stage which can be loaded with a pull-down or a pull-up resistor. The output voltage represents the angular orientation of the magnet above the AS5171A on a linear absolute scale and is ratiometric to VDD.

PWM Output (AS5171B)

The AS5171B has a PWM output. With the DIGOS setting, the PWM output stage can be programmed as a push-pull, pull-down, or pull-up driver. The duty-cycle of each pulse is proportional to the absolute angular position of the external magnet.

The PWM signal consists of a frame of 4096 clock periods as shown in Figure 31. The PWM frame begins with a certain number of clocks high, defined by the CLMPL, which is followed by the electrical angle information. The frame ends with a certain number of clock pulses low, as defined by the CLMPH. It is possible to invert the frame using the PWMINV setting.

Figure 31:
Pulse Width Modulation Frame



The PWMFR setting sets the duration of the PWM frequency. The PWMSR setting chooses between fast and slow steps.

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Diagnostic and Functional Safety

AS5171 can be used in safety critical applications. For this reason, AS5171 is developed as SEooC (Safety element out of context) according the ISO26262, which assumed safety goals and assumed ASIL level.

The assumption of use (AoU) and the robust embedded self-diagnostic, to achieve a high ASIL level in the application, are described in the AS5171 safety manual.

For additional information regarding the ISO26262 flow at **ams** and the SEooC relevant documents (e.g. FMEDA, safety manual,) please contact the **ams** technical support for magnetic position sensors.

Figure 32: Diagnostic Table

| SM | Safety Mechanism | Recoverable | Safe State |
|------|--|---|---|
| SM1 | Watchdog failure | No, if a watchdog error is detected, the sensor provides the error information till a sensor reset happens | Output is going into HIZ> failure band (depending on output resistor) |
| SM2 | Offset compensation not complete | Yes, if the offset is below the specified threshold, sensor recovers the output | Output is forced in failure band. Depending on FBS setting |
| SM3 | CORDIC overflow | Yes, if the magnetic input field is below the specified threshold, sensor recovers the output | Output is forced in failure band. Depending on FBS setting |
| SM4 | Magnetic input field too high/too low | Yes, if the magnetic field is inside the specific range, after the recovery time the sensor leave the failure | Output is forced in failure band. Depending on FBS setting |
| SM5 | Vreg undervoltage | Yes | Hi-z: Failure band related to the out load |
| SM6 | Reverse polarity | Yes, if reverse polarity issue is solved. No direct safety mechanism, it's a protection! | Hi-z: Failure band related to the out load |
| SM7 | VDD overvoltage | Yes, if the VDD is below the specified threshold. | Hi-z: Failure band related to the out load |
| SM8 | VDD undervoltage | Yes, if the VDD is above the specified threshold | Hi-z: Failure band related to the out load |
| SM9 | Broken VDD | Yes | Hi-z: Failure band related to the out load |
| SM10 | ADC check | No, sensor stays in failure band till the Sensor is resetting. | Hi-z: Failure band related to the out load |
| SM11 | Analog read fail | Yes | Hi-z: Failure band related to the out load |
| SM12 | Short circuit | Yes | Hi-z: Failure band related to the out load |

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| SM | Safety Mechanism | Recoverable | Safe State |
|------|------------------|---|--|
| SM13 | Signature | No, sensor stays in failure band till the sensor is resetting | Hi-z: Failure band related to the out load |
| SM14 | Broken GND | Yes | Hi-z: Failure band related to the out load |

The FBS setting allows selecting the failure band (lower or upper) when the output goes into diagnostic mode.

Diagnostic Explanations

For a detailed explanation of the diagnostic and the SPFM please contact the **ams** application team for magnetic position sensor.

Analog Read Fail (SM11)

This safety mechanism operates differently for AS5171A (analog) and AS5171B (digital):

For AS5171B readout failure: After a falling edge there
must be a rising edge after a defined time.
 In case this is not respected output driver is kept in high
impedance. After a certain time this condition is checked
again.

The readout mechanism for AS5171B is defined by PWMRTH and PWMFTH, which set the maximum timeout period to wait for a falling/rising before triggering an error condition, according to the figures below.

Figure 33: PWMRTH Conditions

| PWMRTH | | Delay (μs) |
|--------|---|-----------------------------|
| 0 | 0 | PWM Read Back rise disabled |
| 0 | 1 | 24-28 |
| 1 | 0 | 56-60 |
| 1 | 1 | 112-120 |

Figure 34: PWMFTH Conditions

| PWMFTH | | Delay (μs) | |
|--------|---|-----------------------------|--|
| 0 | 0 | PWM Read Back fall disabled | |
| 0 | 1 | 24-28 | |
| 1 | 0 | 56-60 | |
| 1 | 1 | 112-120 | |

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• For AS5171A readout failure: Comparison of the analog output information versus the digital information of the sensor. If the difference is too high output driver is kept in high impedance. After a certain time this condition is checked again.

The readout mechanism for AS5171A is defined by RDBCKDEB, which set the maximum timeout period to wait before triggering an error condition, according to the tables below.

Figure 35: AS5171A Readout Mechanisms

| RDBCKDEB02 | RDBCKDEB01 | RDBCKDEB00 | CORDIC Cycles ⁽¹⁾ | Note |
|------------|------------|------------|---------------------------------|---------------------------|
| 0 | 0 | 0 | 0 | Analog Read Back disabled |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 2 | |
| 0 | 1 | 1 | 4 | |
| 1 | 0 | 0 | 8 | |
| 1 | 0 | 1 | 16 | |
| 1 | 1 | 0 | 32 | |
| 1 | 1 | 1 | 64 | |

Note(s):

1. 1 CORDIC cycle typ.:111µs

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Application Information

Signature Calculation

The OTP of AS5171A and AS5171B uses a BIST technique with Multiple Input Signature Register circuits.

To activate this BIST a calculation of the Signature Byte is necessary and has to store into the OTP during the programming sequence.

For calculating the signature byte the content of the whole memory (0x02 to 0x1D) has to be read.

Out of this information the following calculation has to be done.

Byte: 0x02 = data2Byte: 0x1D = data29

```
Unsigned int signature (unsigned int * content)
unsigned int misr,misr_shift,misr_xor,misr_msb;
misr = 0;
for (int i=0; i<28; i++) {
misr_shift = (misr<<1);
misr_xor = (misr_shift ^ content[i])%256;
misr_msb = misr/(128);
if (misr_msb == 0)
misr = misr_xor;
else
misr = (misr_xor ^ 29)%256;
return misr;
content= {,data2,data3,data4,data5,data6,
          data7,data8,data9,data10,data11,
          data12,data13,data14,data15,data16,
          data17,data18,data19,data20,data21,data22,
          data23,data24,data25,data26,data27,data28,data29};
```

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Programming Parameter

The programming has to be performed in communication mode. If the cust_lock=0, the sensor starts in communication mode.

The following procedure and the block diagram are showing the common 2 point calibration. For special calibration procedure:

AS5171A: Analog output driver calibration

AS5171A/AS5171B: Linearization.

Please go in contact with the ams application team.

Burn and Verification of the OTP Memory

- 1. Power on cycle
- 2. Move magnet to the first mechanical start position
- 3. Reset the DSP. Writing 0x20 into Reg(0x0023)
- 4. Read out the measured angle from ANGLECORDIC register: T1 Value
- 5. Moving of magnet to the second mechanical position (stop position)
- 6. Read out the measured angle from ANGLECORDIC register: T2 Value
- 7. Write T1,T2 and all other transfer parameter into the DLL: Calculation of GAIN, Offset, BP, Clamping
- 8. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7. --> AS5171 Settings
- Read reg(0x000A) to reg (0x001E) ---> Read register step 1
- 10. Comparison of AS5171 settings with content of read register step 1
- 11. If point 10 is correct: Decision: pass 2 function (measurement verification) or programming. Programming sequence starts with point 12.
- 12. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7 + customer lock Bit. --> AS5171 Settings_Prog
- 13. Read reg(0x0000) to reg (0x001D) ---> Read register step 2
- 14. Calculation of Signature Byte out of Read register step2 content: Signature Byte
- 15. Write 8Bit Signature to reg(0x001E)
- 16. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7 + customer lock Bit + Signature byte. --> AS5171 Settings_ Prog_final

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- 17. Read reg(0x000A) to reg (0x001E) ---> Read register step 3
- 18. Comparison of AS5171 Settings_Prog_final with content of read register step 3
- 19. If point 18 is correct, start the OTP burn procedure by writing: Reg(0x0062)=0x70 and Reg(0x0063)=0x51
- 20. Programming procedure is complete after 10ms
- 21. Clear the memory content writing 0x00 into reg (0x001E)
- 22. Write Reg0x23=0x40 to set the threshold for the guard band test (1)
- 23. 5ms wait time to refresh the non-volatile memory content with the OTP content
- 24. Read reg(0x000A) to reg (0x001E) ---> Read register step 4
- 25. If content from reg (0x001E) compares with content from "Signature Byte" refresh was successful
- 26. Comparison of AS5171 Settings_Prog_final with content of read register step 4. Mandatory: guard band test (1).
- 27. If point 26 fails, the test with the guard band (1) was not successful and the device is incorrectly programmed. A reprogramming is not allowed.
- 28. Clear the memory content writing 0x00 into reg (0x001E)
- 29. Write Reg0x23=0x00to set the threshold for the guard band test (1)
- 30. 5ms wait time to refresh the non-volatile memory content with the OTP content
- 31. Read reg(0x000A) to reg (0x001E) ---> Read register step 5
- 32. If content from reg (0x001E) compares with content from "Signature Byte" refresh was successful
- 33. Comparison of AS5171 Settings_Prog_final with content of read register step 5. Mandatory: guard band test (1)
- 34. If point 33 fails, the test with the guard band (1) was not successful and the device is incorrectly programmed. A reprogramming is not allowed.
- 35. Reset of the device. After power on the Sensor starts in functional mode

Note(s):

1. Guard band test:

Restricted to temperature range: 25 °C \pm 20 °C

Right after the programming procedure (max. 1 hour with same

Conditions 25°C ± 20 °C)

Same VDD voltage

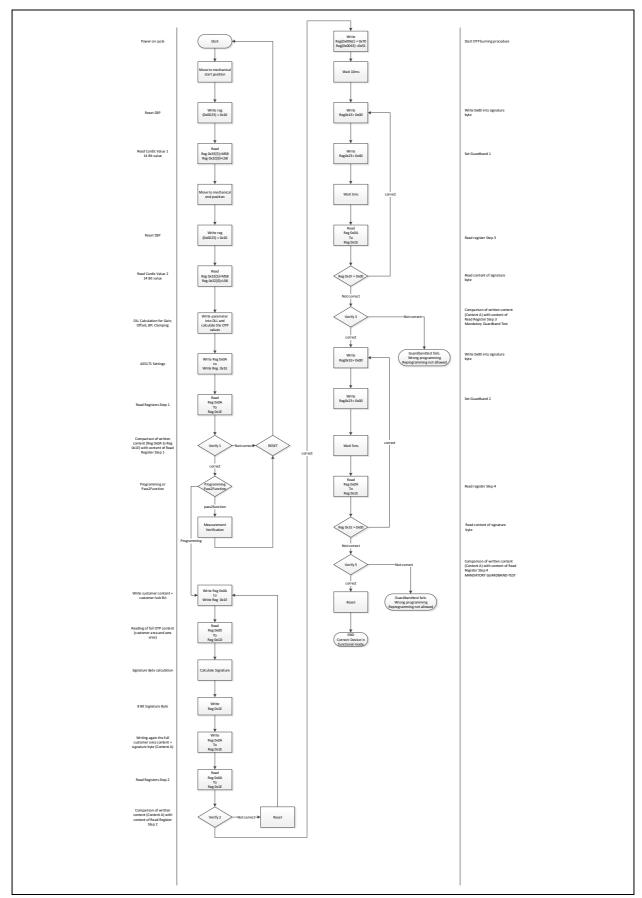
The guard band test is only for the verification of the burned OTP fuses during the programming sequence.

A use of the guard band in other cases is not allowed.

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Figure 36: OTP Memory Burn and Verification Flowchart



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Recommended Application Diagrams and Built-In Capacitors

Figure 37:
Application with Pull-Down Load Resistor

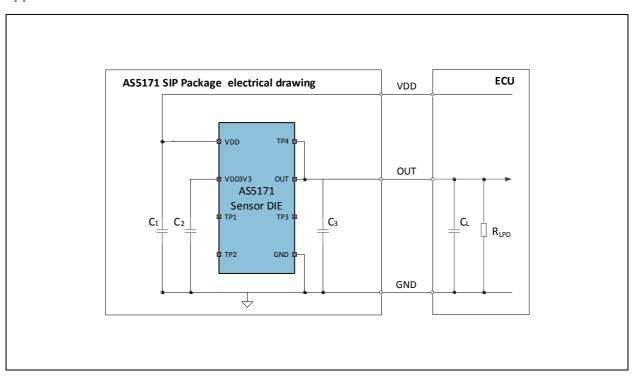
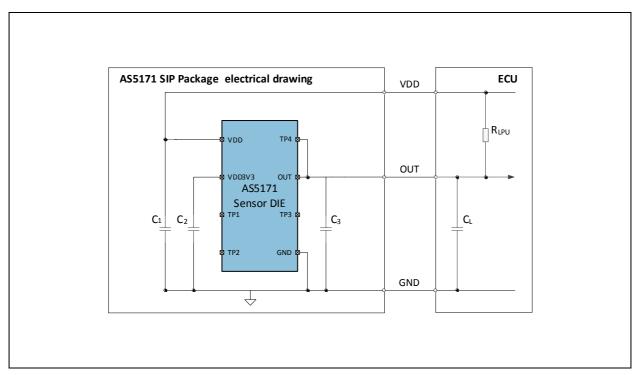


Figure 38:
Application with Pull-Up Load Resistor

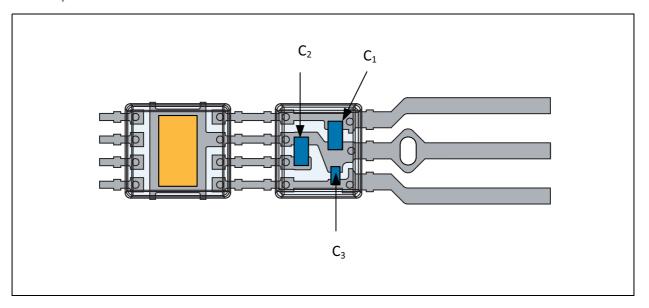


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Figure 37 and Figure 38 show the recommended schematic in the application. C1, C2 and C3 are Built-in capacitors in the SIP Package as shown in Figure 43.

Figure 39: SIP Components



The built-in capacitors are ceramic multilayer type X8R. The capacitors build for high temperature applications up to 150°C

Components Spec

Figure 40: SIP Components and Recommended ECU Components for AS5171A

| Component | Symbol | Min | Тур | Max | Unit | Notes |
|---------------------------------|------------------|---------|------|------|------|---------------------|
| | SI | P Compo | nent | | | |
| VDD buffer capacitor | C ₁ | 90 | 100 | 110 | nF | Included in the SIP |
| VDD3V3 regulator capacitor | C ₂ | 90 | 100 | 110 | nF | Included in the SIP |
| OUT load capacitor (sensor PCB) | C ₃ | 4,23 | 4.7 | 5,17 | nF | Included in the SIP |
| ECU Component | | | | | | |
| OUT load capacitor (ECU) | C _L | 0 | | 33 | nF | |
| OUT pull-up resistance | R _{LPU} | 4 | | 10 | kΩ | |
| OUT pull-down resistance | R _{LPD} | 4 | | 10 | kΩ | |

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Figure 41: SIP Components and Recommended ECU Components for AS5171 B With PWM

| Component | Symbol | Min | Тур | Max | Unit | Notes | |
|---------------------------------|------------------|------|-----|------|------|---------------------|--|
| SIP Component | | | | | | | |
| VDD buffer capacitor | C ₁ | 90 | 100 | 110 | nF | Included in the SIP | |
| VDD3V3 regulator capacitor | C ₂ | 90 | 100 | 110 | nF | Included in the SIP | |
| OUT load capacitor (sensor PCB) | C ₃ | 4,23 | 4.7 | 5,17 | nF | Included in the SIP | |
| ECU Component | | | | | | | |
| OUT load capacitor (ECU) | C _L | 0 | | 33 | nF | | |
| OUT pull-up resistance | R _{LPU} | 1 | | 10 | kΩ | | |
| OUT pull-down resistance | R _{LPD} | 1 | | 10 | kΩ | | |

Information Regarding Manufacturability of AS5171A and AS5171B

For the SIP Package which is used for AS5171A and AS5171B, please refer to the following document (available upon request):

Application Note SIP Dual Mold Package

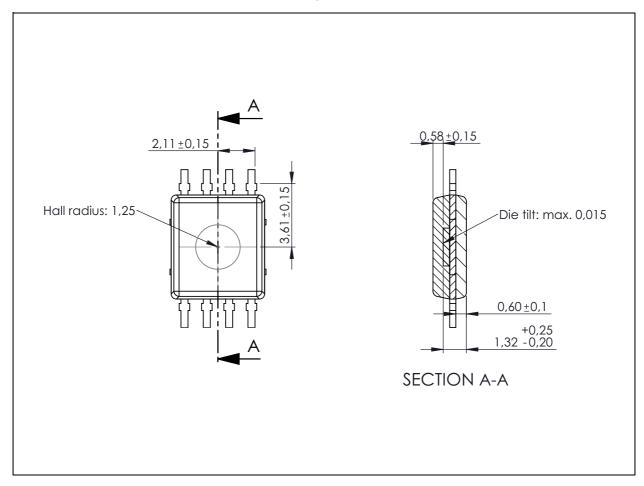
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Mechanical Data

The internal Hall elements are placed in the center of the header package on a circle with a radius of 1.25mm.

Figure 42: Hall Element Positions in the Header of SIP Package



Note(s):

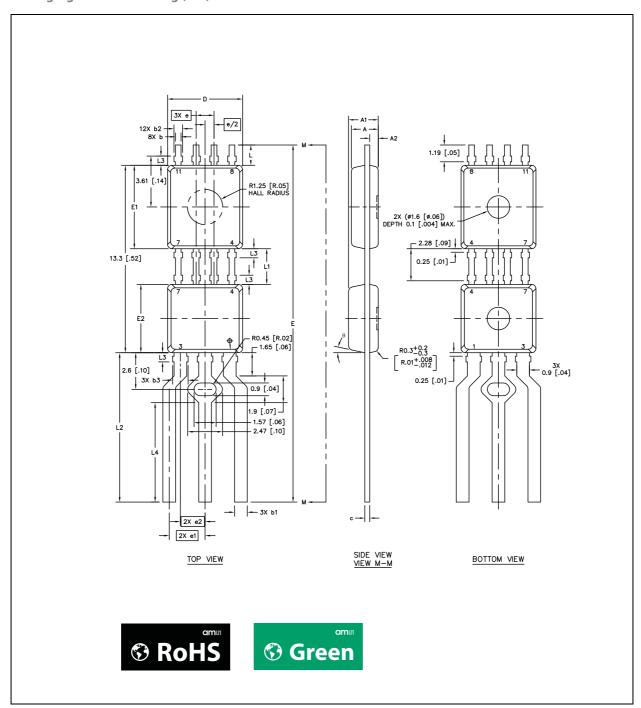
- 1. All dimensions in mm.
- 2. Tolerances shown represent expected values and are to be verified. Tolerances will be guaranteed prior to product release.

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Package Drawings & Markings

Figure 43: Packaging Outline Drawing (SIP)



Note(s):

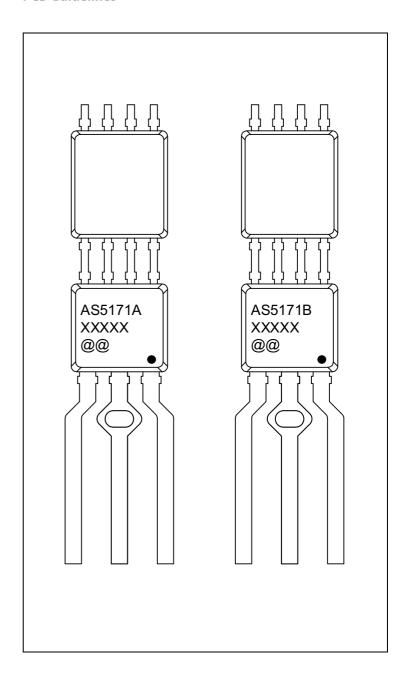
- 1. All dimensions are nominal are in millimeters.
- 2. Tolerances shown represent expected values and are to be verified. Tolerances will be guaranteed prior to production release.
- 3. Ejector pin marks with max. depth 0.1 mm to be expected on the package backside.
- 4. Dimensions of molded parts do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.3mm.
- $5. \, Dimensions \, of \, molded \, parts \, do \, not \, include \, interlead \, flash \, or \, protrusion. \, Interlead \, flash \, or \, protrusion \, shall \, not \, exceed \, 0.3 \, mm \, per \, side.$
- 6. Lead dimensions do not include dam bar protrusion and matte tin plating. Allowable dam bar protrusion shall be 0.3mm in excess of the lead dimension.
- 7. Dimension tolerance: ±0.15mm unless otherwise noted.

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Marking

Figure 44: PCB Guidelines



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Figure 45: Package Marking

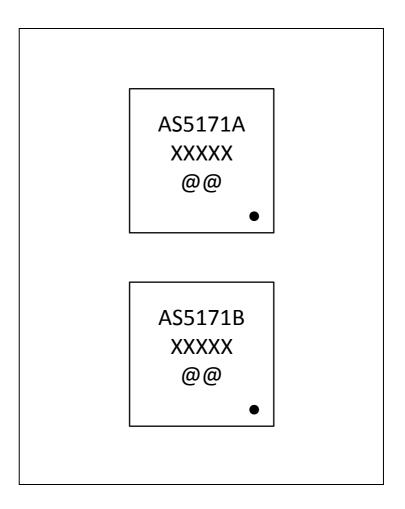


Figure 46: Packaging Code

| XXXXX | @@ |
|----------------|-------------------|
| TC_5 Tracecode | Sublot Identifier |

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Ordering & Contact Information

Figure 47: Ordering Information

| Ordering Code | Package | Marking | Delivery Form | Delivery Quantity |
|---------------|---------|---------|-----------------------------|-------------------|
| AS5171A-HSIT | SIP | AS5171A | 13" Tape & Reel in dry pack | 2000 pcs/reel |
| AS5171B-HSIT | SIP | AS5171B | 13" Tape & Reel in dry pack | 2000 pcs/reel |

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Document Status

| Document Status | Product Status | Definition |
|--------------------------|-----------------|--|
| Product Preview | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
| Preliminary Datasheet | Pre-Production | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice |
| Datasheet | Production | Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade |
| Datasheet (discontinued) | Discontinued | Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs |

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Revision Information

| Changes from 1-03 (2016-Jun-23) to current revision 1-04 (2017-Feb-21) | Page |
|--|------|
| Updated Figure 5 | 4 |
| Updated Figure 39 | 32 |
| Updated Figure 43 | 35 |

Note(s):

- 1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- $2. \, Correction \, of \, typographical \, errors \, is \, not \, explicitly \, mentioned.$

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