IS32FL3207

18-CHANNEL LED DRIVER WITH 16-BIT PWM

May 2024

GENERAL DESCRIPTION

IS32FL3207 is an LED driver with 18 constant current channels. Each channel can be pulse width modulated (PWM) by 16 bits for smooth LED brightness control. In addition, each channel has an 8-bit output current control register which allows fine tuning the current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel can be adjusted by one 8-bit global control register.

Proprietary programmable algorithms are used in IS32FL3207 to minimize audible noise caused by the MLCC decoupling capacitor. All registers can be programmed via a high speed I2C (1MHz).

IS32FL3207 can be turned off with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature.

IS32FL3207 is available in WFQFN-28 (5mm × 5mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- 2.7V to 5.5V supply
- Accuracy between channels and ICs: <±6% (Max.)
- I2C interface, automatic address increment function
- Four selectable I2C addresses
- Accurate color rendition
  - Selectable 8-bit/10-bit/12-bit/16-bit PWM
  - 8-bit dot correction
  - 8-bit global current adjust
- Open/Short detect function
- 62kHz PWM frequency (8-bit PWM)
- Temperature detect function
- EMI/noise reduction technology
  - Spread spectrum
  - Selectable Phase Delay
  - Selectable 180 degree Clock Phase
- -40°C to +125°C temperature range
- WFQFN-28 (5mm × 5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C

APPLICATIONS

- Automotive clusters
- Dashboards
- Automotive interiors
- Ambient lighting
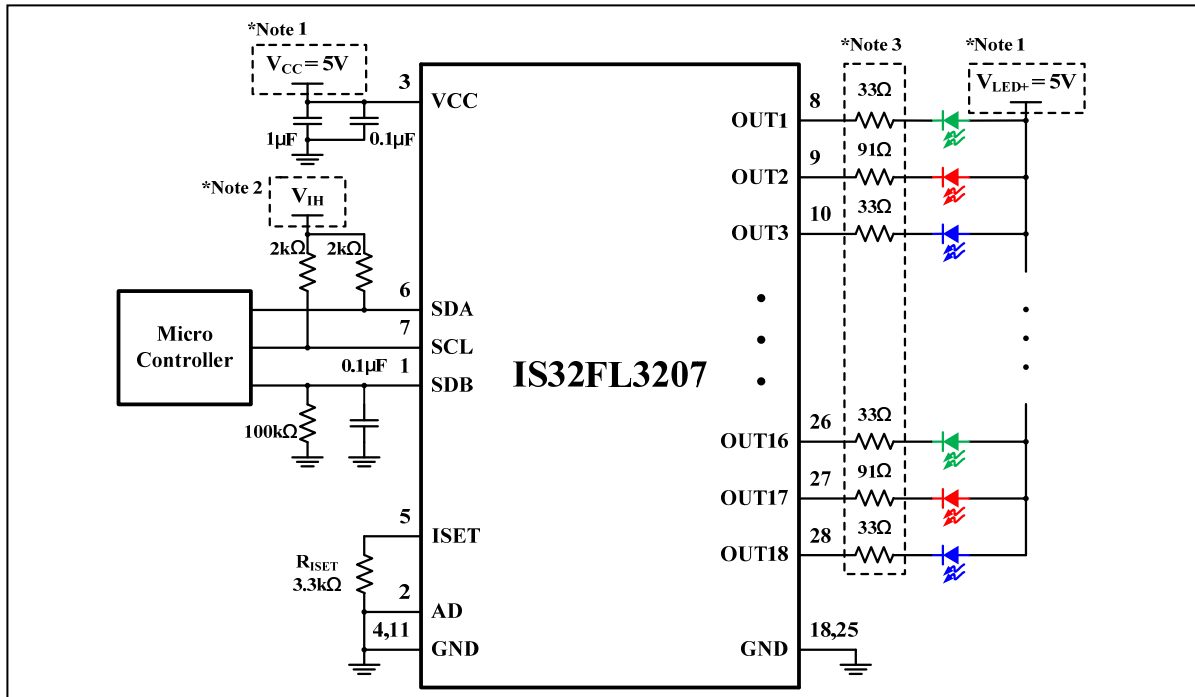- Functional lighting

TYPICAL APPLICATION CIRCUIT

Figure 1 Typical Application Circuit (V_{CC}= 5V)

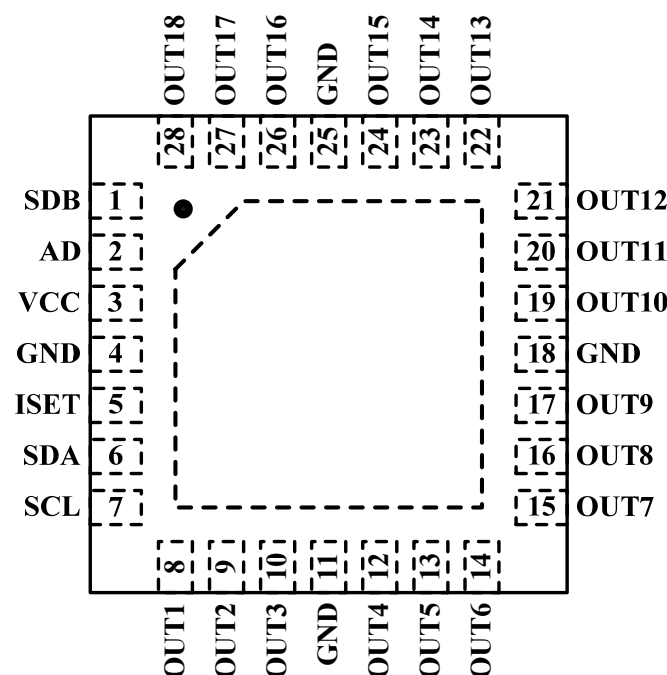**Note 1**: V_{LED+} should be same as VCC voltage.

Note 2: V_{IH} is the high level voltage for IS32FL3207, which is usually same as V_{CC} of Micro Controller, e.g. if V_{CC} of Micro Controller is 3.3V, V_{IH}=3.3V. If V_{CC}=5V and V_{IH} is lower than 2.8V, recommend to add a level shift circuit for SDA and SCL.

Note 3: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS32FL3207.

Note 4: The maximum global output current is set up to 23mA when R_{ISET}= 3.3kΩ. The maximum global output current can be set by external resistor, R_{ISET}. Please refer to the detail application information in R_{ISET} section.

Note 5: The IC and LED should be placed far away from the antenna in order to prevent the EMI.

IS32FL3207

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WFQFN-28	

PIN DESCRIPTION

No.	Pin	Description
1	SDB	Shutdown the chip when pulled low.
2	AD	I2C address setting.
3	VCC	Power supply.
4,11, 18,25	GND	Ground.
5	ISET	Input terminal used to connect an external resistor. This regulates the global output current.
6	SDA	I2C serial data.
7	SCL	I2C serial clock.
8~10	OUT1~OUT3	Output channel 1~3 for LEDs.
12~17	OUT4 ~ OUT9	Output channel 4~9 for LEDs.
19~24	OUT10 ~ OUT15	Output channel 10~15 for LEDs.
26~28	OUT16 ~ OUT18	Output channel 16~18 for LEDs.
	Thermal Pad	Connect to GND.

IS32FL3207

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32FL3207-QWLA3-TR	WFQFN-28, Lead-free	2500

IS32FL3207

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at SCL, SDA, SDB, OUT1 to OUT18	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, $T_A=T_J$	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	38.7°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-2A), θ_{JP}	2.02°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 6: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Typical values are T_A = 25°C, V_{CC} = 5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{OUT}	Maximum output current	V_{CC}= 5V, V_{OUT}= 0.8V, R_{ISET}= 2kΩ, GCC= 0xFF, Scaling= 0xFF (Note 7)		38		mA
	Output current	V_{CC}= 5V, V_{OUT}= 0.6V, R_{ISET}= 3.3kΩ, GCC= 0xFF, SL= 0xFF	21.39	23	24.61	mA
ΔI_{MATCH}	Output current mismatch between channels	R_{ISET}= 3.3kΩ, GCC= 0xFF, V_{OUT}= 0.6V, SL= 0xFF (Note 8)	-6		6	%
V_{HR}	Headroom voltage	R_{ISET}= 3.3kΩ, I_{OUT}= 20mA SL= 0xFF		0.3	0.5	V
I_{CC}	Quiescent power supply current	V_{CC}= 5V, R_{ISET}= 3.3kΩ, GCC= 0xFF, SL = 0xFF, I_{OUT}= 23mA, PWM= 0x00		3.3	5	mA
		V_{CC}= 3.6V, R_{ISET}= 3.3kΩ, GCC= 0xFF, SL = 0xFF, I_{OUT}= 23mA, PWM= 0x00		2.7	4	mA
I_{SD}	Shutdown current	V_{CC}= 5V, R_{ISET}= 3.3kΩ, V_{SDB}= 0V or software shutdown		2	3	µA
		V_{CC}= 3.6V, R_{ISET}= 3.3kΩ, V_{SDB}= 0V or software shutdown		1	2	µA
f_{OUT}	PWM frequency of output	PWM Resolution 8 bit, OSC clock select 8MHz	30	32	34	kHz
I_{OZ}	Output leakage current	V_{SDB}= 0V or software shutdown, V_{OUT}= 5.5V			0.1	µA
T_{SHDN}	Thermal shutdown	(Note 9)		160		°C
$T_{SHDNHYST}$	Hysteresis	(Note 9)		20		°C
V_{ISET}	Output voltage of ISET pin		0.8	1.0	1.1	V

ELECTRICAL CHARACTERISTICS (CONTINUED)

Typical values are T_A = 25°C, V_{CC} = 5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT}= 0V (Note 9)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= V_{CC} (Note 9)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 9)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	µs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	µs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	µs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	µs
$t_{HD, DAT}$	Data hold time (Note 10)	-		-	-		-	µs
$t_{SU, DAT}$	Data setup time (Note 11)	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	µs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	µs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 7: The recommended minimum value of R_{ISET} is 2kΩ, or it may cause a large current.

Note 8: ΔI_{MAT}= (I_{OUT}- I_{AVG})/I_{AVG}×100%. I_{AVG}= (I_{OUT1}+I_{OUT2}+…I_{OUT18})/18.

Note 9: Guaranteed by design.

Note 10: The minimum $t_{HD, DAT}$ measured start from V_{IL}(max) of SCL signal. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. V_{IL}(max).

Note 11: A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU,DAT}$≥ 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU,DAT}$ = 1000 + 250 = 1250ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

FUNCTIONAL BLOCK DIAGRAM
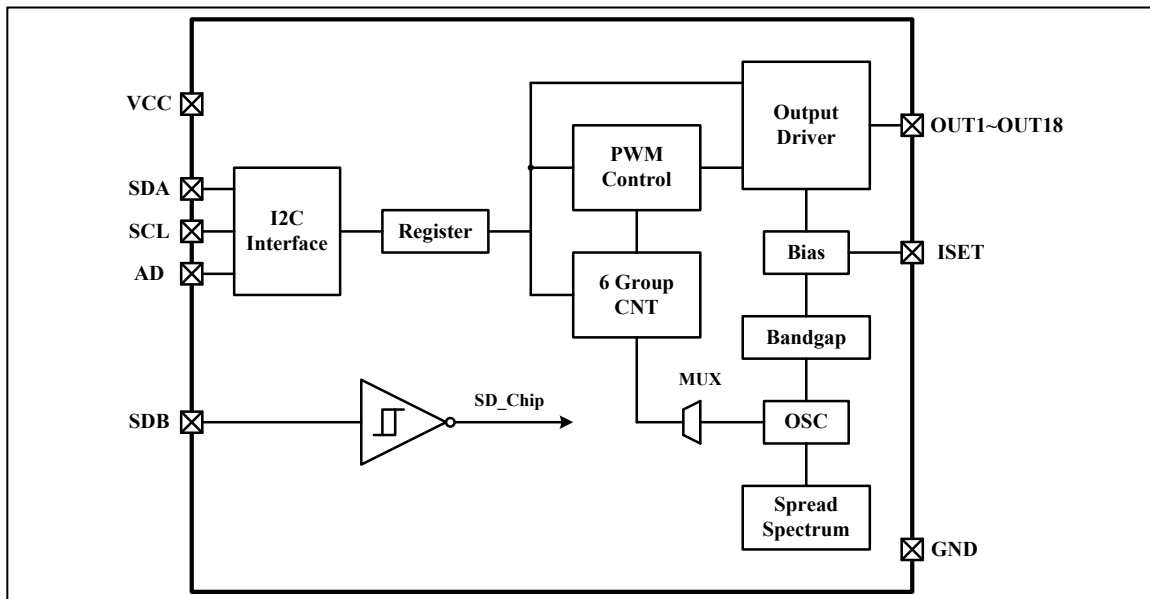
DETAILED DESCRIPTION

I2C INTERFACE

The IS32FL3207 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS32FL3207 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin. The complete slave address is:

Table 1   Slave Address (Write Only):

Bit	A7:A3	A2:A1	A0
Value	01101	AD	0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS32FL3207.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS32FL3207's acknowledge. The master releases the SDA line high (through a pull-up resistor).

Then the master sends an SCL pulse. If the IS32FL3207 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32FL3207, the register address byte is sent, most significant bit first. IS32FL3207 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS32FL3207 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS32FL3207, load the address of the data register that the first data byte is intended for. During the IS32FL3207 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS32FL3207 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS32FL3207 (Figure 5).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS32FL3207 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS32FL3207 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS32FL3207 to the master (Figure 6).
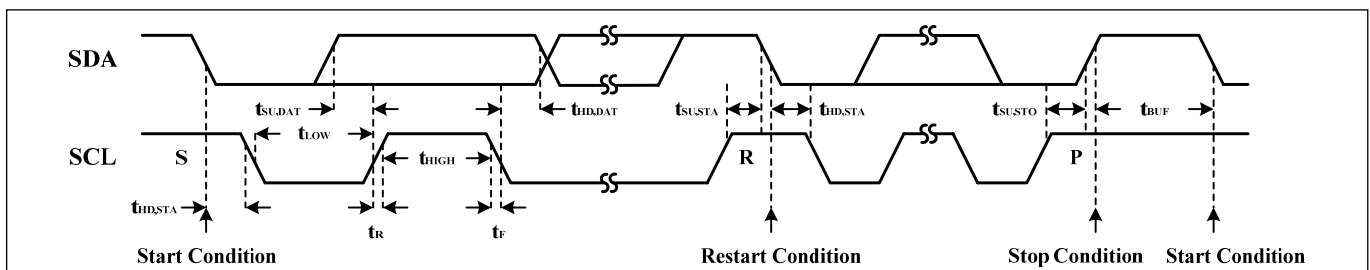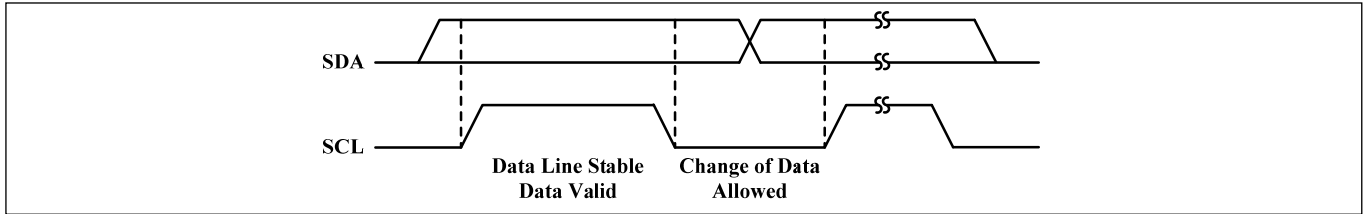

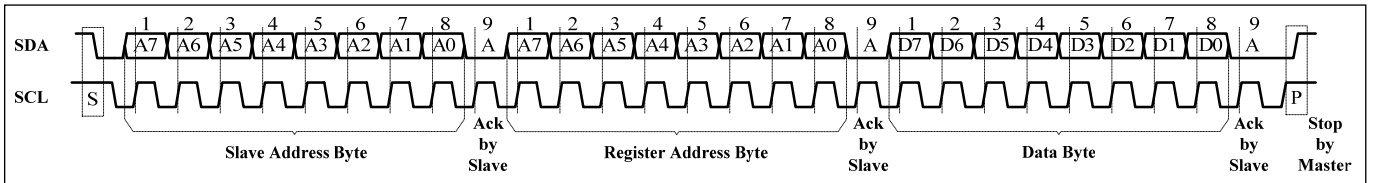**Figure 2**   Interface Timing

Figure 3   Bit Transfer

Figure 4   Writing to IS32FL3207 (Typical)
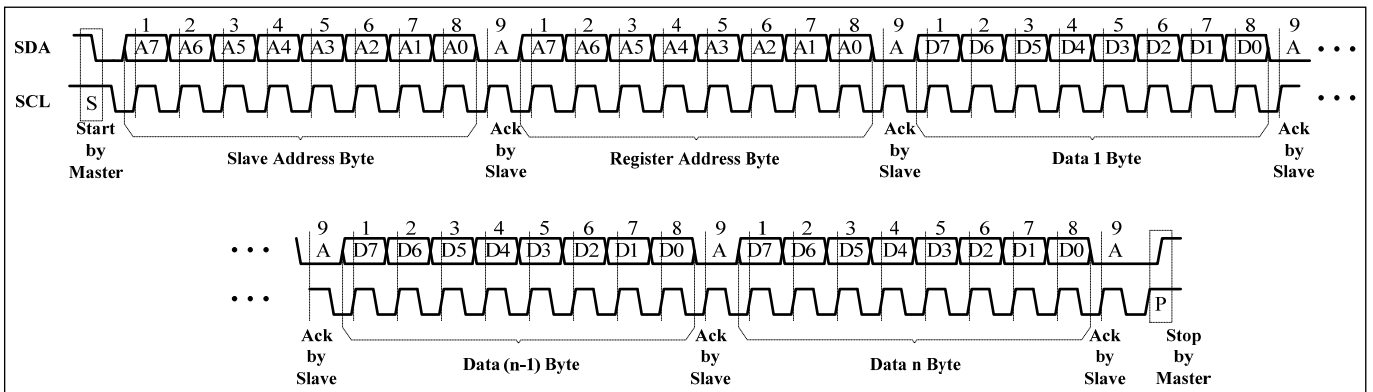
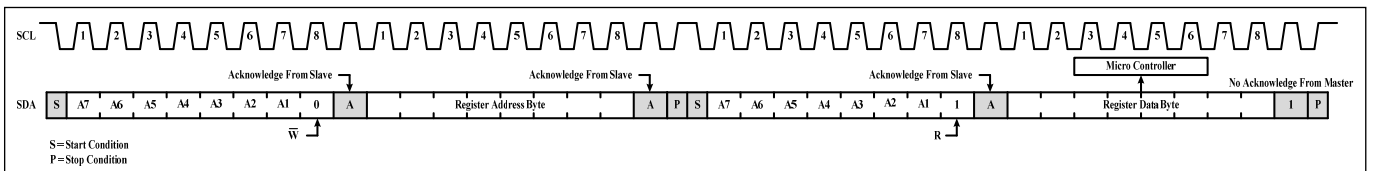**Figure 5**   Writing to IS32FL3207 (Automatic Address Increment)

Figure 6   Reading from IS32FL3207

IS32FL3207

REGISTER DEFINITIONS
Table 2   Register Function

Address	Name	Function	R/W	Table	Default
00h	Control Register	Power control register	R/W	3	
01h~24h	PWM Register	Channel [18:1] PWM register byte	R/W	5	
49h	Update Register	Update the PWM and Scaling data	W	-	
4Ah~5Bh	LED Scaling Register	Control each channel's DC current	R/W	7	
6Eh	Global Current Control Register	Control Global DC current/SSD	R/W	8	
70h	Phase Delay and Clock Phase Register	Phase Delay and Clock Phase	R/W	9	0000 0000
71h	Open Short Detect Enable Register	Open short detect enable	R/W	10	
72h~74h	LED Open/Short Register	Open short information	R/W	11	
77h	Temperature Sensor Register	Temperature information	R/W	12	
78h	Spread Spectrum Register	Spread spectrum control register	R/W	13	
7Fh	Reset Register	Reset all registers	W	-	

Table 3   00h   Control Register

Bit	D7	D6:D4	D3	D2:D1	D0
Name	-	OSC	-	PMS	SSD
Default	0	000	0	00	0

The Control Register sets software shutdown mode, internal oscillator clock frequency and PWM resolution. The internal oscillator clock frequency and the PWM resolution will decide the output PWM frequency. Recommend selecting PWM frequency higher than 20 kHz to avoid MLCC audible noise as shown in Table 4.

SSD   Software Shutdown Enable
0   Software shutdown mode
1   Normal operation

PMS   PWM Resolution
00   N=256, 8-bit
01   N=1024, 10-bit
10   N=4096, 12-bit
11   N=65536, 16-bit

OSC   Oscillator Clock Frequency Selection
000   16MHz
001   8MHz
010   1MHz
011   500kHz
100   250kHz
101   125kHz
110   62kHz
111   31kHz

Table 4   PWM Frequency

PWM Resolution	16M	8M	1M	500k	250k	125k	62k	31k
8bit	62k	32k	4k	2k	1k	0.5k	244	122
10bit	16k	8k	1k	0.5k	244	122	NA	NA
12bit	4k	2k	244	122	NA	NA	NA	NA
16bit	244	122	NA	NA	NA	NA	NA	NA

Table 5   01h~24h   PWM Register

Reg	02h (04h, 06h…)	01h (03h, 05h…)
Bit	D7:D0	D7:D0
Name	PWM_H	PWM_L
Default	0000 0000	0000 0000

Each output has 2 bytes to modulate the PWM duty in 256/1024/4096/65536 steps. If using 8-bit PWM resolution, only PWM_L bits need to be set.

The value of the SL (Scaling Register) decides the peak current of each LED noted as I_{OUT}.

I_{OUT} and the value of the PWM Registers decide the average current of each LED noted as I_{LED}.

I_{OUT} is computed by Formula (1):

$$I_{OUT} = I_{OUT(MAX)} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (1)$$

I_{LED} computed by Formula (2):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT} \qquad (2)$$

$$N=256: \quad PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

N=1024: $PWM = \sum_{n=0}^{9} D[n] \cdot 2^n$

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$

N=65536: $PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$ (3)

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information), GCC is the global current setting (6Eh), and SL is the scaling of each output (4Ah~6Dh), N=256/1024/4096/65536(8/10/12/16 bits PWM resolution).

For example: R_{ISET}=3.3kΩ, GCC=0xFF, SL=0xFF, PMS= "11" (16-bit PWM resolution), PWM_H=0xFF, PWM_L=0xFF, $I_{OUT(MAX)}$= 23.18mA.

$$I_{OUT} = I_{OUT(MAX)} \times \frac{255}{256} \times \frac{255}{256} = 23\,mA \quad (1)$$

$$PWM = \sum_{n=0}^{15} D[n] \cdot 2^n = 65535 \quad (3)$$

N= 65536

$$I_{LED} = \frac{65535}{65536} \times 23\,mA = 23\,mA \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information).

The I_{OUT} of each channel is set by the SL bits of LED Scaling Register (4Ah~6Dh). Please refer to the detail information in Table 7.

If R_{ISET}=3.3kΩ, GCC=0xFF, SL=0xFF, PMS= "00" (8-bit PWM resolution, only use the PWM_L, the PWM_H will be ignored), PWM_H=0x77, PWM_L=0xAA, $I_{OUT(MAX)}$ = 23.18mA

$$I_{OUT} = I_{OUT(MAX)} \times \frac{255}{256} \times \frac{255}{256} = 23\,mA \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n = 170 \quad (3)$$

N= 256

$$I_{LED} = \frac{170}{256} \times 23\,mA \quad (2)$$

Table 6   PWM and Scaling Register Map

OUT	PWM		SL
	PWM_H	PWM_L	
1	02h	01h	4Ah
2	04h	03h	4Bh
3	06h	05h	4Ch
4	08h	07h	4Dh
5	0Ah	09h	4Eh
6	0Ch	0Bh	4Fh
7	0Eh	0Dh	50h
8	10h	0Fh	51h
9	12h	11h	52h
10	14h	13h	53h
11	16h	15h	54h
12	18h	17h	55h
13	1Ah	19h	56h
14	1Ch	1Bh	57h
15	1Eh	1Dh	58h
16	20h	1Fh	59h
17	22h	21h	5Ah
18	24h	23h	5Bh

49h   Update Register
When SDB = "H" and SSD = "1", a write of 00h to 49h is to update the PWM Registers (01h~24h) values.

Table 7   4Ah~5Bh   LED Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Each output has 8 bits to modulate DC current in 256 steps.

The value of the LED Scaling Registers decides the DC peak current of each LED noted I_{OUT}.

I_{OUT} is computed by Formula (1):

$$I_{OUT} = I_{OUT(MAX)} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (1)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (4)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET}, GCC is the global current setting (6Eh).

4Ah~5Bh don't need to update by 49h, each register will be updated immediately when it is written.

Table 8   6Eh   Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

GCC and SL control the I_{OUT} as shown in Formula (1).

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (5)$$

If GCC=0xFF, SL=0xFF, $I_{OUT}=I_{OUT(MAX)}$
If GCC=0x01, SL=0xFF,

$$I_{OUT} = I_{OUT(MAX)} \times \frac{1}{256} \times \frac{255}{256}$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information).

Table 9   70h   Phase Delay and Clock Phase Register

Bit	D7	D6:D3	D2	D1	D0
Name	PDE	-	PS3	PS2	PS1
Default	0	0000	0	0	0

IS32FL3207 features a 3-phase delay function, when PDE bit is set, the phase delay function is enabled.

Phase Delay separates 18 outputs as 3 groups, OUT1~OUT6 as group 1, OUT7~OUT12 as group 2, OUT13~OUT18 as group 3. When Phase Delay is enabled, group 2 has a $1/(3 \times f_{OUT})$ time delay than group 1, group 3 also has a $1/(3 \times f_{OUT})$ time delay than group 2.

Phase Delay feature and Clock Phase options can work together to minimize the voltage ripple of LED power supply.

PDE	Group Phase Delay Enable
0	Phase delay disable
1	Phase delay enable

PS1	OUT1~OUT6 Phase Select
0	Phase delay 0 Degree
1	Phase delay 180 Degree

PS2	OUT7~OUT12 Phase Select
0	Phase delay 0 Degree
1	Phase delay 180 Degree

PS3	OUT13~OUT18 Phase Select
0	Phase delay 0 Degree
1	Phase delay 180 Degree

Table 10   71h   Open Short Detect Enable Register

Bit	D7:D2	D1:D0
Name	-	OSDE
Default	0000 00	00

OSDE enables the open and/or short LED channel detection with the result stored in 72h~76h, note either open or short information is saved not both.

OSDE	Open Detect Enable
00	Detect disable
01	Detect disable
10	Short detect enable
11	Open detect enable

Table 11-1   72h   LED Open/Short Register

Bit	D7:D0
Name	OP/ST[8:1]
Default	0000 0000

Table 11-2   73h   LED Open/Short Register

Bit	D7:D0
Name	OP/ST[16:9]
Default	0000 0000

Table 11-3   74h   LED Open/Short Register

Bit	D7:D2	D1:D0
Name	-	OP/ST[18:17]
Default	0000 00	00

Open or short status is stored in 72h to 74h.

OP[18:1]	Open Information of OUT18:OUT1
0	Open not detected
1	Open detected

ST[18:1]	Short Information of OUT18:OUT1
0	Short not detected
1	Short detected

Table 12   77h   Temperature Sensor Register

Bit	D7:D6	D5	D4	D3:D2	D1:D0
Name	TROF	-	T_Flag	-	TS
Default	00	0	0	00	00

TS stores the temperature/thermal roll-off point. TROF stores percentage of output current of the thermal rool-off function.

Read T_Flag can indicate if the die temperature exceeds the setting point (TS). Before each reading of 77h register, TROF and TS need to be re-written.

TROF	Thermal roll off percentage of output current
00	I_{OUT} x 100%
01	I_{OUT} x 75%
10	I_{OUT} x 55%
11	I_{OUT} x 30%

T_Flag	Temperature Flag
0	Temperature point not exceeded
1	Temperature point exceeded

TS	Temperature Point, Thermal roll off start point
00	140°C
01	120°C
10	100°C
11	90°C

Table 13   78h   Spread Spectrum Register

Bit	D7:D5	D4	D3:D2	D1:D0
Name	DCPWM	SSP	RNG	CLT
Default	000	0	00	00

When DCPWM is set to "0", the PWM outputs are decided by 01h~48h, and the PWM range is 0/256~255/256(8-bit PWM, 0/1024~1023/1024 for 10 bit PWM, 0/4096~4095/4096 for 12 bit PWM, 0/65536~65535/65536 for 16 bit PWM), still the 1/256(8-bit PWM, 1/1024 for 10 bit PWM, 1/4096 for 12 bit PWM, 1/65536 for 16 bit PWM), can't be turned on. When the DCPWM is set to "1", PWM dimming is disabled and dimming will be done by current adjust GCC and SL registers.

Spread spectrum register configures the spread spectrum function, adjust the cycle time and range.

DCPWM	Setting the output to work in DC mode
xx0	Output 1~12 PWM data set by registers 01h~18h
xx1	Output 1~12 set to turn on (PWM is disabled)
x0x	Output 13~18 PWM data set by registers 19h~24h
x1x	Output 13~18 set to turn on (PWM is disabled)

SSP	Spread Spectrum Enable
0	Disable
1	Enable

RNG	Spread Spectrum Range
00	±5%
01	±15%
10	±24%
11	±34%

CLT	Spread Spectrum Cycle Time
00	1980µs
01	1200µs
10	820µs
11	660µs

7Fh   Reset Register

When SDB = "H" and SSD = "1", a write of "0000 0000" to 7Fh will reset all registers to their default values.

APPLICATION INFORMATION

R$_{ISET}$

The maximum output current I$_{OUT(MAX)}$ of OUT1~OUT18 can be adjusted by the external resistor, R$_{ISET}$, as described in Formula (6).

$$I_{OUT\,(MAX\,)} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (6)$$

x = 76.5, V$_{ISET}$ = 1.0V.

The recommended minimum value of R$_{ISET}$ is 2kΩ.

When R$_{ISET}$=3.3kΩ, I$_{OUT(MAX)}$=23.18mA

When R$_{ISET}$=2kΩ, I$_{OUT(MAX)}$=38.25mA

R$_{ISET}$ should be close to the chip and the ground side should well connect to the GND plane.

CURRENT SETTING

The maximum output current is set by the external register R$_{ISET}$. The current of each output can also be set independently by the SL 8 bits of LED Scaling Register (4Ah~5Bh).

Some applications may require the IOUT of each channel need to be adjusted independently. For example, if OUT1 drives 1 LED and OUT2 drives 2 parallel LEDs, and they should have the same average current like 18mA, we can set the I$_{OUT(MAX)}$ to 36mA, and GCC=0xFF, 4Ah=0x80, 4Bh=0xFF, the OUT1 sinks about 18mA and OUT2 sinks 36mA which can have two LEDs in parallel.

Another example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED, with same R$_{ISET}$, GCC and same SL bits, when OUT1 OUT2 and OUT3 have the same PWM value, the LED may look a litter pink, or not so white, in this case, the SL bits can be used to adjust the single IOUTx of some output and make it pure white color. We call this SL bits another name: white balance registers.

PWM CONTROL

The PWM Registers (01h~24h) can modulate LED brightness of each 18 channels with 256/1024/4096/65536 steps. For example, if the data in PWM_H Register is "0000 0000" and in PWM_L Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

PWM FREQUENCY SELECT

The IS32FL3207 output channels operate with a default 8 bits PWM resolution and the PWM frequency of 62kHz (the oscillator frequency is 16MHz). Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 300Hz to 18kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS32FL3207's output PWM frequency above/below the audible range. The Contorl Register (00h) can be used to set the switching frequency to 122Hz~62kHz as shown in Table 4, some combine setting of the OSC and PMS bits will get different output PWM frequency, and higher than 20kHz is out of the audible range.

OPEN/SHORT DETECT FUNCTION

IS32FL3207 has open and short detect bit for each LED.

By setting the OSDE bit of Open Short Detect Enable Register (71h) from "00" to "10" (store short information) or "11" (store open information), the LED Open/Short Register will store the open/short information immediately the MCU can get the open/short information by reading the 72h~74h.

SPREAD SPECTRUM FUNCTION

PWM current switching of LED outputs can be particularly troublesome when the EMI is concerned. To optimize the EMI performance, the IS32FL3207 includes a spread spectrum function. By setting the RNG bit of Spread Spectrum Register (78h), Spread Spectrum range can be choosen from ±5% /±15% /±24% /±34%. The spread spectrum function will lower the total electromagnetic emitting energy by spreading the energy into a wider range to significantly degrade the peak energy of EMI. With spread spectrum, the EMI test is easier to pass with a smaller size and lower cost filter circuit.

OPERATING MODE

IS32FL3207 can only operate in PWM Mode. The brightness of each LED can be modulated with 256/1024/4096/65536 steps by PWM registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

IS32FL3207

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting the SSD bit of the Control Register (00h) to "0", the IS32FL3207 will operate in software shutdown mode. When the IS32FL3207 is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers accessible. Typical current consume is 1µA (V_{CC}=3.6V).

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consumption is 1µA (V_{CC}=3.6V).

The chip releases hardware shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but the register information retains. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS32FL3207 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks' supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1µF capacitor, if possible with a 1µF capacitor is recommended to connected to the ground at power supply pin of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

R_{ISET}

R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. The thermal pad of IS32FL3207 should connect to GND net and need to use 4 or 9 vias connect to GND copper area, the GND area should be as large area as possible to help radiate the heat from the IS32FL3207.

Current Rating Example

For a R_{ISET}=3.3kΩ application, the current rating for each net is as follows:

• VCC pin maximum current is 5mA when V_{CC}=5V, but the VLED+ net is provided total current of all outputs, its current can as much as 23mA×18=414mA, recommend trace width for VCC pin: 0.20mm~0.3mm, recommend trace width for VLED+ net: 0.25mm~0.5mm,

• Output pins=23mA, recommend trace width is 0.2mm~0.254mm

• All other pins<3mA, recommend trace width is 0.15mm~0.254mm

CLASSIFICATION REFLOW PROFILES

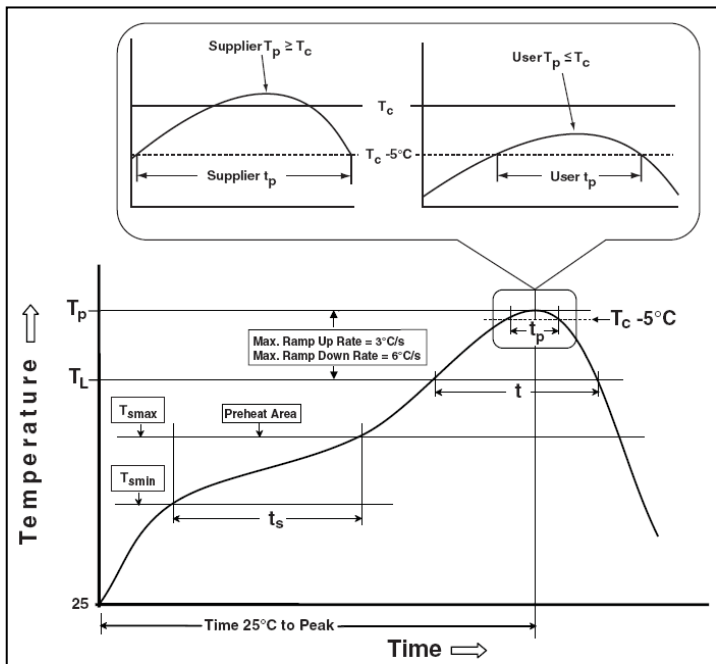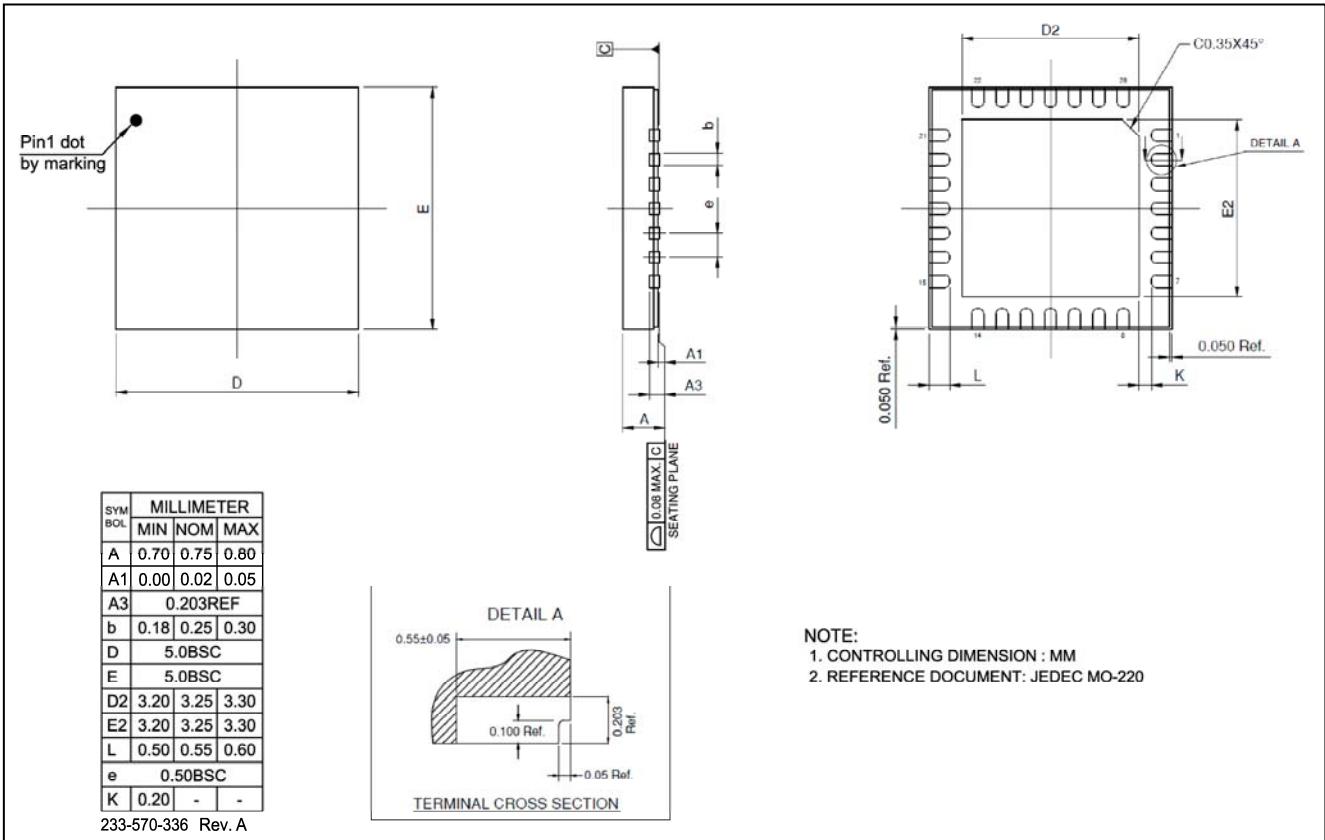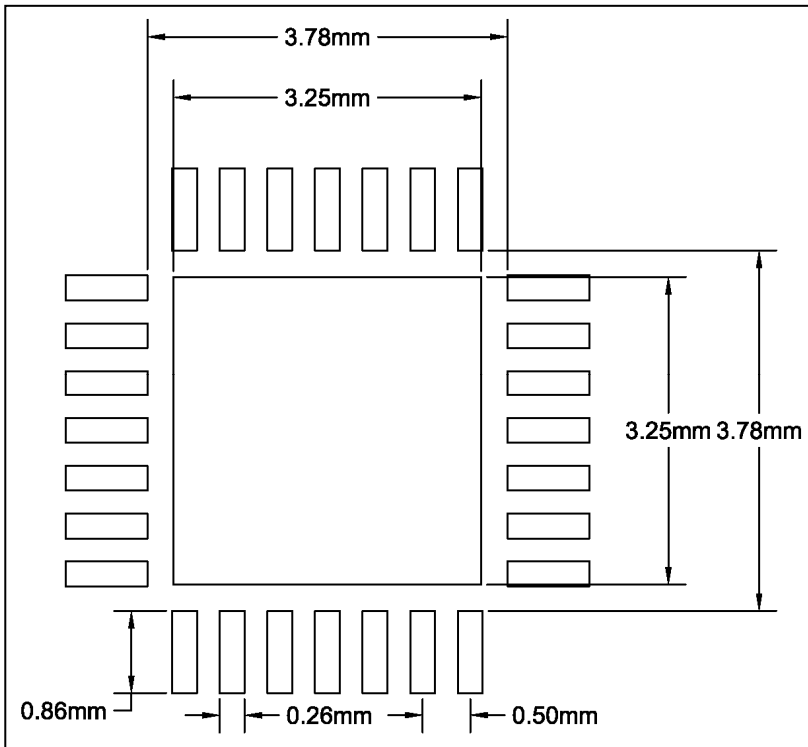| Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Figure 7   Classification Profile

PACKAGE INFORMATION

WFQFN-28

SYM BOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.18	0.25	0.30
D	5.0BSC		
E	5.0BSC		
D2	3.20	3.25	3.30
E2	3.20	3.25	3.30
L	0.50	0.55	0.60
e	0.50BSC		
K	0.20	-	-

233-570-336   Rev. A

Pin1 dot by marking

DETAIL A

0.55±0.05

0.100 Ref.

0.203 Ref.

0.05 Ref.

TERMINAL CROSS SECTION

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

C0.35X45°

0.050 Ref.

0.050 Ref.

RECOMMENDED LAND PATTERN

WFQFN-28

Note:

1. Land pattern complies to IPC-7351.

2. All dimensions in MM.

3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

IS32FL3207

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release.	2020.05.12
B	1. Update to new Lumissil logo 2. Add RoHS and update AECQ information	2024.05.14