

## Dual N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) Max.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
100	0.012 at V <sub>GS</sub> = 10 V	12	20.7 nC
	0.013 at V <sub>GS</sub> = 7.5 V	11	
	0.014 at V <sub>GS</sub> = 4.5 V	10	

### FEATURES

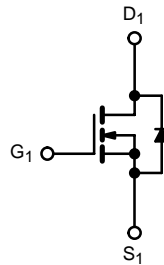
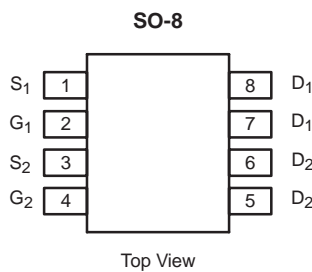
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested

### APPLICATIONS

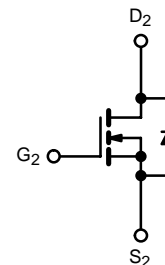
- DC/DC Primary Side Switch
- Telecom/Server
- Industrial



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	A
		T <sub>C</sub> = 70 °C	
		T <sub>A</sub> = 25 °C	
		T <sub>A</sub> = 70 °C	
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	45	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	
Single Pulse Avalanche Current	I <sub>AS</sub>	30	mJ
Avalanche Energy	E <sub>AS</sub>	45	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	W
		T <sub>C</sub> = 70 °C	
		T <sub>A</sub> = 25 °C	
		T <sub>A</sub> = 70 °C	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	33	42	°C/W
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	16	21	

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 85 °C/W.

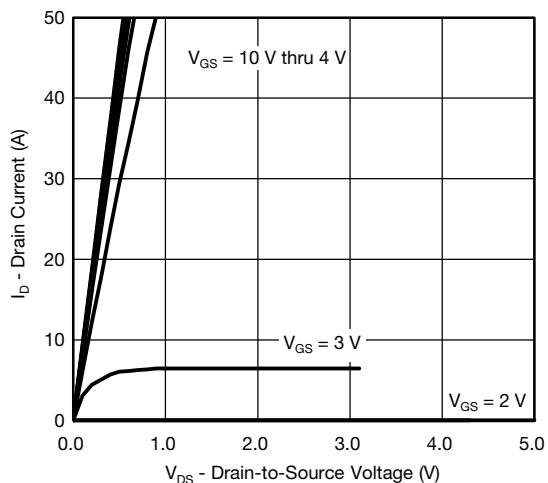
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		64		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-5.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.012		$\Omega$
		$V_{GS} = 7.5\text{ V}, I_D = 10\text{ A}$		0.013		
		$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		0.014		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		54		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1970		pF
Output Capacitance	$C_{oss}$			695		
Reverse Transfer Capacitance	$C_{rss}$			62		
Total Gate Charge	$Q_g$	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		44.4	67	nC
		$V_{DS} = 50\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		20.7	31	
Gate-Source Charge	$Q_{gs}$			6.1		
Gate-Drain Charge	$Q_{gd}$			9.1		
Output Charge	$Q_{oss}$	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		56	85	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.4	1.1	2.2	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega$ $I_D \equiv 10\text{ A}, V_{GEN} = 7.5\text{ V}, R_g = 1\text{ }\Omega$		15	30	ns
Rise Time	$t_r$			11	22	
Turn-Off Delay Time	$t_{d(off)}$			31	60	
Fall Time	$t_f$			10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega$ $I_D \equiv 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		12	24	
Rise Time	$t_r$			10	20	
Turn-Off Delay Time	$t_{d(off)}$			34	65	
Fall Time	$t_f$			10	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			5.4	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				70	
Body Diode Voltage	$V_{SD}$	$I_S = 5\text{ A}$		0.76	1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		42	80	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			40	80	nC
Reverse Recovery Fall Time	$t_a$			19		ns
Reverse Recovery Rise Time	$t_b$			23		

Notes:

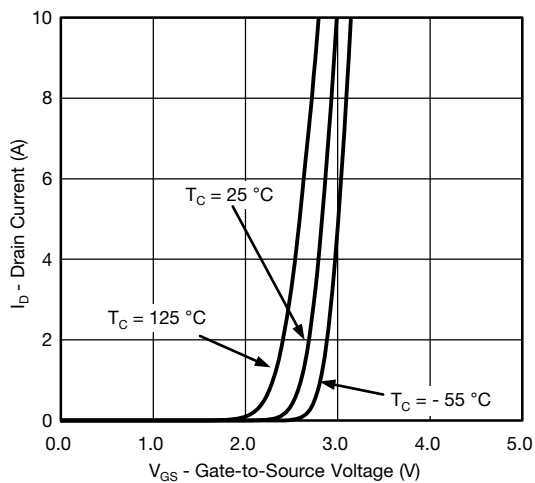
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

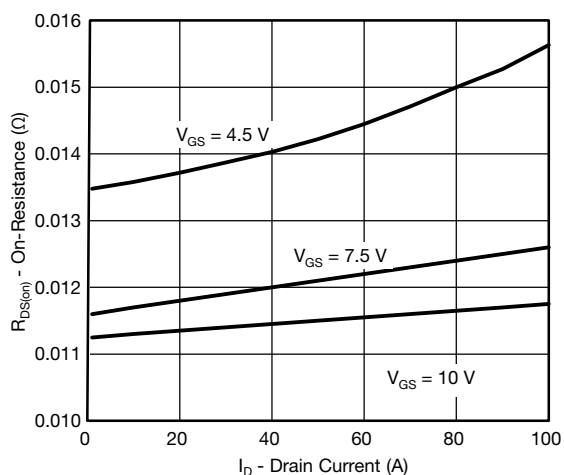
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



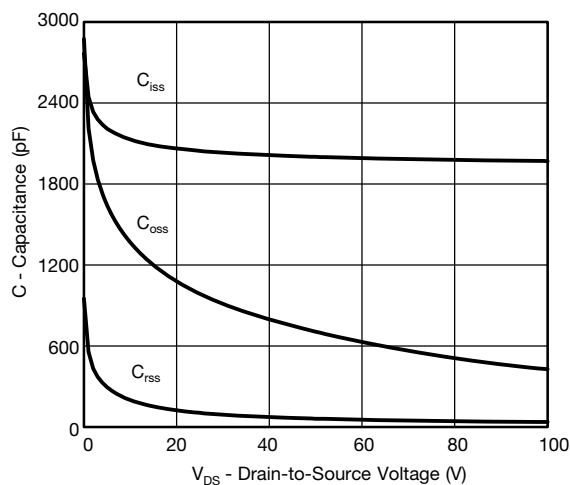
**Output Characteristics**



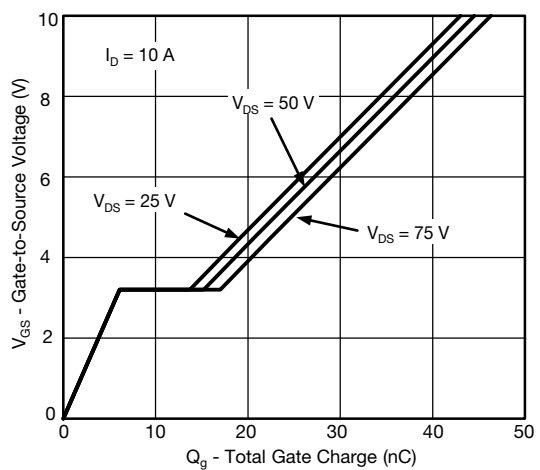
**Transfer Characteristics**



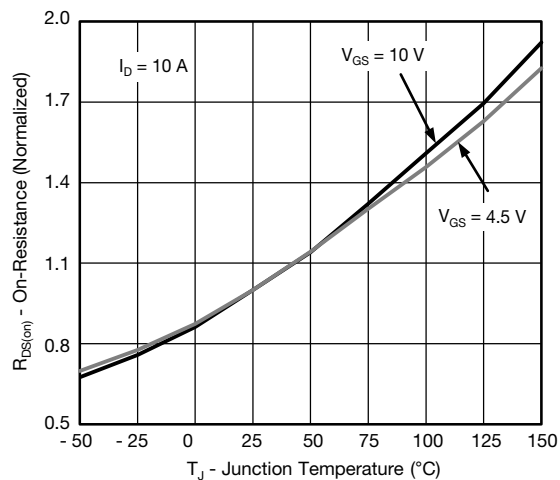
**On-Resistance vs. Drain Current**



**Capacitance**

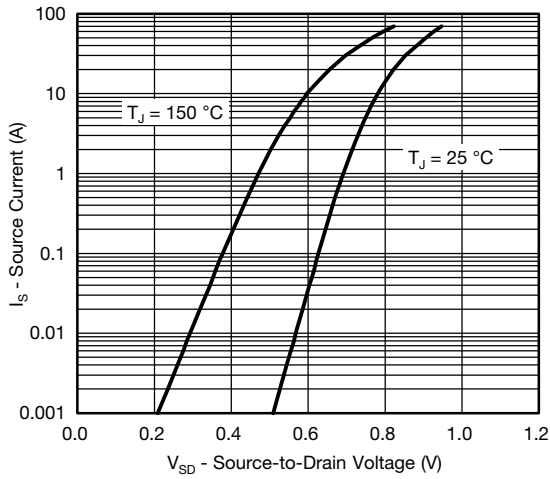


**Gate Charge**

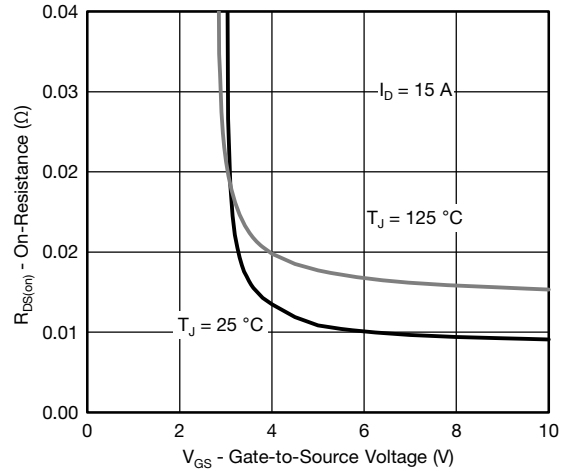


**On-Resistance vs. Junction Temperature**

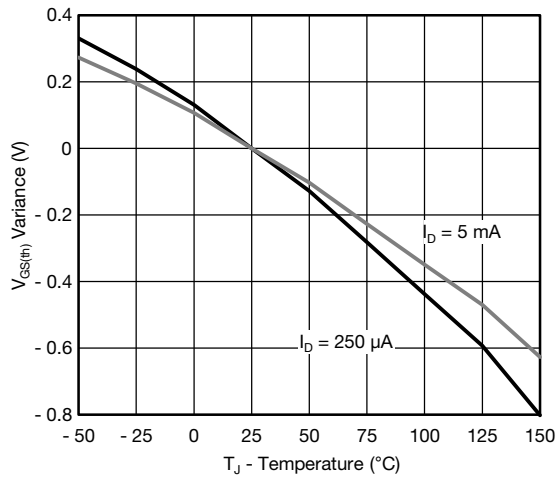
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



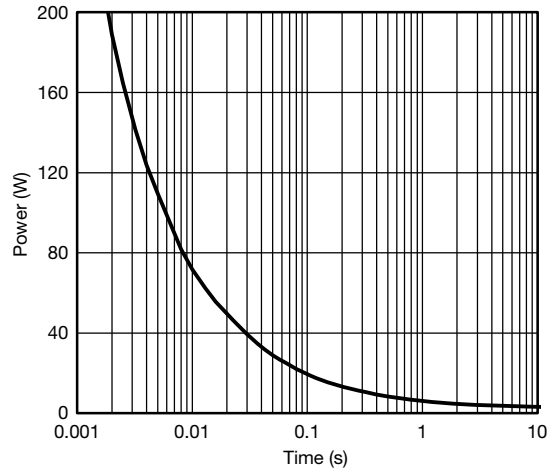
**Source-Drain Diode Forward Voltage**



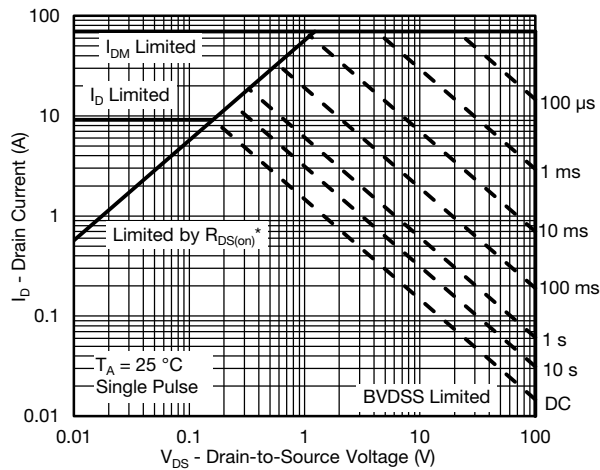
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



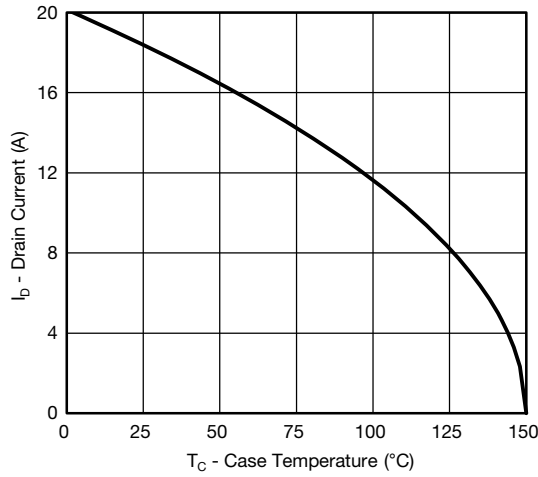
**Single Pulse Power, Junction-to-Ambient**



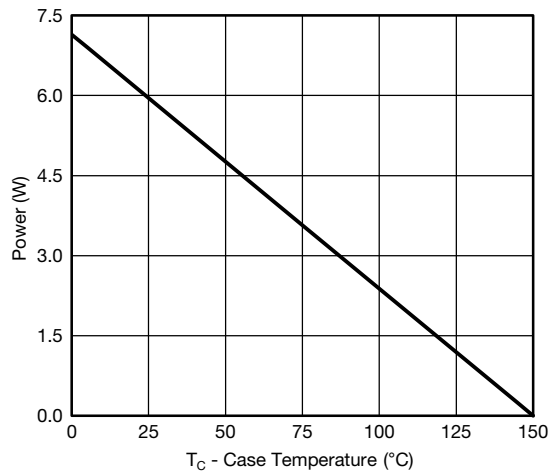
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

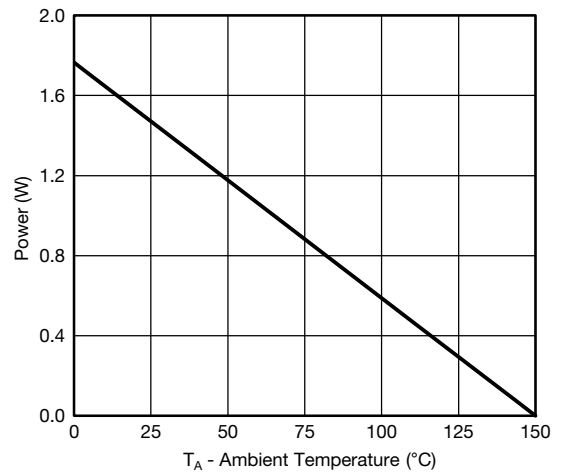
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



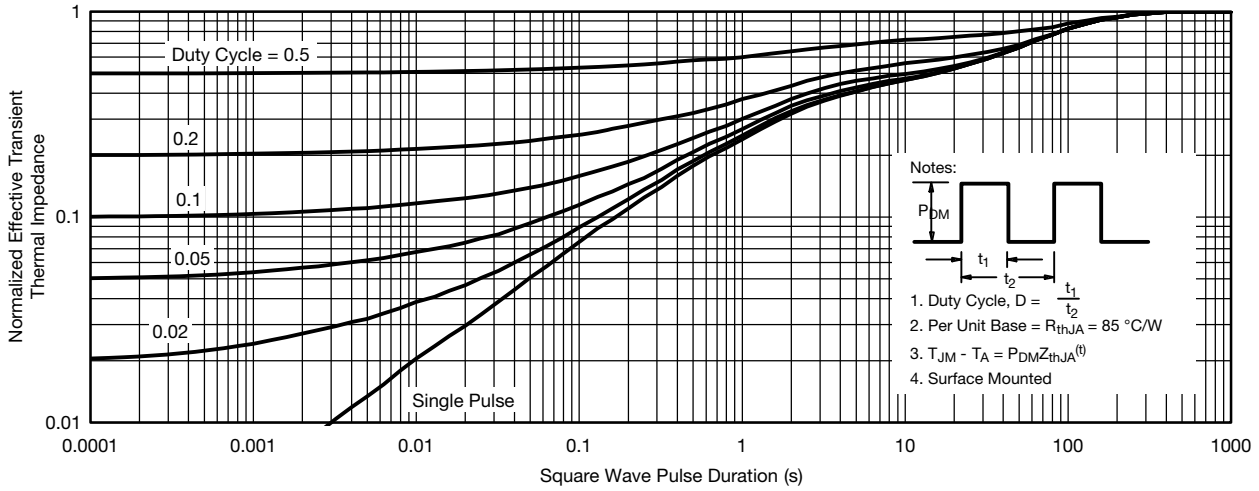
**Power, Junction-to-Foot**



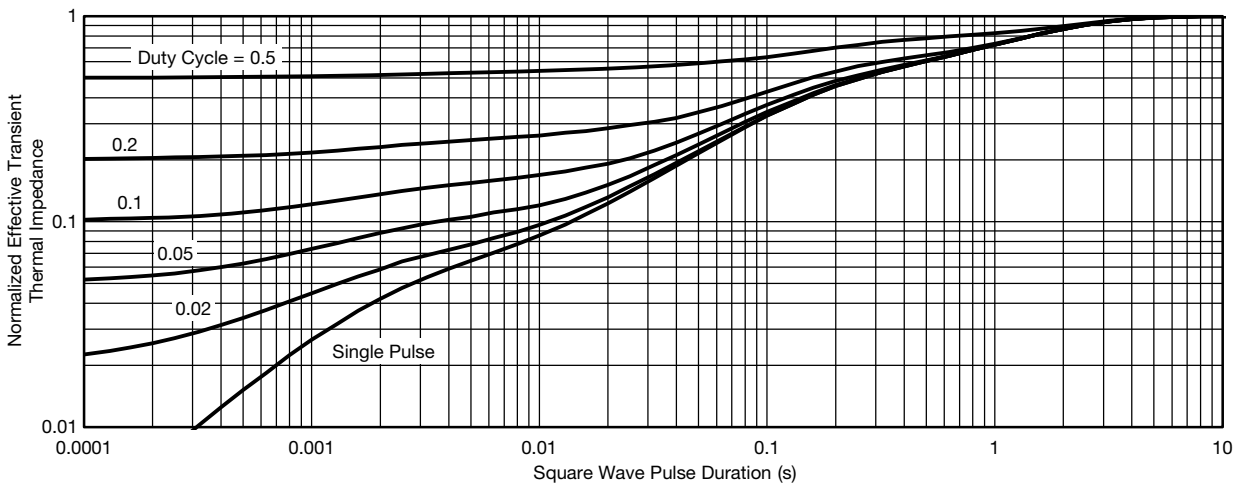
**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



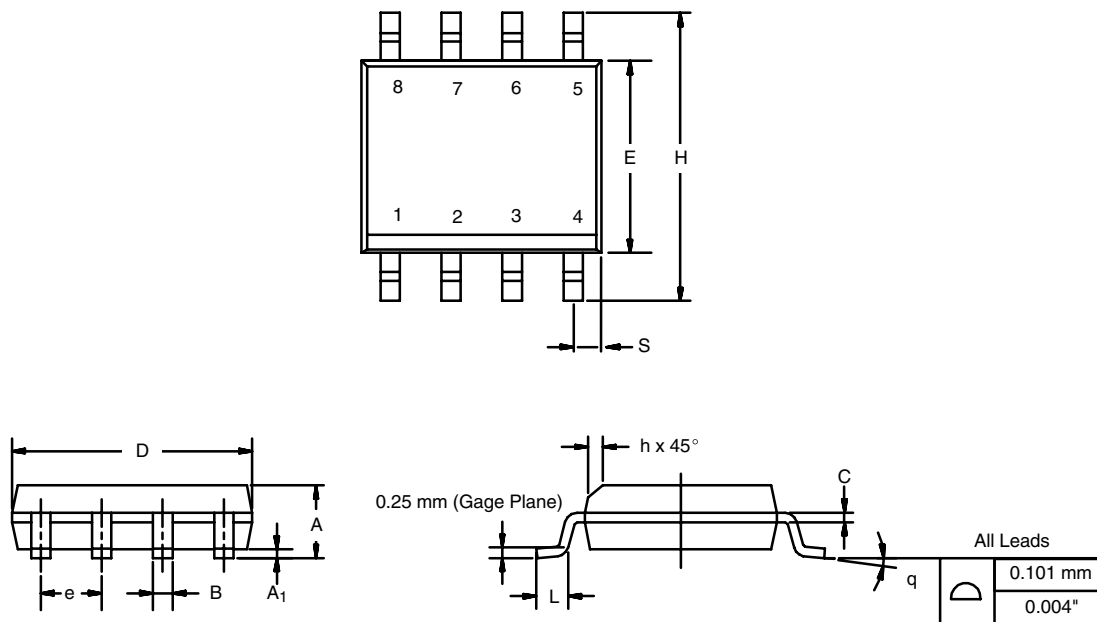
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

**SOIC (NARROW): 8-LEAD**

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06  
DWG: 5498

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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