IS2062/64

Bluetooth® Dual Mode Stereo Audio SoC

Introduction

The IS2062/64 products are part of the Bluetooth Dual Mode family of stereo audio System on Chip (SoC) devices.

- Flash-based devices:
  - The IS2062GM and IS2064GM SoCs are offered in LGA packages and contain in-package Flash, which allows for firmware updates.
- ROM-based devices:
  - The IS2064S and IS2064B support Stereo Mode functionality in ROM. This allows for audio playback on two devices. Some Bluetooth parameters can be customized and stored in an internal EEPROM. These products are offered in QFN and BGA packages.

Features

- Qualified for Bluetooth v5.0 Specification
- Bluetooth 5.0 Core System Component QDID is 110017
- Bluetooth Audio Profiles:
  - A2DP 1.3
  - AVRCP 1.6
  - HFP 1.6
  - HSP 1.2
  - SPP 1.2
- Bluetooth Low Energy (BLE):
  - Generic access service
  - Device information service
  - Proprietary services for data communication
  - Apple Notification Center Service (ANCS)
- Supports Bluetooth Low Energy data rate up to 1Mbits/s
- Supports 16 kHz High Definition (HD) Voice
- Audio Interfaces:
  - I^2S digital output (IS2064GM and IS2064S/B)
  - Analog output
  - Auxiliary input
  - Analog microphone input
- Supports Firmware Upgrade (IS2062GM/64GM)
- Integrated Battery Charger (up to 350 mA)

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Baseband Features

- 16 MHz main clock input
- Built-in Flash memory for programing (8 Mbit) (IS2062GM/64GM)
- Built-in EEPROM
- Connects simultaneously to two hosts over HFP/A2DP and SPP/BLE
- Adaptive Frequency Hopping (AFH)

Audio Codec

- Sub-Band Coding (SBC) decoding, Advanced Audio Coding (AAC) decoding (IS2062GM/64GM), and LDAC decoding (IS2064GM-0L3)
- 20-bit Digital-to-Analog Converter (DAC) with 98 dB SNR
- 16-bit Analog-to-Digital Converter (ADC) with 92 dB SNR
- Supports up to 24-bit, 96 kHz I^2S digital audio (IS2064GM and IS2064S/B)

RF Features

- Transmit output power: +2 dBm
- Receive sensitivity: -90 dBm (2 Mbps Enhanced Data Rate (EDR))
- Combined Tx/Rx RF terminal simplifies external matching and reduces external antenna switches
- Tx/Rx RF switch for Class 2 or Class 3 applications
- Integrated synthesizer requires no external voltage-controlled oscillator (VCO), varactor diode, and resonator or loop filter
- Crystal oscillator with built-in digital trimming compensates for temperature or process variations

DSP Audio Processing

- Includes a 32-bit DSP core
- Synchronous Connection-Oriented (SCO) channel operation
- 8/16 kHz noise suppression
- 8/16 kHz acoustic echo cancellation
- Modified Sub-Band Coding (MSBC) decoder for wide band speech
- Built-in High Definition Clean Audio (HCA) algorithms for both narrow band and wideband speech processing
- Packet Loss Concealment (PLC)
- Built-in audio effect algorithms to enhance audio streaming
- Serial Copy Management System (SCMS-T) content protection

Package Details

Table 1. PACKAGE DETAILS

Parameter	IS2062GM	IS2064GM	IS2064S	IS2064B
Package type	LGA	LGA	QFN	BGA
Pin count	56	68	68	61

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Parameter	IS2062GM	IS2064GM	IS2064S	IS2064B
Contact/Lead Pitch	0.4	0.4	0.4	0.5
Package size	7x7x1.0	8x8x1.0	8x8x0.9	5x5x0.9

Note: All dimensions are in millimeters (mm) unless specified.

Peripherals

- UART interface for host MCU communication
- Full-speed USB 1.1 interface (IS2064GM and IS2064S)
- Built-in lithium-ion (Li-Ion) and lithium-polymer (Li-Po) battery charger (up to 350 mA)
- Integrated 1.8V and 3V configurable voltage regulators
- Built-in ADC for battery monitoring, voltage sensor and charger thermal protection
- Built-in under voltage protection (UVP)
- LED drivers: 2 (IS2062GM and IS2064B) and 3 (IS2064GM and IS2064S)

Operating Condition

- Operating voltage : 3.2V to 4.2V
- Operating temperature : -20℃ to +70℃

Applications

- Headsets and headphones (IS2062GM and IS2064B)
- Portable speakers
- Earbuds and neckbands (IS2064B)

Table of Contents

1. Device Overview

The IS2062/64 SoC integrates:

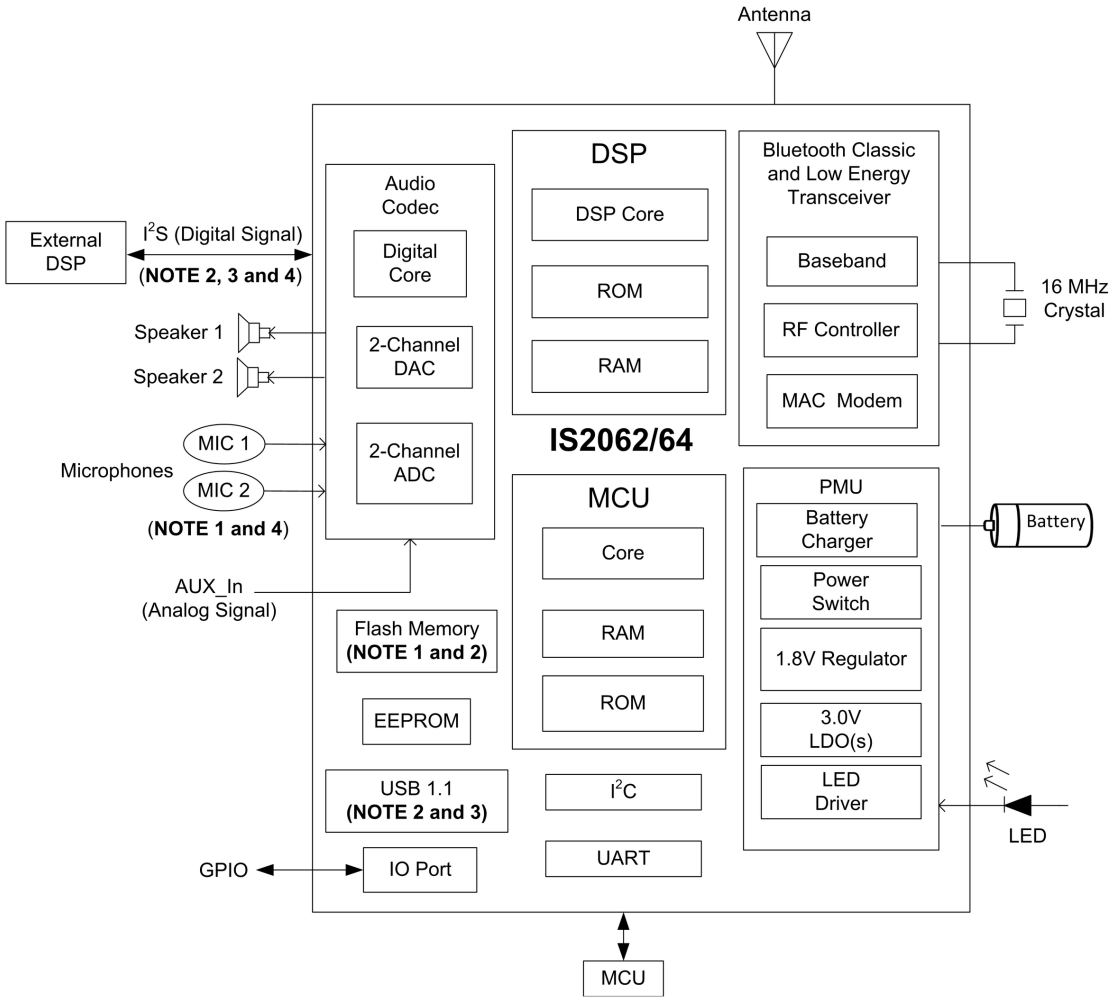
- Bluetooth 5.0 dual-mode radio transceiver
- Power Management Unit (PMU)
- Microcontroller (MCU)
- Audio codec
- Crystal oscillator
- 32-bit DSP
- Flash (IS2062GM/64GM)
- EEPROM

The IS2062/64 SoC is configured using an UI tool.

Note: The UI tool is a Windows® based configuration utility tool, which is available for download from the Microchip website at http://www.microchip.com/wwwproducts/en/IS2062 and http://www.microchip.com/wwwproducts/en/IS2064.

The following figure illustrates the block diagram of the IS2062/64 SoC.

Figure 1-1. BLOCK DIAGRAM OF IS2062/64 SOC



Note:

1. IS2062GM
2. IS2064GM
3. IS2064S
4. IS2064B

1.1 Key Features

The following table provides the key features of the IS2062/64 family.

Table 1-1. KEY FEATURES

Feature	IS2062GM	IS2064GM		IS2064S	IS2064B
		IS2064GM-012	IS2064GM-0L3		
Application	Headset/ Speaker	Speaker	Speaker	Speaker	Headset
Flash/ROM	Flash	Flash	Flash	ROM	ROM

.....continued

Feature	IS2062GM	IS2064GM		IS2064S	IS2064B
		IS2064GM-012	IS2064GM-0L3		
Stereo mode	Yes/ Programmable	Yes/ Programmable	Yes/ Programmable	Yes	Yes
Package	LGA	LGA	LGA	QFN	BGA
Pin/Ball count	56	68	68	68	61
Dimensions (mm)	7x7	8x8	8x8	8x8	5x5
Audio DAC output	2-channel	2-channel	NA	2-channel	2-channel
DAC (single-ended) SNR at 2.8V (dB)	-98	-98	NA	-98	-98
DAC (capless) SNR at 2.8V (dB)	-96	-96	NA	-96	-96
ADC SNR at 2.8V (dB)	-92	-92	-92	-92	-92
I^2S digital output	No	Yes	Yes	Yes	Yes
Analog output	Yes	Yes	No	Yes	Yes
Analog Auxiliary-Input	Yes	Yes	Yes	Yes	Yes
Mono analog microphone	2	1	1	1	2
External audio amplifier interface	Yes	Yes	Yes	Yes	Yes
UART	Yes	Yes	Yes	Yes	Yes
Full-speed USB 1.1	No	Yes	Yes	Yes	No
LED driver	2	3	3	3	2
Integrated DC-DC step-down regulator	1	1	1	1	1
Integrated LDO regulator	2	2	2	2	2
DC 5V adaptor input	Yes	Yes	Yes	Yes	Yes
Battery charger (350 mA maximum)	Yes	Yes	Yes	Yes	Yes

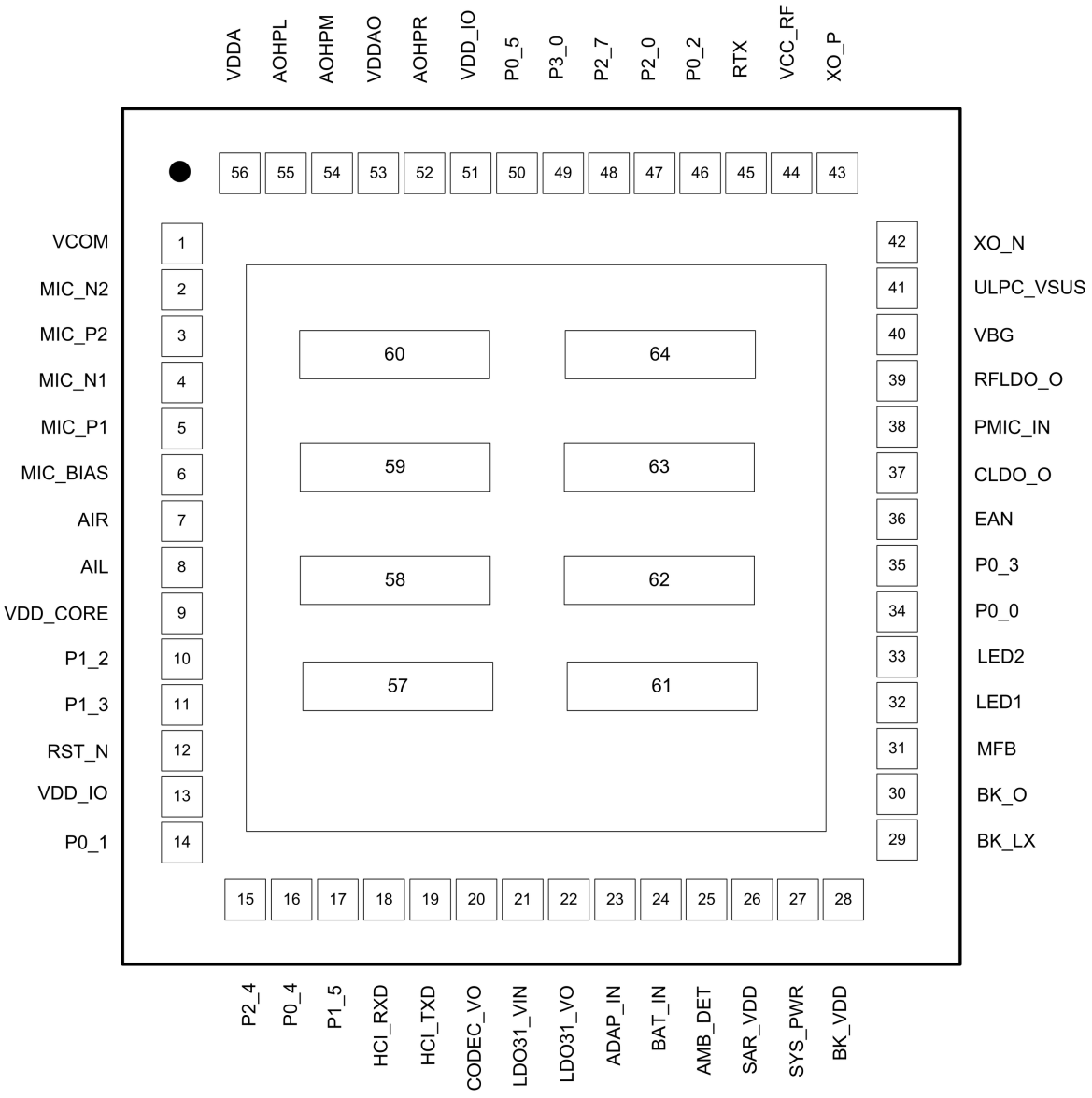
.....continued

Feature	IS2062GM	IS2064GM		IS2064S	IS2064B
		IS2064GM-012	IS2064GM-0L3		
ADC for charger thermal protection	Yes	Yes	Yes	Yes	Yes
Under Voltage Protection (UVP)	Yes	Yes	Yes	Yes	Yes
GPIO	10	15	15	15	10
EEPROM	128K	128K	128K	256K	128K
Multitone	Yes	Yes	Yes	Yes	Yes
DSP functions (audio playback and voice call)	Yes	Yes	Yes	Yes	Yes
BLE	Yes	Yes	Yes	Yes	Yes
Bluetooth profiles					
A2DP	1.3	1.3	1.3	1.3	1.3
AVRCP	1.6	1.6	1.6	1.6	1.6
HFP	1.6	1.6	1.6	1.6	1.6
HSP	1.2	1.2	1.2	1.2	1.2
SPP	1.2	1.2	1.2	1.2	1.2

1.2 Pin Details

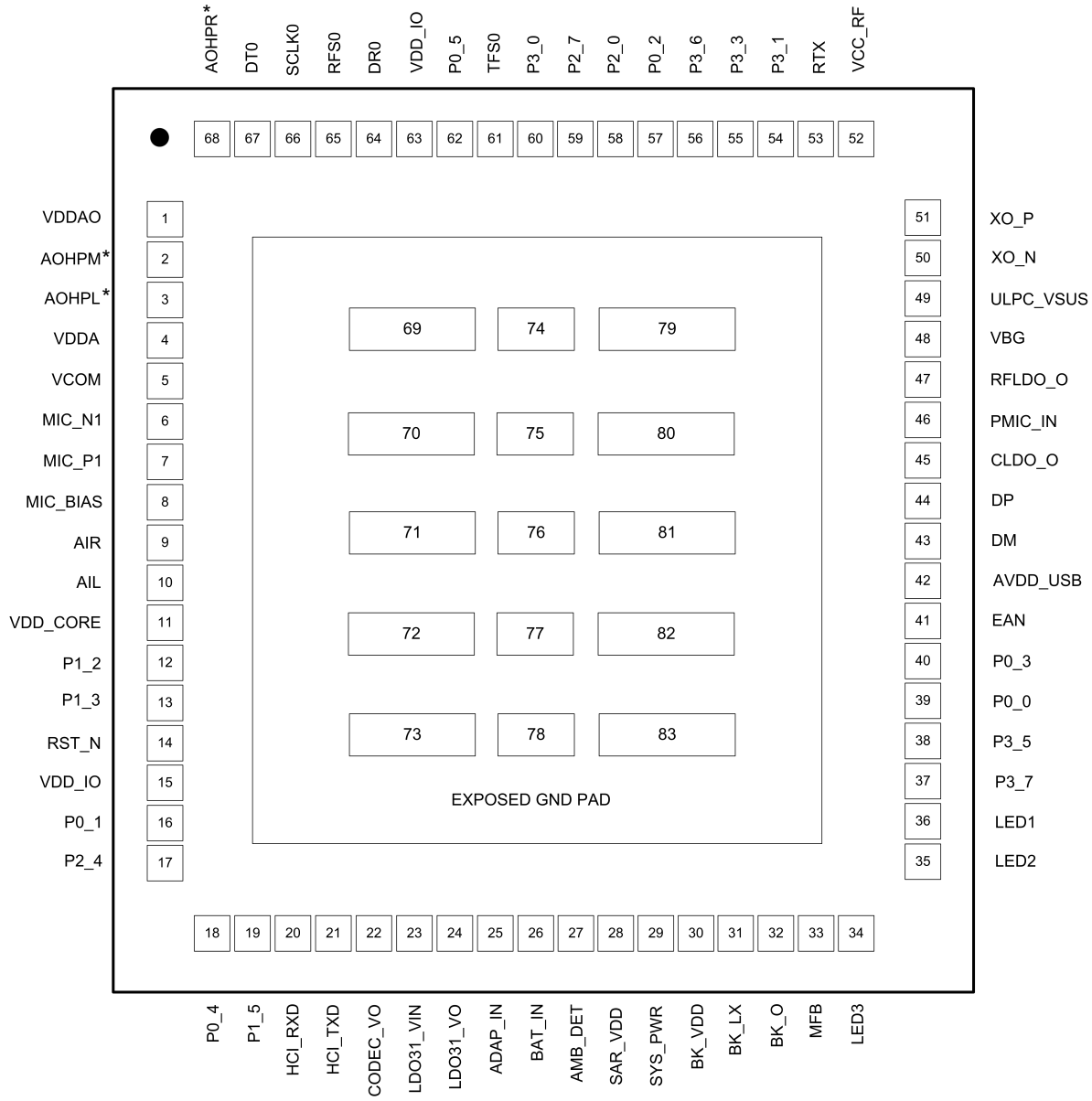
The following figure illustrates the pin diagram of the IS2062GM.

Figure 1-2. IS2062GM PIN DIAGRAM



The following figure illustrates the pin diagram of the IS2064GM.

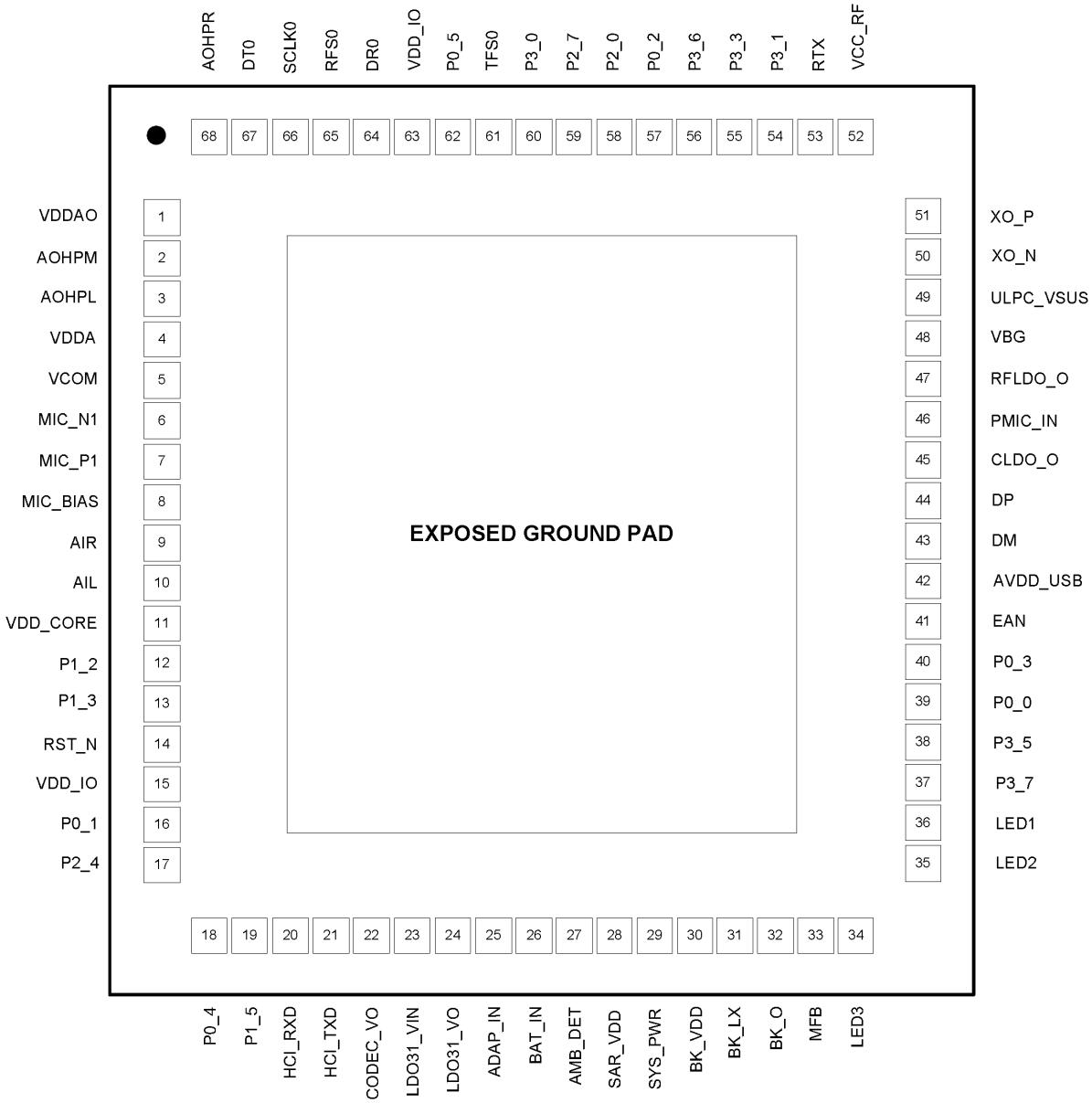
Figure 1-3. IS2064GM PIN DIAGRAM



1. IS2064GM-0L3 does not support an analog output from the DAC. The * on AOHPR, AOHPM, and AOHPL reflect the affected pins.

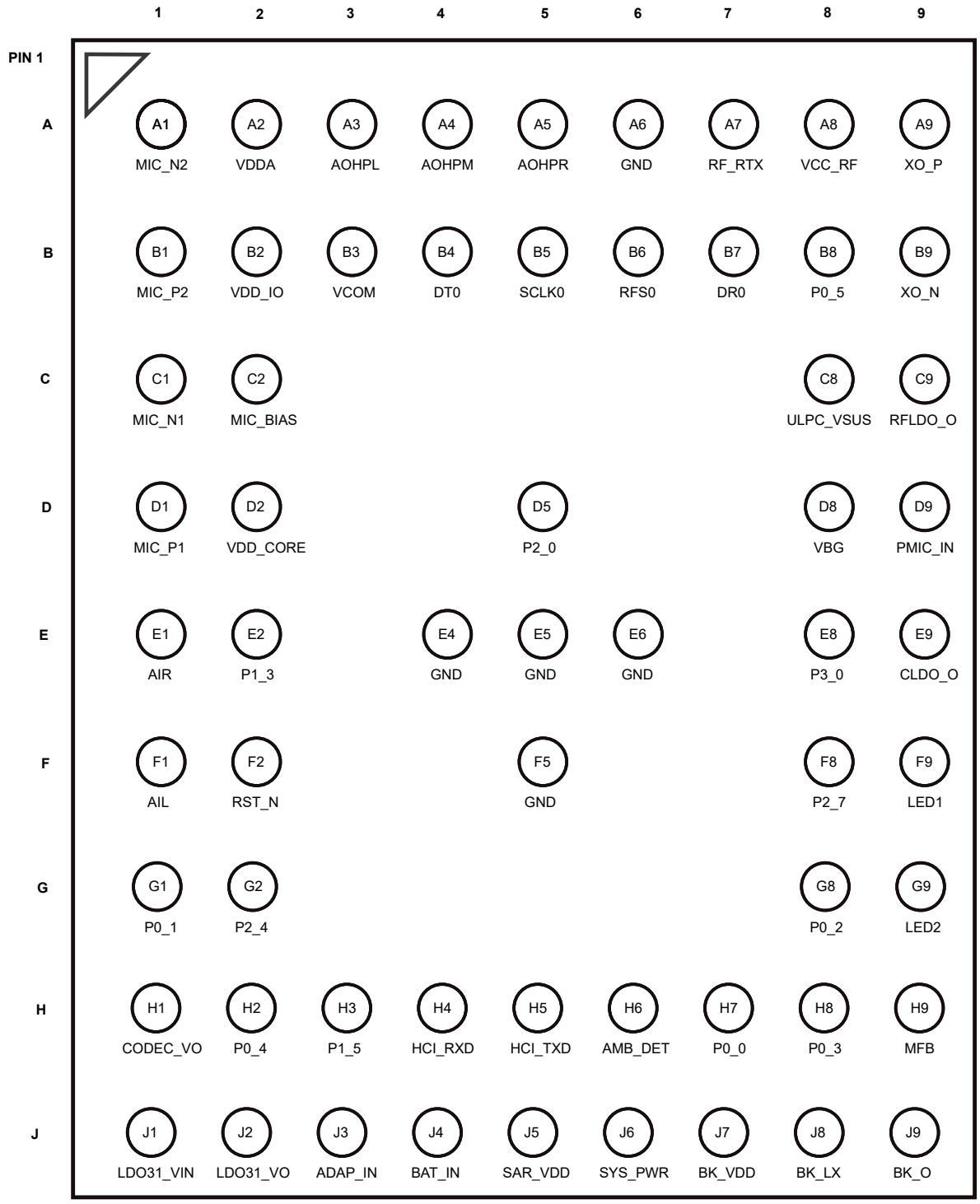
The following figure illustrates the pin diagram of the IS2064S.

Figure 1-4. IS2064S PIN DIAGRAM



The following figure illustrates the pin diagram of the IS2064B.

Figure 1-5. IS2064B PIN DIAGRAM



The following table provides the pin description of the IS2062GM, IS2064GM, IS2064S and IS2064B.

Note: The conventions used in the below table are indicated as follows:

- I = Input pin
- O = Output pin
- I/O = Input/Output pin

- P = Power pin

Table 1-2. PIN DESCRIPTION

IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
53	1	1	—	P	VDDAO	Power supply (3.0V to 3.6V) dedicated to codec output amplifiers; connect to CODEC_VO pin
54	2	—	A4	O	AOHPM	Headphone common mode output/sense input
55	3	—	A3	O	AOHPL	Left channel, analog headphone output
56	4	4	A2	P	VDDA	Analog reference voltage. Do not connect, for internal use only
1	5	5	B3	P	VCOM	Internal biasing voltage for codec, connect a 4.7 µF capacitor to ground
4	6	6	C1	I	MIC_N1	MIC1 mono differential analog negative input
5	7	7	D1	I	MIC_P1	MIC1 mono differential analog positive input
2	—	—	A1	I	MIC_N2	MIC2 mono differential analog negative input
3	—	—	B1	I	MIC_P2	MIC2 mono differential analog positive input
6	8	8	C2	P	MIC_BIAS	Electric microphone biasing voltage
7	9	9	E1	I	AIR	Right channel, single-ended analog input
8	10	10	F1	I	AIL	Left channel, single-ended analog input
9	11	11	D2	P	VDD_CORE	Core 1.2V power input; connect to CLDO_O pin; connect to GND through a 1 µF (X5R/X7R) capacitor
10	12	12	—	O	P1_2	I^2C SCL (Internal EEPROM clock), do not connect

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IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
11	13	13	E2	I/O	P1_3	I^2C SDA (Internal EEPROM data) requires external 4.7 kOhm pull-up resistor
12	14	14	F2	I	RST_N	System Reset (active-low)
13	15	15	B2	P	VDD_IO	I/O power supply input (3.0V to 3.6V); connect to LDO31_VO; connect to GND through a 1 µF (X5R/X7R) capacitor
14	16	16	G1	I/O	P0_1	Configurable control or indication pin (Internally pulled up, if configured as an input) • FWD key when Class 2 RF (default), active-low • Class 1 Tx control signal for external RF Tx/Rx switch, active-high
15	17	17	G2	I/O	P2_4	For IS2062GM/64GM (Flash variant): External address bus negative, System configuration pin along with the P2_0 and EAN pins can be used to set the SoC in any one of the following three modes: • Application mode (for normal operation) • Test mode (to change EEPROM values), and • Write Flash mode (to load a new firmware into the SoC), see Table 6-1 For IS2064S/B (ROM variant): Do not connect this pin
16	18	18	H2	I/O	P0_4	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Out_Ind_1

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IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
17	19	19	H3	I	P1_5	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Slide switch detector, active-high • Out_Ind_1 • Master/Slave mode control
18	20	20	H4	O	HCI_RXD	HCI UART data input
19	21	21	H5	I	HCI_TXD	HCI UART data output
20	22	22	H1	P	CODEC_VO	LDO output for codec power
21	23	23	J1	P	LDO31_VIN	LDO input, connect to SYS_PWR
22	24	24	J2	I	LDO31_VO	3V LDO output for VDD_IO power, do not calibrate
23	25	25	J3	P	ADAP_IN	5V power adapter input, used to charge the battery in case of Li-Ion battery power applications
24	26	26	J4	P	BAT_IN	Power Supply input. Voltage range: 3.2V to 4.2V. Source can either be a Li-Ion battery or any other power rail on the host board
25	27	27	H6	P	AMB_DET	Analog input for ambient temperature detection
26	28	28	J5	P	SAR_VDD	SAR 1.8V input; connect to BK_O pin
27	29	29	J6	P	SYS_PWR	System power output derived from the ADAP_IN or BAT_IN. Do not connect, for internal use only
28	30	30	J7	I	BK_VDD	1.8V buck VDD power input; connect to SYS_PWR pin
29	31	31	J8	I	BK_LX	1.8V buck regulator feedback path

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IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
30	32	32	J9	I	BK_O	1.8V buck regulator output. Do not connect to other devices. For internal use only
31	33	33	H9	P	MFB	• Multi-Function Button and power-on key • UART RX_IND, active-high (used by host MCU to wake up the Bluetooth system)
—	34	34	—	P	LED3	LED driver 3
33	35	35	G9	P	LED2	LED driver 2
32	36	36	F9	P	LED1	LED driver 1
—	37	37	—	P	P3_7	Configurable control or indication pin (Internally pulled-up, if configured as an input) • UART TX_IND, active-low (used by Bluetooth system to wake-up the host MCU)
—	38	38	—	P	P3_5	Configurable control or indication pin (Internally pulled-up, if configured as an input)
34	39	39	H7	I/O	P0_0	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Slide switch detector, active-high
35	40	40	H8	I/O	P0_3	Configurable control or indication pin (Internally pulled-up, if configured as an input) • REV key (default), active-low • Buzzer signal output • Out_Ind_2 • Class 1 Rx control signal of external RF T/R switch, active-high

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IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
36	41	41	—	I/O	EAN	For IS2062GM/64GM (Flash variant): External address-bus negative System configuration pin along with the P2_0 and P2_4 pins can be used to set the SoC in any one of the following three modes: • Application mode (for normal operation) • Test mode (to change EEPROM values), and • Write Flash mode (to load a new firmware into the SoC), see Table 6-1 For IS2064S/B (ROM variant): Do not connect for this pin
—	42	42	—	P	AVDD_USB	USB power input; connect to LDO31_VO pin
—	43	43	—	I/O	DM	Differential data-minus USB
—	44	44	—	I/O	DP	Differential data-plus USB
37	45	45	E9	P	CLDO_O	1.2V core LDO output for internal use only. Connect to GND through a 1 µF capacitor
38	46	46	D9	P	PMIC_IN	1.8V power input for internal blocks; connect to BK_O
39	47	47	C9	P	RFLDO_O	1.28V RF LDO output for internal use only. Connect to GND through a 1 µF capacitor
40	48	48	D8	P	VBG	Bandgap output reference for decoupling interference, connect to GND through a 1 µF capacitor
41	49	49	C8	P	ULPC_VSUS	ULPC 1.2V output power, maximum loading 1 mA, connect to GND through a 1 µF capacitor
42	50	50	B9	I	XO_N	16 MHz crystal input negative

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IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
43	51	51	A9	I	XO_P	16 MHz crystal input positive
44	52	52	A8	P	VCC_RF	RF power input (1.28V) for both synthesizer and Tx/Rx block, connect to RFLDO_O
45	53	53	A7	I/O	RTX/ RF_RTX	RF path (transmit/receive)
—	54	54	—	I/O	P3_1	Configurable control or indication pin (Internally pulled-up, if configured as an input) • REV key when Class 1 RF (default), active-low
—	55	55	—	I/O	P3_3	Configurable control or indication pin (Internally pulled-up, if configured as an input) • FWD key when Class 1 RF (default), active-low
—	56	56	—	I/O	P3_6	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Master/Slave mode control
46	57	57	G8	I/O	P0_2	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Play/Pause key (default)

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IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
47	58	58	D5	I/O	P2_0	For IS2062GM/64GM (Flash variant): External address-bus negative System configuration pin along with the P2_4 and EAN pins can be used to set the SoC in any one of the following three modes: • Application mode (for normal operation) • Test mode (to change EEPROM values), and • Write Flash mode (to load a new firmware into the SoC), see Table 6-1 For IS2064S/B (ROM variant): Do not connect for this pin
48	59	59	F8	I/O	P2_7	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Volume up key (default), active-low
49	60	60	E8	I/O	P3_0	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Auxiliary input detector, active-low
—	61	61	—	I/O	TFS0	I^2S interface: left/right clock
50	62	62	B8	I/O	P0_5	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Volume down key (default), active-low
51	63	63	B2	P	VDD_IO	I/O power supply input (3V to 3.6V); connect to LDO31_VO pin, connect to GND through a 1 µF (X5R/X7R) capacitor

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IS2062GM Pin No	IS2064GM-012 and IS2064S Pin No	IS2064GM-0L3 Pin No	IS2064B Ball No	Pin Type	Pin Name	Description
—	64	64	B7	I/O	DR0	I^2S interface: digital left/right data
—	65	65	B6	I/O	RFS0	I^2S interface: left/right clock
—	66	66	B5	I/O	SCLK0	I^2S interface: bit clock
—	67	67	B4	I/O	DT0	I^2S interface: digital left/right data
52	68	—	A5	O	AOHPR	Right-channel, analog headphone output
57-64	69-83	69-83	—	P	EP	Exposed pads, Used as ground (GND) pins
—	—	—	A6, E4, E5, E6, F5	P	GND	Ground reference

Note: All I/O pins are configured using UI tool, a Windows® based utility.

2. Audio

The input and output audio signals have different stages and each stage is programmed to vary the gain response characteristics. For microphones, both single-ended inputs and differential inputs are supported. To maintain a high quality signal, a stable bias voltage source to the condenser microphone's FET is provided. The DC blocking capacitors are used at both positive and negative sides of the input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

2.1 Digital Signal Processor

A Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as acoustic echo cancellation and noise reduction, are built-in. To reduce nonlinear distortion and to help echo cancellation, an outgoing signal level to the speaker is monitored and adjusted to avoid saturation of speaker output or microphone input. To provide an echo free and full-duplex user experience, adaptive filtering is also applied to track the echo path impulse in response.

The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by microphones and improves mutual understanding in communication. The advanced audio features, such as multi-band dynamic range control, parametric multi-band equalizer, audio widening and virtual bass are built-in. The audio effect algorithms improve the user's audio listening experience in terms of better quality audio after audio signal processing.

The following figures illustrate the processing flow of speaker phone applications for speech and audio signal processing.

Figure 2-1. SPEECH PROCESSING

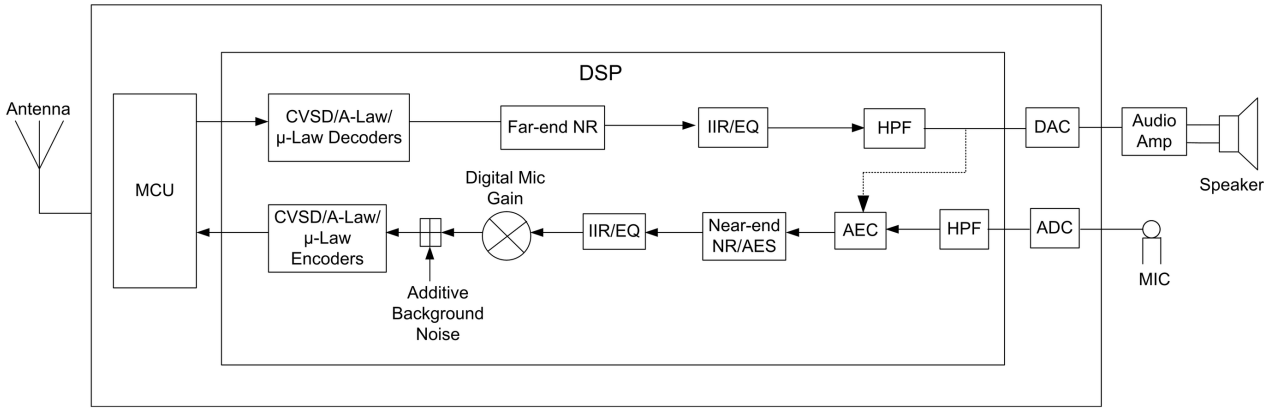
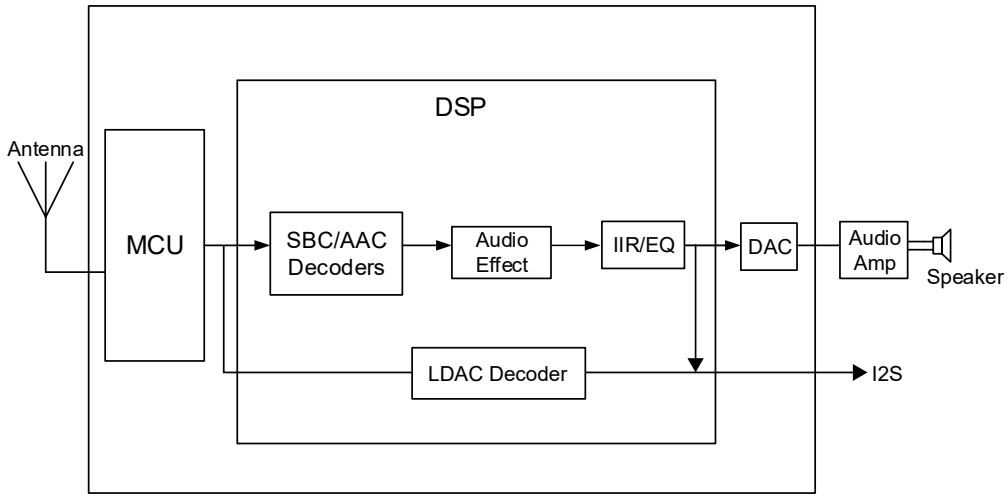


Figure 2-2. AUDIO PROCESSING



1. LDAC decoder in the preceding figure is supported only in the IS2064GM-0L3 variant.

For SBC and AAC audio data, the DSP parameters such as EQ, Speaker Gain, Mic Gain, Sound Effect etc. are configured using the DSP tool. For additional information on the DSP tool, refer to the *"IS206x DSP Application Note*".

Note: The DSP tool and *IS206x DSP Application Note* are available for download from the Microchip website at http://www.microchip.com/wwwproducts/en/IS2062 and http://www.microchip.com/wwwproducts/en/IS2064.

2.2 Codec

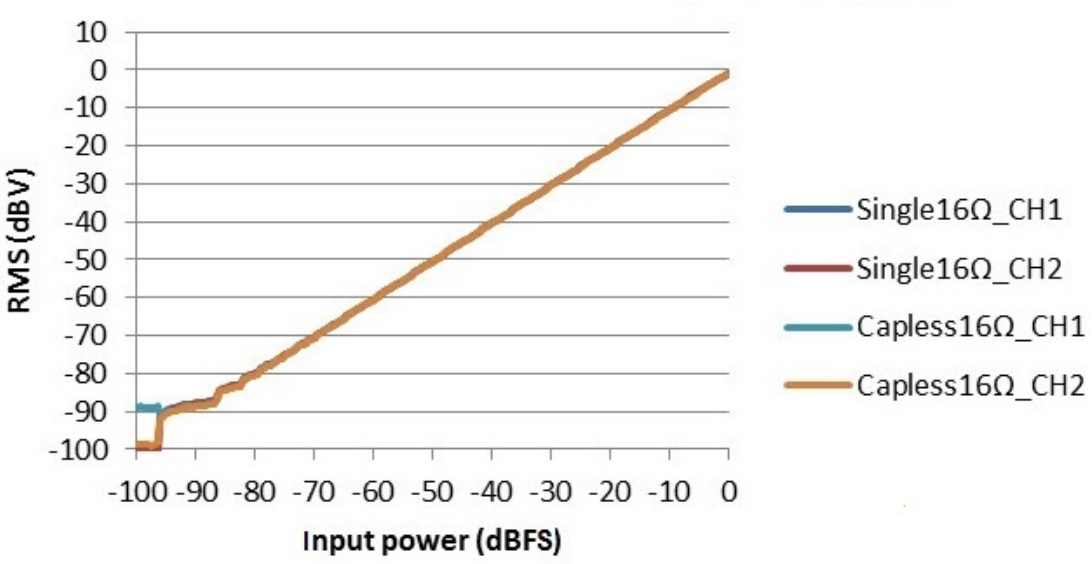
The built-in codec has a high Signal-to-Noise Ratio (SNR) performance and it consists of an ADC, a DAC and additional analog circuitry.

Note: The internal DAC is not supported in the IS2064GM-0L3 variant.

Note: The internal DAC supports 16-bit resolution. 24-bit I^2S port requirements are met by adding trailing zeros in LSBs.

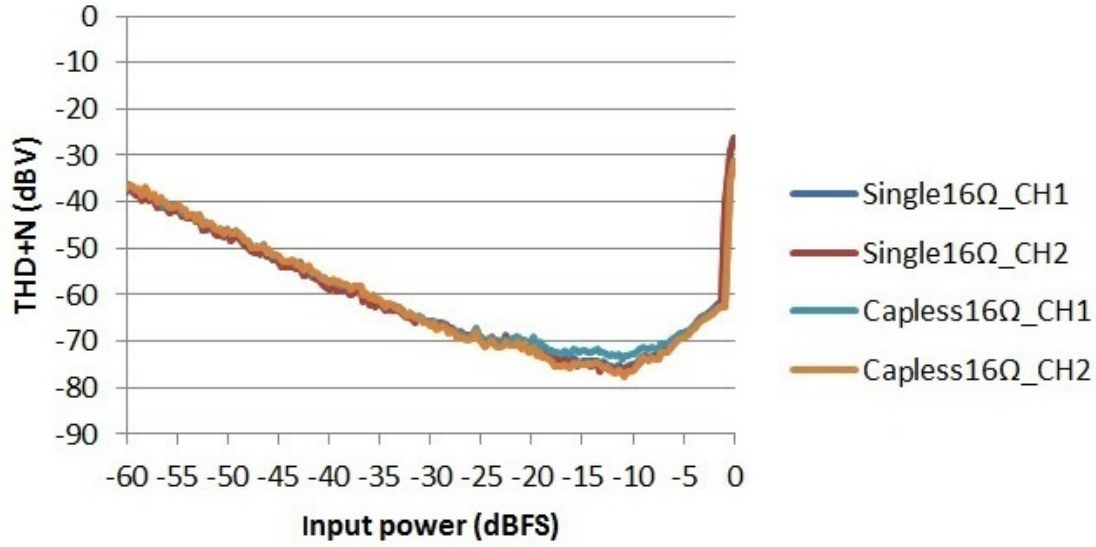
The following figures illustrate the dynamic range and frequency response of the codec.

Figure 2-3. CODEC DAC DYNAMIC RANGE



Note: The data corresponds to the 16 Ohm load with 2.8V operating voltage and +25°C operating temperature.

Figure 2-4. CODEC DAC THD+N VERSUS INPUT POWER



Note: The data corresponds to the 16 Ohm load with 2.8V operating voltage and +25°C operating temperature.

Figure 2-5. CODEC DAC FREQUENCY RESPONSE (CAPLESS MODE)

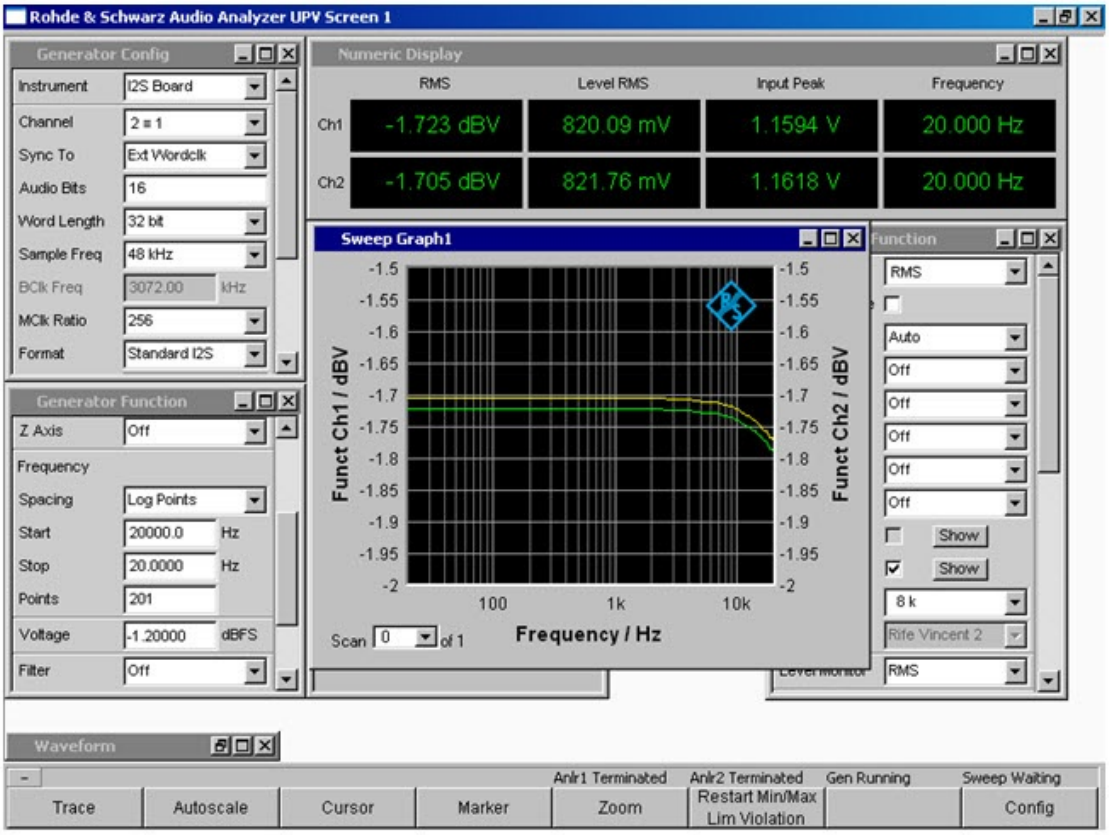
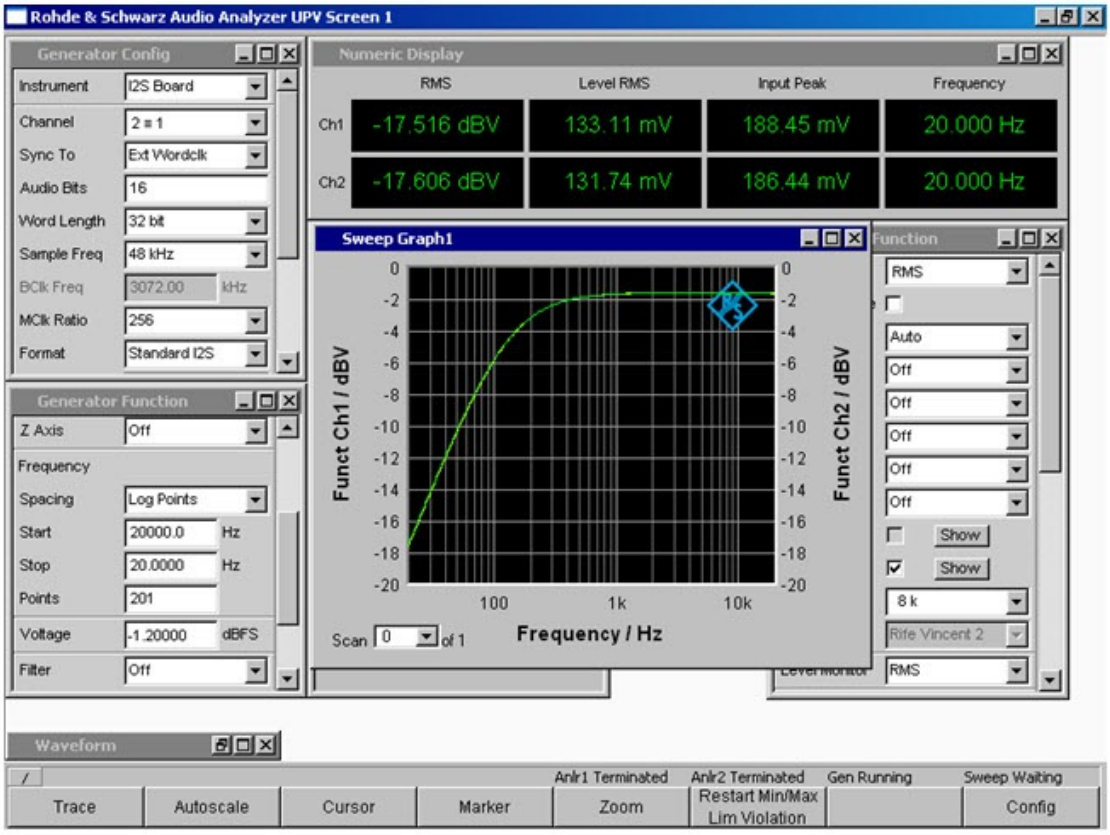


Figure 2-6. CODEC DAC FREQUENCY RESPONSE (SINGLE-ENDED MODE)



Note: The DAC frequency response corresponds to Single-Ended mode with a 47 µF DC block capacitor.

2.3 Auxiliary Port

The SoC supports one analog (line-in) signal from the external audio source. The analog signal is processed by the DSP to generate different sound effects (multi-band dynamic range compression and audio widening), which are configured using the DSP tool.

2.4 Analog Speaker Output

The IS2062/64 SoC (except IS2064GM-0L3) supports the following speaker output modes:

- Capless mode — Recommended for headphone applications in which capless output connection helps to save the BOM cost by avoiding a large DC blocking capacitor. Figure 2-7 illustrates the analog speaker output Capless mode.
- Single-Ended mode — Used for driving an external audio amplifier, where a DC blocking capacitor is required. Figure 2-8 illustrates the analog speaker output Single-Ended mode.

Figure 2-7. ANALOG SPEAKER OUTPUT CAPLESS MODE

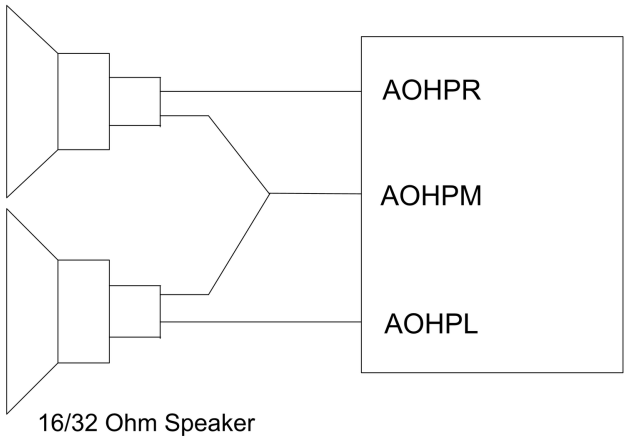
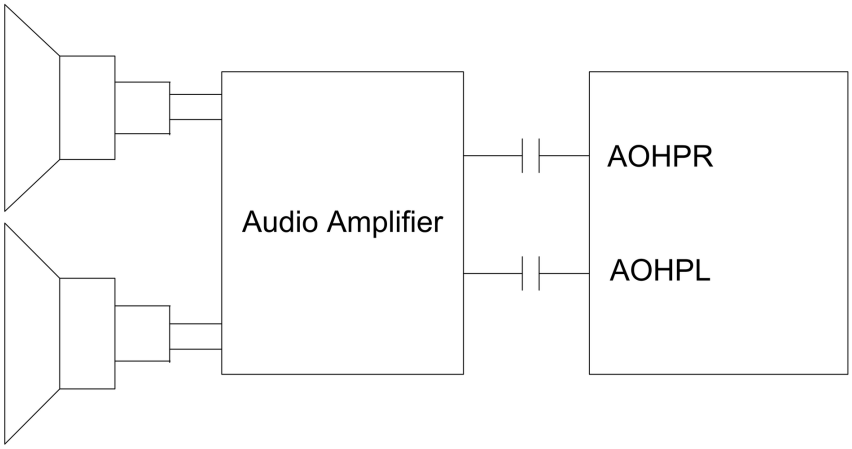


Figure 2-8. ANALOG SPEAKER OUTPUT SINGLE-ENDED MODE



3. Transceiver

The SoC is designed and optimized for Bluetooth 2.4 GHz systems. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock to synchronize with another device.

3.1 Transmitter

The internal Power Amplifier (PA) has a maximum output power of +4 dBm. This is applied to Class 2 or Class 3 radios, without an external RF PA. The transmitter directly performs the IQ conversion to minimize the frequency drift.

3.2 Receiver

The Low-Noise Amplifier (LNA) operates with TR-combined mode for the single port application. It saves the pin on the package without having an external Tx/Rx switch.

The ADC is used to sample the input analog signal and convert it into a digital signal for demodulator analysis. A channel filter is integrated into a receiver channel before the ADC to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject the image frequency for the low-IF architecture, and it also intended to reduce external Band Pass Filter (BPF) component for a super heterodyne architecture.

The Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

3.3 Synthesizer

A synthesizer generates a clock for radio transceiver operation. The VCO inside, with a tunable internal LC tank, can reduce any variation for components. A crystal oscillator with an internal digital trimming circuit provides a stable clock for the synthesizer.

3.4 Modem

For Bluetooth 1.2 specification and below, 1 Mbps is the standard data rate based on the Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with EDR specifications.

For Bluetooth 2.0 and above specifications, EDR is introduced to provide the data rates of 1/2/3 Mbps. For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of EDR packets represent 2-bit or 3-bit. This is achieved by using two different modulations, π/4 DQPSK and 8 DPSK.

3.5 Adaptive Frequency Hopping (AFH)

The SoC has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose the clear channel for transceiver Bluetooth signal.

4. Microcontroller

A single-cycle 8-bitmicrocontroller is built into the SoC to execute the Bluetooth protocols. It operates from 16 MHz to higher frequencies, where the firmware dynamically adjusts the trade-off between the computing power and the power consumption. In the ROM version, the MCU firmware is hard-wired to minimize power consumption for the firmware execution and to save the external Flash cost.

4.1 Memory

There are sufficient ROM and RAM to fulfill the processor requirements, in which a synchronous single port RAM interface is used. The register bank, dedicated single port memory and Flash memory are connected to the processor bus. The processor coordinates with all link control procedures and the data movement happens using a set of pointer registers.

4.2 External Reset

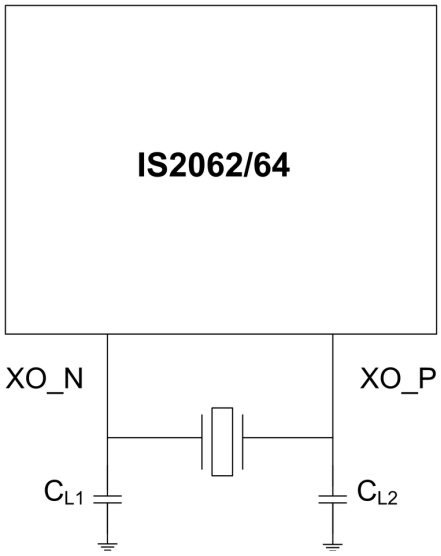
The IS2062/64 SoC provides a Watchdog Timer (WDT) to reset the SoC. It has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power-on state. This action is also driven by an external Reset signal, which is used to control the device externally by forcing it into a POR state. The RST_N signal input is active-low and no connection is required in most of the applications.

4.3 Reference Clock

The IS2062/64 SoC is composed of an integrated crystal oscillation function that uses a 16 MHz±10 ppm external crystal and two specified loading capacitors to provide a high quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors, which are associated with the crystal and its equivalent loading capacitance in the mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors (C_{trim}).

The value of trimming capacitance is 200 fF ($200x10^{-15}$ F) per LSb at 5-bit word and the overall adjustable clock frequency is ±40 kHz (based on the crystal with load capacitance, C_L spec = 9 pF). The following figure illustrates the crystal connection of the IS2062/64 SoC with two capacitors.

Figure 4-1. CRYSTAL CONNECTION



Note:

1. C_{trim}= 200 fF * (1 to 31); C_{int} = 3 pF.
2. C_L= [C_{L1} x C_{L2})/(C_{L1}+C_{L2})]+(C_{trim}/2)+C_{int} (set trim value as 16, then C_{trim} = 3.2 pF).
3. For a 16 MHz crystal, in which C_L= 9 pF, then the C_{L1} = C_{L2} = 9.1 pF).
4. For C_L selection, refer to the data sheet of the crystal.

5. Power Management Unit

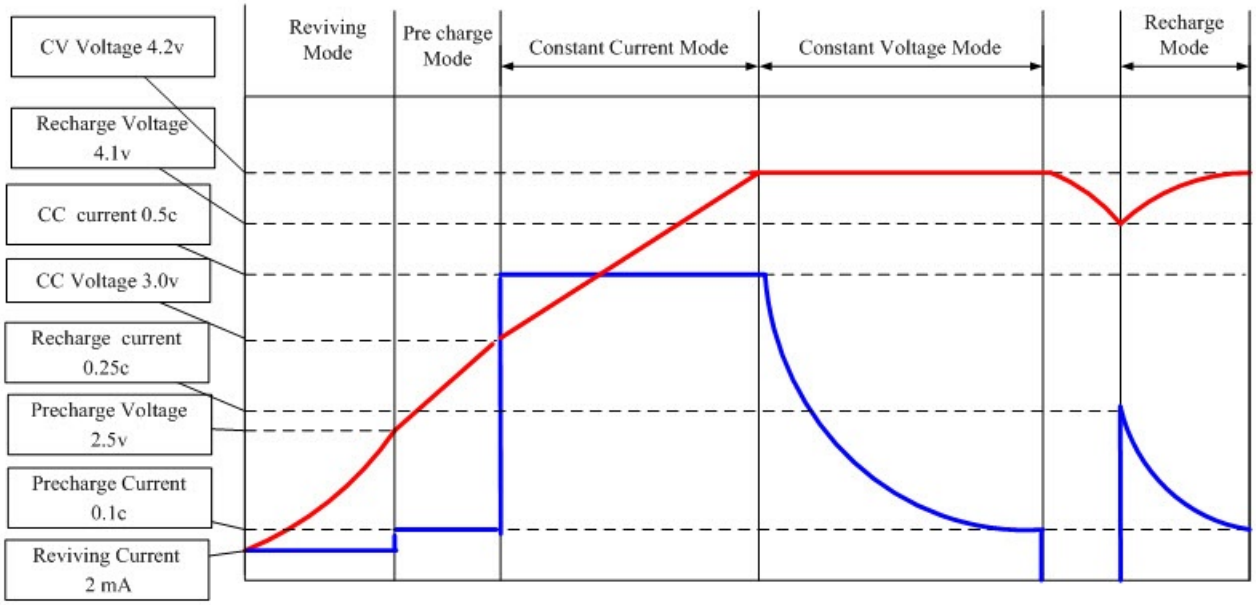
The IS2062/64 SoC has an integrated Power Management Unit (PMU). The main features of the PMU are a lithium-ion and lithium-polymer battery charger, and a voltage regulator. The power switch is used to exchange the power source between a battery and an adaptor. Also, the PMU provides current to the LED drivers.

5.1 Charging a Battery

The IS2062/64 SoC has a built-in battery charger, which is optimized with lithium-ion and lithium-polymer batteries. The battery charger includes a current sensor for charging control, user programmable current regulator, and high accuracy voltage regulator.

The charging current parameters are configured by using the UI tool. An adapter is plugged in to activate the charging circuit. Reviving, pre-charging, constant current and constant voltage modes and re-charging functions are included. The maximum charging current is 350 mA. The following figure illustrates the charging curve of a battery.

Figure 5-1. BATTERY CHARGING CURVE



5.2 Voltage Monitoring

A 10-bit, successive approximation register ADC (SAR ADC) provides a dedicated channel for battery voltage level detection. The warning level is programmed by using the UI tool. The ADC provides a granular resolution to enable the MCU to take control over the charging process.

5.3 Low Dropout Regulator

A built-in Low Dropout (LDO) Regulator is used to convert the battery or adaptor power for power supply. It also integrates the hardware architecture to control the power-on/off procedure. The built-in

programmable LDOs provide power for codec and digital I/O pads. Also, it is used to buffer the high input voltage from battery or adapter. This LDO requires 1 µF bypass capacitor.

5.4 Switching Regulator

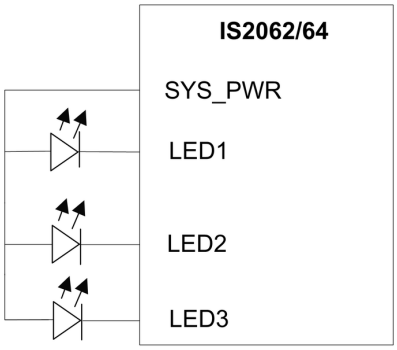
The built-in programmable output voltage regulator converts the battery voltage to RF and baseband core power supply. This converter has a high conversion efficiency and a fast transient response.

5.5 LED Driver

The IS2062GM and IS2064B have two LED drivers, and the IS2064GM and IS2064S have three LED drivers to control the LEDs. The LED drivers provide enough sink current (16-step control and 0.35 mA for each step) and the LED is connected directly to the IS2062/64 SoC. The LED settings are configured using the UI tool.

The following figure illustrates the LED driver in the IS2062/64 SoC.

Figure 5-2. LED DRIVER



5.6 Under Voltage Protection

When the voltage of SYS_PWR pin drops below the voltage level of 2.9V, the system shuts down automatically.

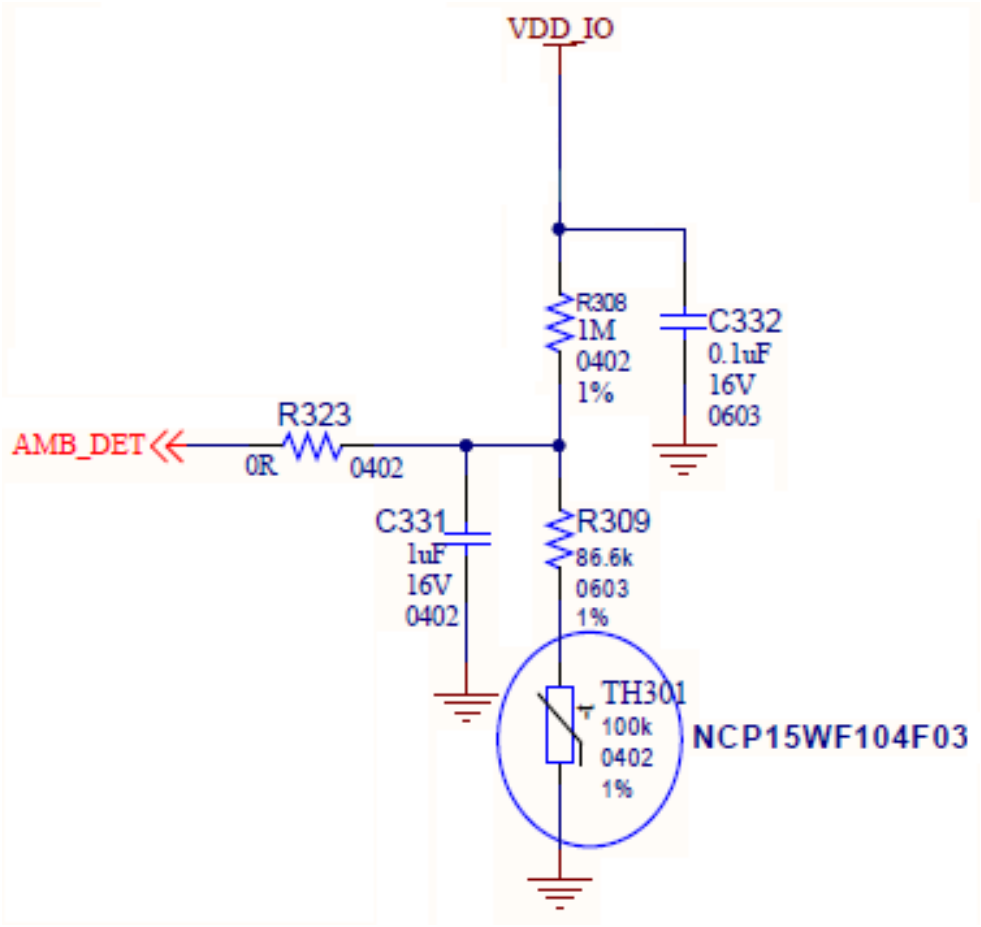
5.7 Ambient Detection

The IS2062/64 SoC contains a built-in ADC for charger thermal protection.

The following figure illustrates the suggested circuit and thermistor, Murata NCP15WF104F. The charger thermal protection avoids battery charge in the restricted temperature range. The upper and lower limits for temperature values are configured by using the UI tool.

Note: The thermistor must be placed close to the battery in the user application for accurate temperature measurements and to enable the thermal shutdown feature.

Figure 5-3. AMBIENT TEMPERATURE DETECTOR



6. Application Information

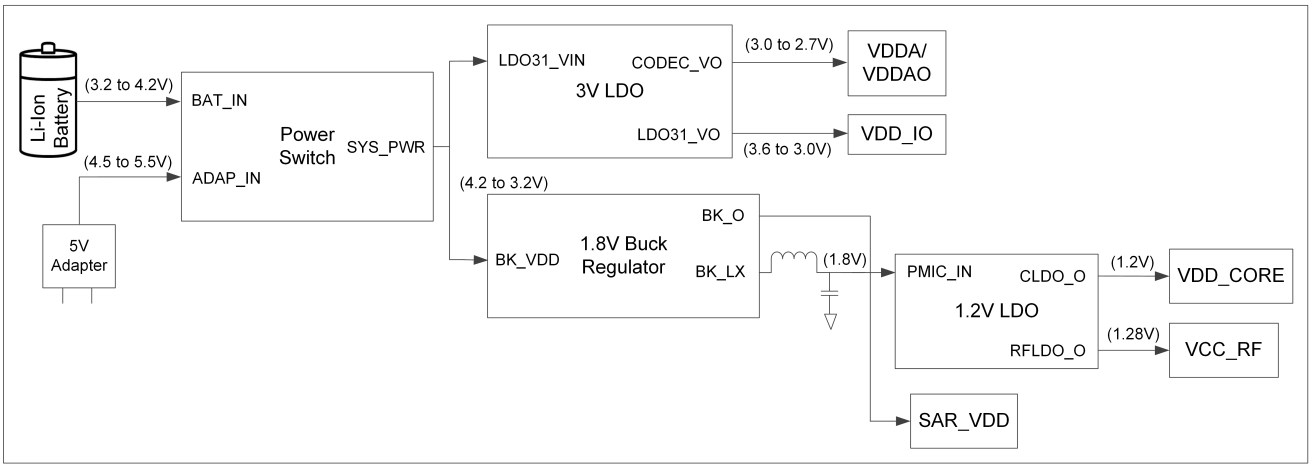
This section describes the power supply connection, host MCU UART interface, and various modes in detail.

6.1 Power Supply

The following figure illustrates the connection from the BAT_IN pin to various other voltage supply pins of the IS2062/64 SoC.

The IS2062/64 SoC is powered through the BAT_IN input pin. The external 5V power adapter can be connected to ADAP_IN in order to charge the battery.

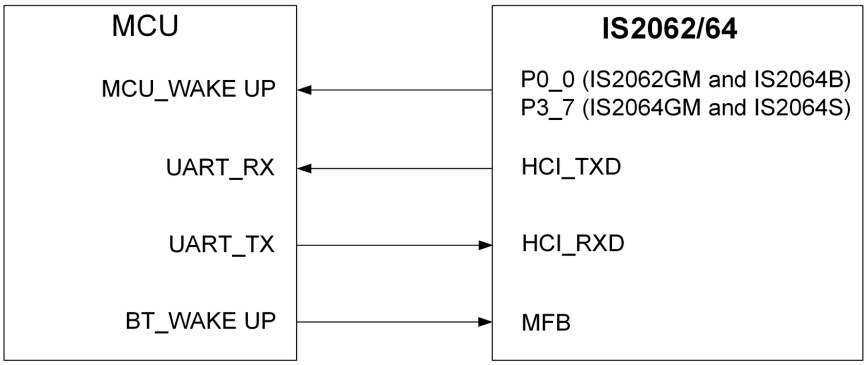
Figure 6-1. POWER TREE DIAGRAM



6.2 Host MCU Interface

The following figure illustrates the UART interface between the IS2062/64 SoC and an external MCU.

Figure 6-2. HOST MCU INTERFACE OVER UART



The MCU controls the IS2062/64 SoC over the UART interface and wakes up the SoC using the MFB, P0_0 (IS2062GM and IS2064B) and P3_7 (IS2064GM and IS2064S) pins.

Refer to the "*UART_CommandSet*" document for a list of functions that the IS2062/64 SoC supports and how to use the UI tool to set up the system using the UART command.

Note: The "*UART_CommandSet*" document is available for download from the Microchip website at http://www.microchip.com/wwwproducts/en/IS2062 and http://www.microchip.com/wwwproducts/en/IS2064.

The following figures illustrate the various UART control signal timing sequences.

Figure 6-3. POWER-ON/OFF SEQUENCE

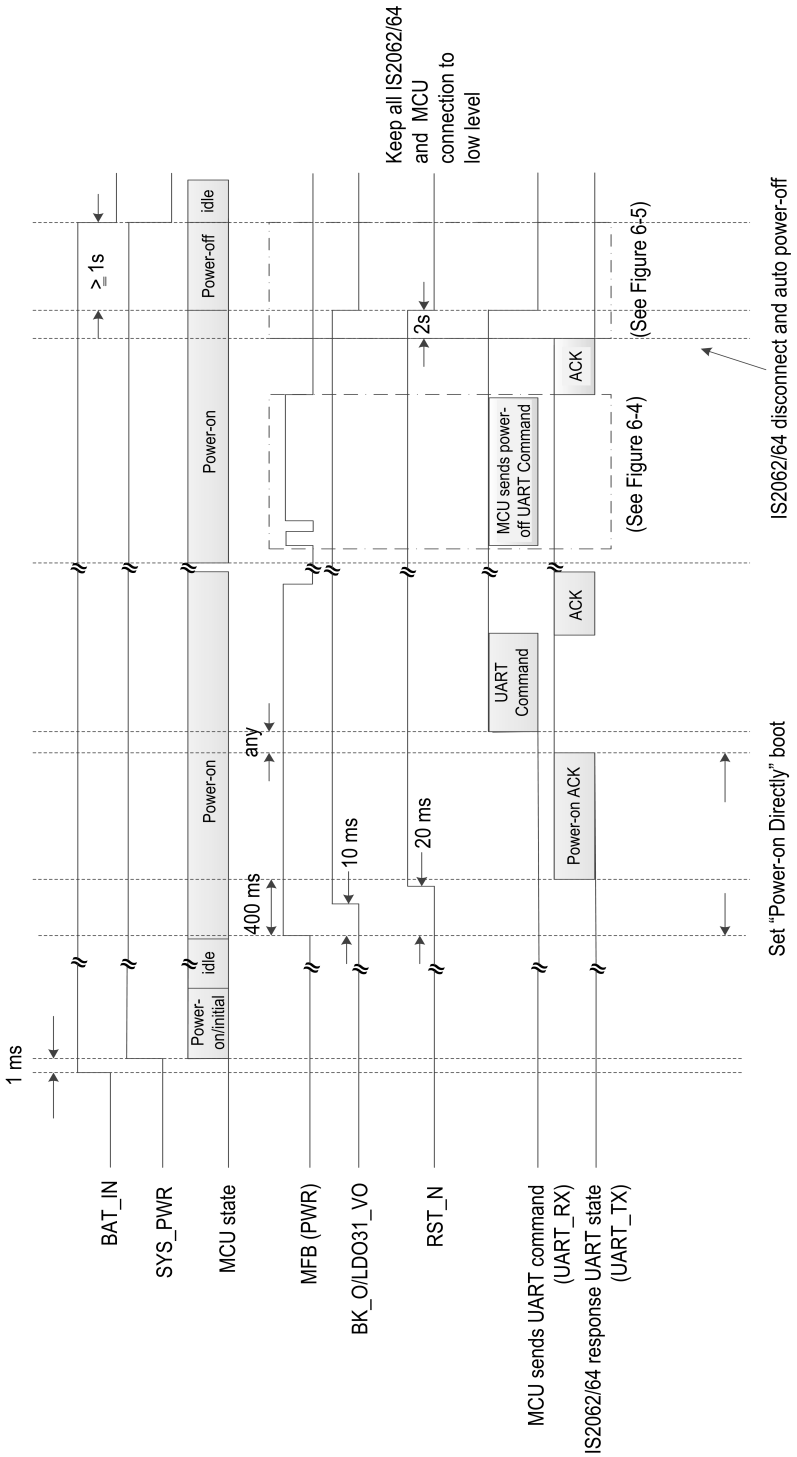


Figure 6-4. TIMING SEQUENCE OF RX INDICATION AFTER POWER-ON

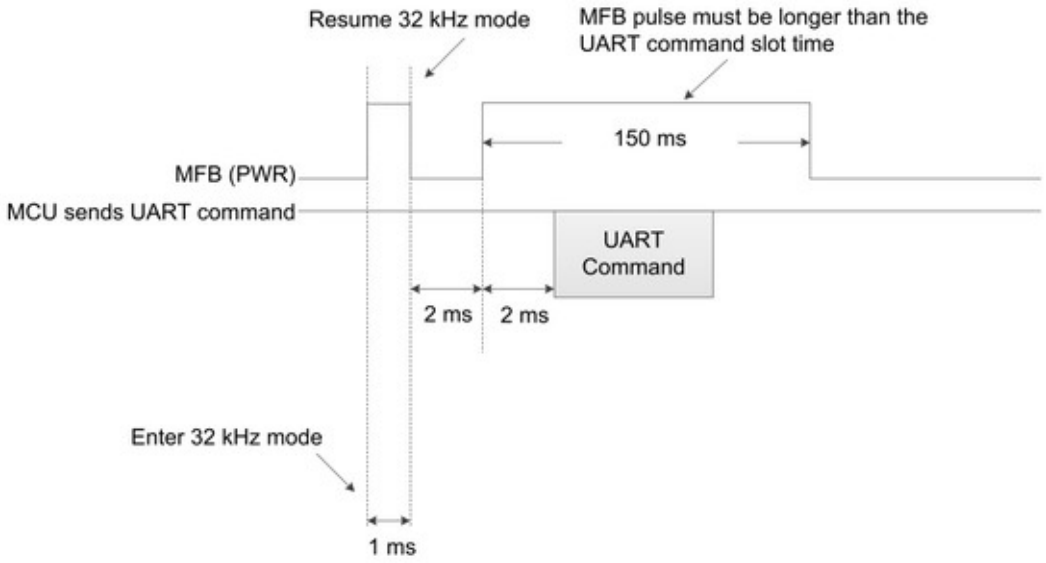
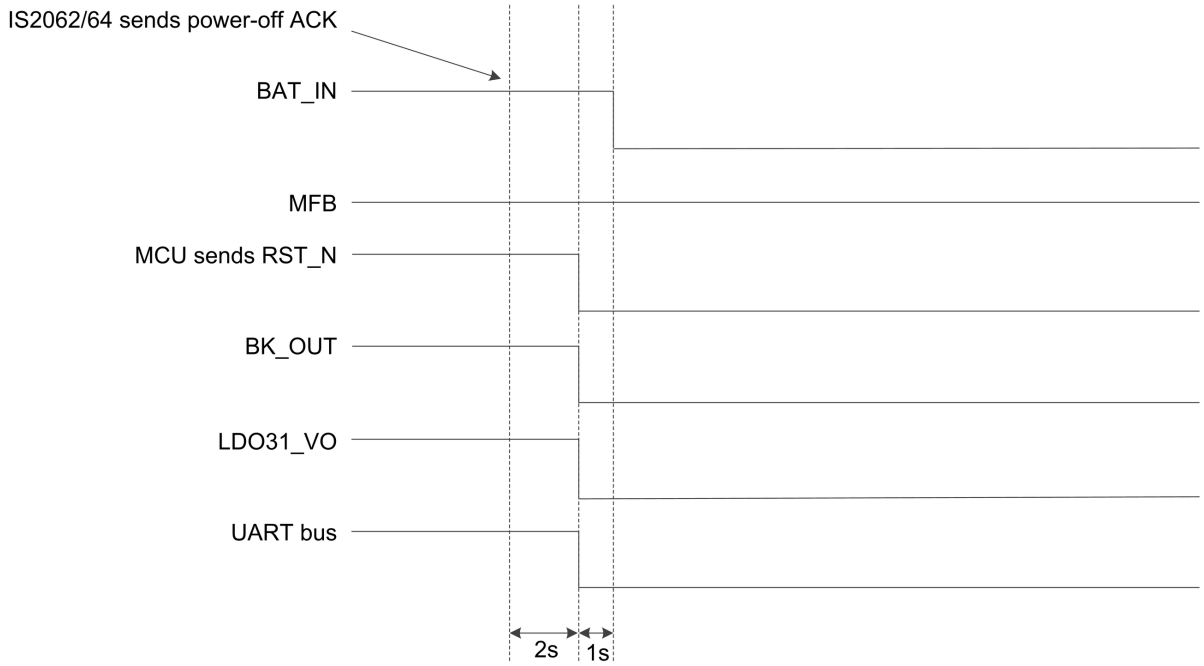


Figure 6-5. TIMING SEQUENCE OF POWER-OFF



Note:

1. EEPROM clock = 100 kHz.
2. For a byte wire, 0.01 ms x 32 clock x 2 = 640 µs.
3. It is recommended to have ramp-down time more than 640 µs during the power-off sequence to ensure safe operation of the device.

Figure 6-6. TIMING SEQUENCE OF POWER-ON (NACK)

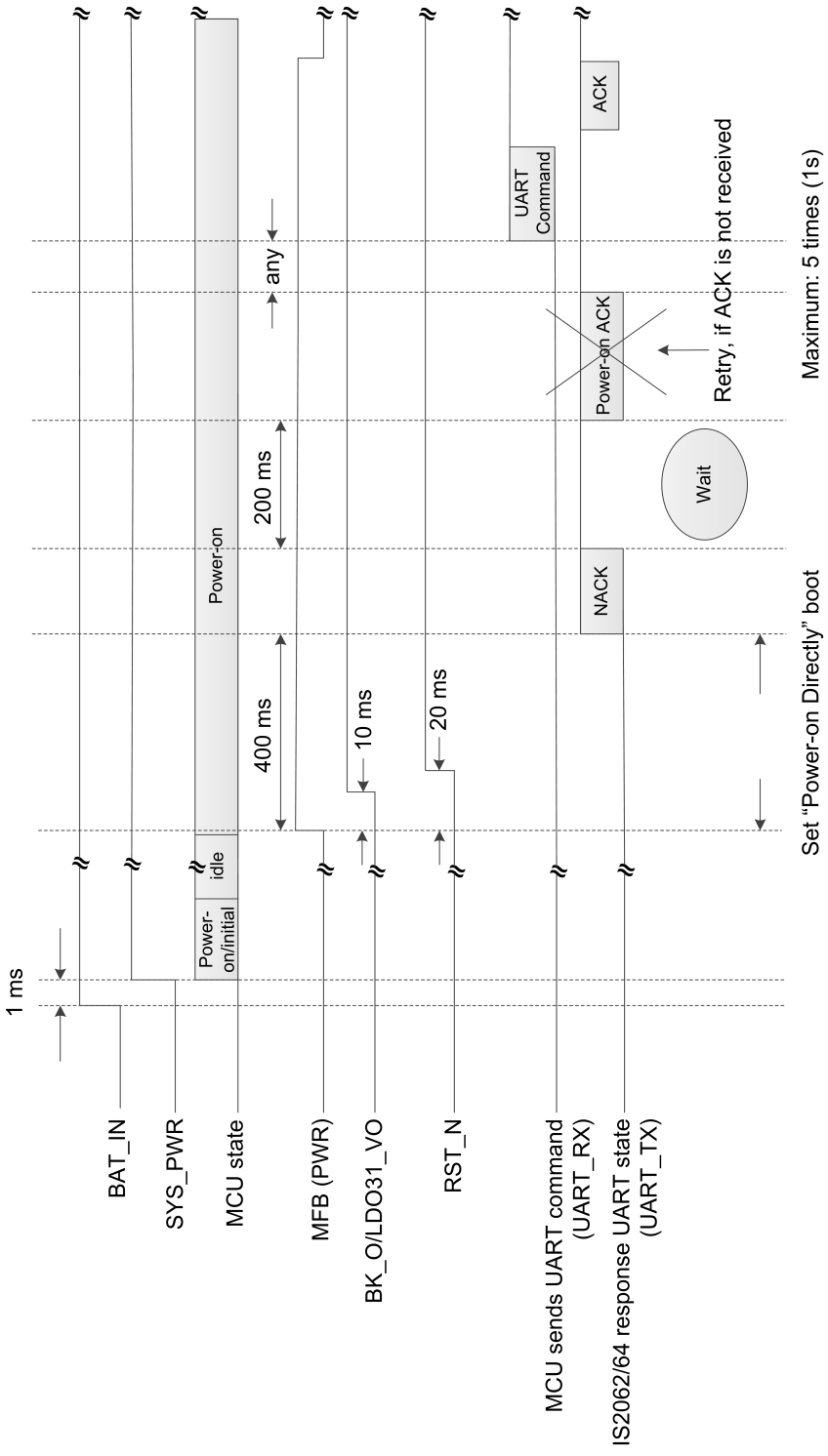
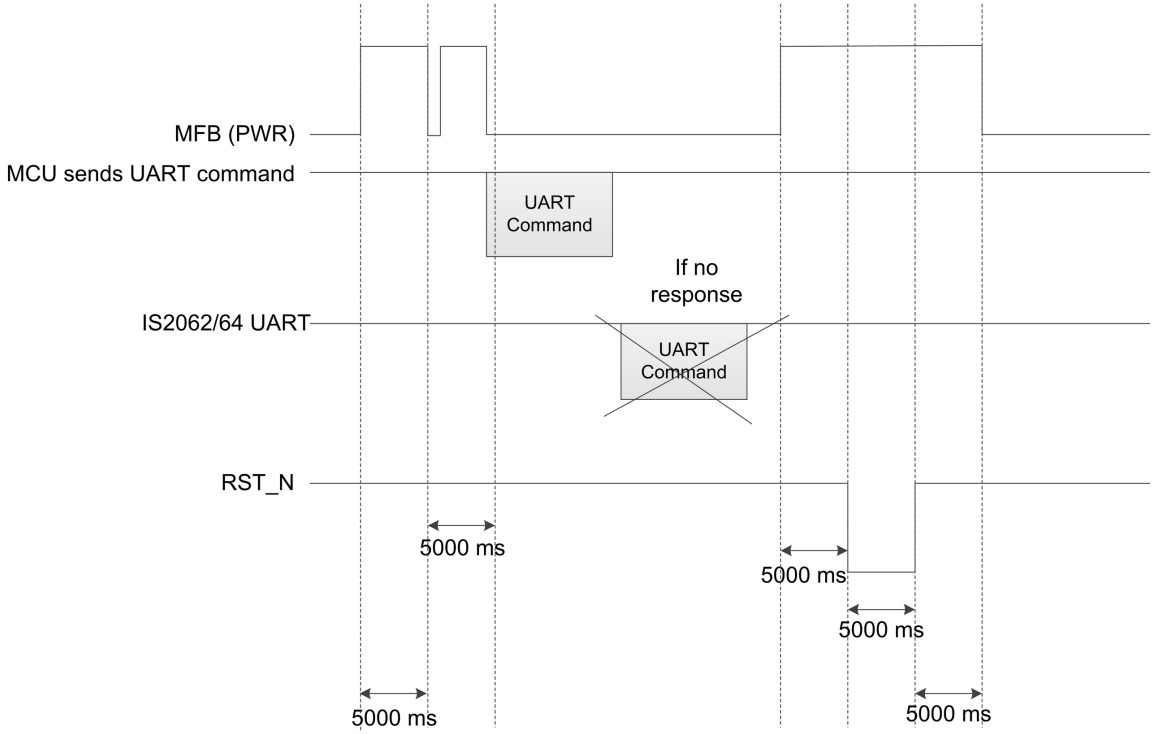
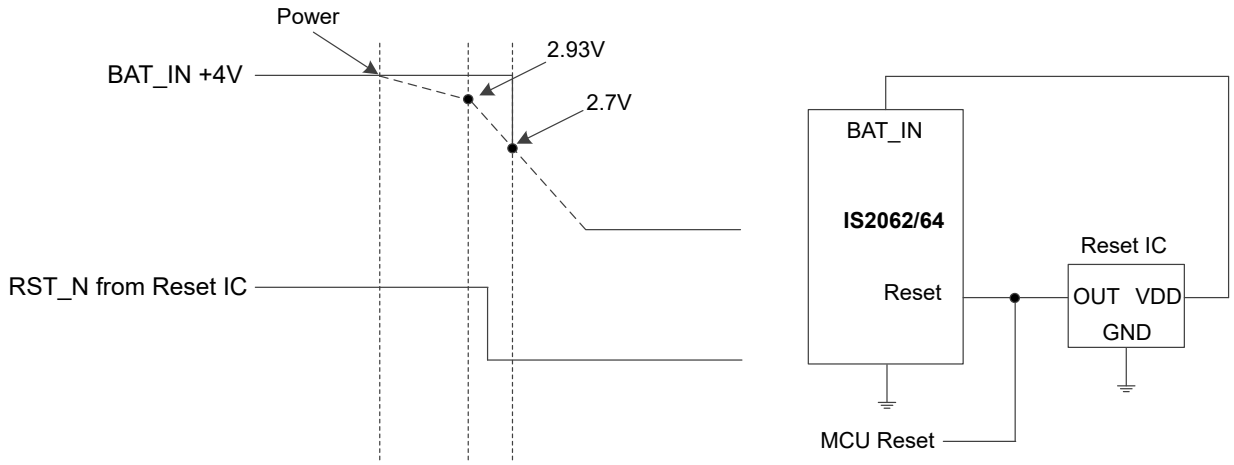


Figure 6-7. RESET TIMING SEQUENCE IN CASE OF NO RESPONSE FROM SoC TO HOST MCU



Note: The MCU sends the UART command again, when SoC is not responding to its first UART command. If the SoC is not responding to the second UART command within 5 secs, then the MCU forces the system to Reset.

Figure 6-8. TIMING SEQUENCE OF POWER DROP PROTECTION



Note:

1. It is recommended to connect the battery on a BAT_IN pin of the SoC for power supply.
2. If an external power source or a power adapter is utilized to provide the power to the SoC (ADAP_IN), use a voltage supervisor IC.
3. The Reset IC output pin, RST_N, must be “Open drain” type and threshold voltage as 2.93V.
4. The RST_N signal must be fully pulled to low before BAT_IN power drop to 2.7V.

6.3 Configuration and Firmware Programming

Configuration and Firmware Programming modes are entered according to the system configuration I/O pins. The following table provides the system configuration settings. The P2_0 and P2_4 pins have internal pull-up.

Table 6-1. SYSTEM CONFIGURATION SETTINGS

P2_0	P2_4	EAN	Operating mode
High	High	Low	Flash Application mode
High	High	High	ROM Application mode
Low	High	Low	Flash Test mode (EEPROM programming)
Low	High	High	ROM Test mode (Flash programming)
Low	Low	High	Boot mode (Flash programming)

6.4 General Purpose I/O pins

The following table provides the details of various functions that are mapped to the I/O pins of IS2062/64 SoC and these I/Os are configured by using the UI tool.

Note: The MFB pin must be configured as the power-on/off key and the remaining pins are configured for any one of the default functions, as provided in the following table.

Table 6-2. I/O PIN CONFIGURATION

S.No	Pin Name	IS2062GM and IS2064B	IS2064GM and IS2064S
1	MFB	Button 0 UART_RX_IND	Button 0 UART_RX_IND
2	P0_0	UART_TX_IND Slide Switch	UART_TX_IND Slide Switch
3	P0_1	Button 4 (FWD) CLASS1 TX	Button 4 (FWD) CLASS1 TX
4	P0_2	Button 1 (Play/Pause)	Button 1 (Play/Pause)
5	P0_3	Button 5 (REV) Buzzer Output Ind.1 CLASS1 RX	Button 5 (REV) Buzzer Output Ind.1 CLASS1 RX
6	P0_4	Output Ind.0 External Amplifier Enable	Output Ind.0 External Amplifier Enable
7	P0_5	Button 3 (VOL-)	Button 3 (VOL-)

.....continued

S.No	Pin Name	IS2062GM and IS2064B	IS2064GM and IS2064S
8	P1_5	Output Ind.0 Slider Switch External Amplifier Enable Twin Role setting1	Output Ind.0 Slider Switch External Amplifier Enable Twin Role setting1
9	P2_0	System Configuration Buzzer	System Configuration Buzzer
10	P2_7	Button 2 (VOL+)	Button 2 (VOL+)
11	P3_0	Aux-in detect	Aux-in detect
12	P3_1	—	Button 5
13	P3_3	—	Button 4 (FWD)
14	P3_6	—	Twin Role setting 2
15	P3_7	—	UART_TX_IND LED3

6.5 I²S Mode Application

The IS2064GM and IS2064S/B SoC provide an I²S digital audio output interface to connect with the external codec or DSP. It provides 8, 16, 44.1, 48, 88.2 and 96 kHz sampling rates for 16-bit and 24-bit data formats. The I²S setting are configured by using the UI and DSP tools.

Note: The UI and DSP tools are available for download from the Microchip website at http://www.microchip.com/wwwproducts/en/IS2062 and http://www.microchip.com/wwwproducts/en/IS2064.

The external codec or DSP interfaces with IS2062/64 over these pins: SCLK0, RFS0, DR0, and DT0. The following figures illustrate the I²S signal connection between the IS2064GM and IS2064S/B SoC and an external DSP. Use the DSP tool to configure the IS2064GM and IS2064S/B SoC as Master/Slave. For additional information on timing specifications, refer to Timing Specifications.

Figure 6-9. I²S MASTER MODE

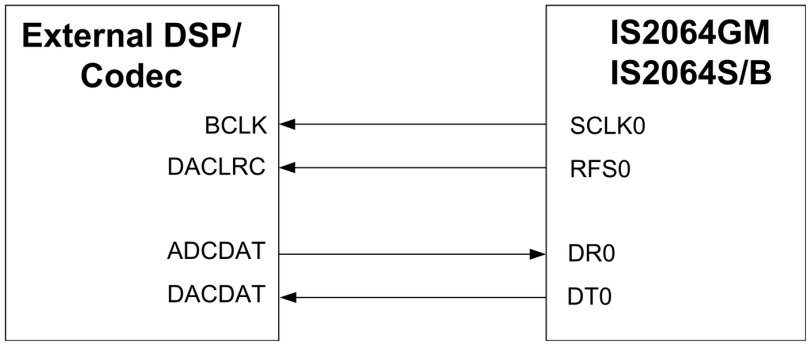
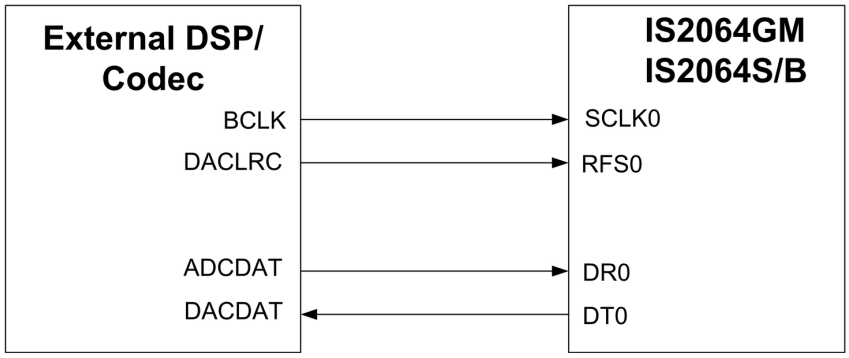


Figure 6-10. I²S SLAVE MODE

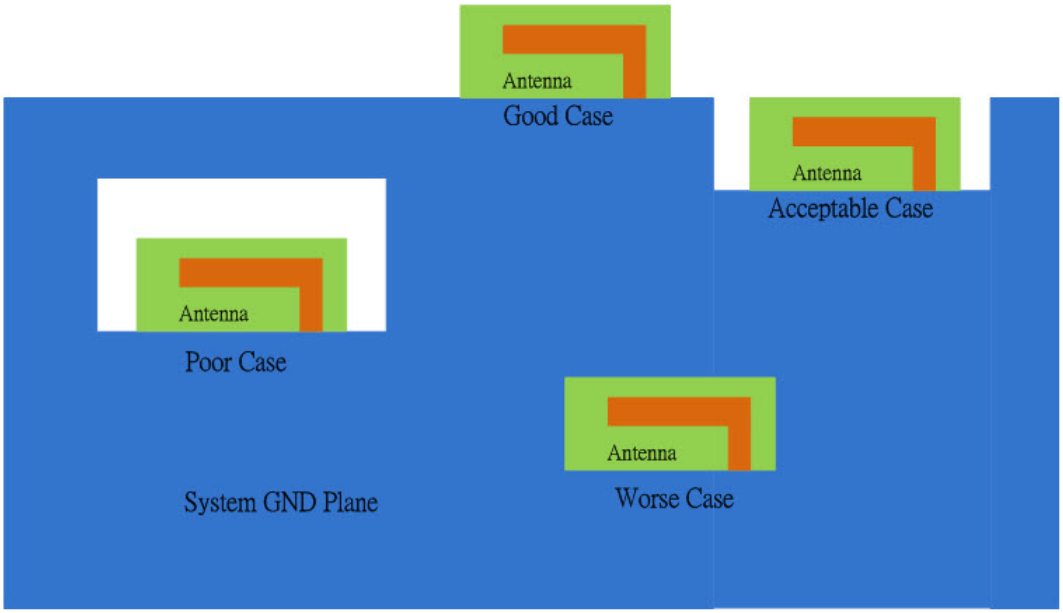


7. Antenna Placement Rule

For Bluetooth enabled products, the antenna placement affects the overall performance. The antenna requires free space to radiate RF signals and it must not be surrounded by the GND plane.

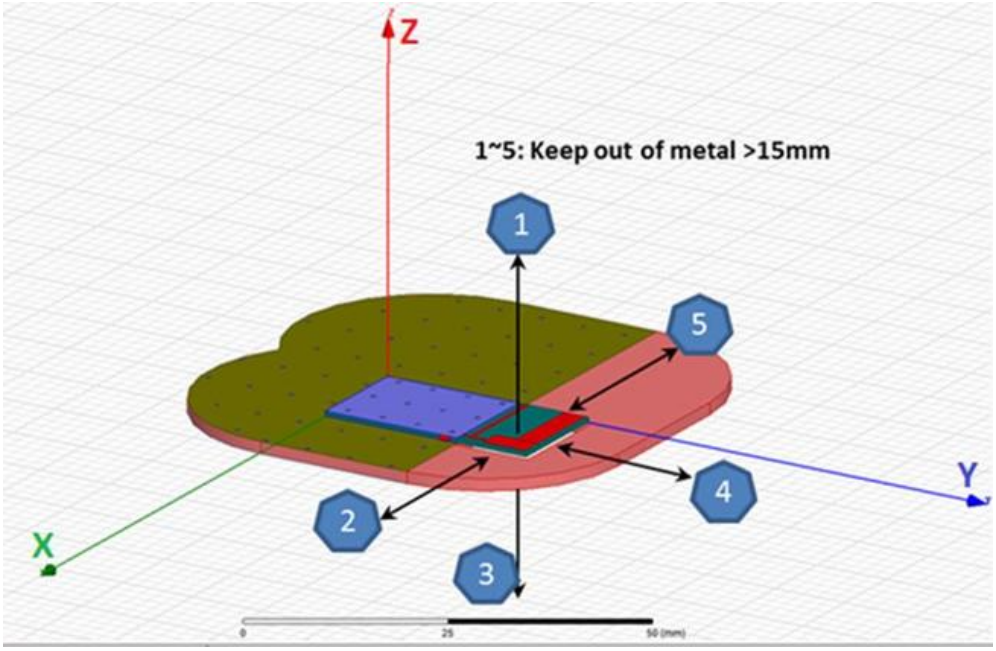
The following figure illustrates a typical example of the good and poor antenna placement on the main application board with the GND plane.

Figure 7-1. ANTENNA PLACEMENT EXAMPLES



The following figure illustrates the keep out area recommended for the PCB antenna.

Figure 7-2. KEEP OUT AREA RECOMMENDED FOR PCB ANTENNA



Note: For additional information on the antenna placement, refer to the antenna specific data sheet from the antenna manufacturer.

8. Electrical Characteristics

This section provides an overview of the IS2062/64 SoC electrical characteristics. Additional information will be provided in future revisions of this document, once it is available.

Table 8-1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Ambient temperature under bias	—	-20	+70	℃
Storage temperature	—	-65	+150	℃
Digital core supply voltage	VDD_CORE	0	1.35	V
RF supply voltage	VCC_RF	0	1.35	V
SAR ADC supply voltage	SAR_VDD	0	2.1	V
Codec supply voltage	VDDA/VDDAO	0	3.3	V
I/O supply voltage	VDD_IO	0	3.6	V
Buck supply voltage	BK_VDD	0	4.3	V
Supply voltage	LDO31_VIN	0	4.3	V
Battery input voltage	BAT_IN	0	4.3	V
Adapter input voltage	ADAP_IN	0	7.0	V

Note: Stresses listed on the preceding table cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification are not implied. Exposure to maximum rating conditions for extended periods affects device reliability.

The following tables provide the recommended operating conditions and the electrical specifications of the IS2062/64 SoC.

Table 8-2. RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital core supply voltage	VDD_CORE	1.14	1.2	1.26	V
RF supply voltage	VCC_RF	1.22	1.28	1.34	V
SAR ADC supply voltage	SAR_VDD	1.62	1.8	1.98	V
Codec supply voltage	VDDA/ VDDAO	1.8	2.8	3.0	V
I/O supply voltage	VDD_IO	3.0	3.3	—	V
Buck supply voltage	BK_VDD	3	3.8	4.25	V
Supply voltage	LDO31_VIN	3	3.8	4.25	V
Input voltage for battery	BAT_IN	3.2	3.8	4.25	V
Input voltage for adapter	ADAP_IN	4.5	5	5.5	V

.....continued					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Operation temperature	$T_{OPERATION}$	-20	+25	+70	℃

Note: The PMU output powers, BK_O, CODEC_VO, RFLDO_O, and CLDO_O are programmed through the EEPROM parameters.

Table 8-3. BUCK REGULATOR

Parameter	Min.	Typ.	Max.	Unit
Input Voltage	3.0	3.8	4.25	V
Output Voltage (I_{load} = 70 mA and V_{in} = 4V)	1.7	1.8	2.05	V
Output Voltage Accuracy	—	±5	—	%
Output Voltage Adjustable Step	—	50	—	mV/Step
Output Adjustment Range	-0.1	—	+0.25	V
Average Load Current (I_{LOAD})	120	—	—	mA
Conversion Efficiency (BAT = 3.8V and I_{load} = 50 mA)	—	88(1)	—	%
Quiescent Current (PFM)	—	—	40	µA
Output Current (peak)	200	—	—	mA
Shutdown Current	—	—	<1	µA

Note:

1. Test condition: Temperature +25℃ and wired inductor 10 µH.
2. These parameters are characterized, but not tested on the manufactured device.

Table 8-4. LOW DROP REGULATOR

Parameter		Min.	Typ.	Max.	Unit
Input Voltage		3.0	3.8	4.25	V
Output Voltage	CODEC_VO	—	2.8	—	V
	LDO31_VO	—	3.3	—	
Output Accuracy (V_{IN} = 3.7V, I_{LOAD} = 100 mA and +27°C)		—	±5	—	%
Output current (average)		—	—	100	mA
Drop-out voltage (I_{load} = maximum output current)		—	—	300	mV
Quiescent Current (excluding load and I_{load} < 1 mA)		—	45	—	µA
Shutdown Current		—	—	<1	µA

Note:

1. Test condition: Temperature +25℃.
2. These parameters are characterized, but not tested on manufactured device.

Table 8-5. BATTERY CHARGER

Parameter		Min.	Typ.	Max.	Unit
Input Voltage (ADAP_IN)		4.5	5.0	5.5	V
Supply current to charger only		—	3	4.5	mA
Maximum Battery Fast Charge Current	Headroom > 0.7V (ADAP_IN = 5V)	—	350	—	mA
	Headroom = 0.3V to 0.7V (ADAP_IN = 4.5V) (**Note 2**)	—	175	—	mA
Trickle Charge Voltage Threshold		—	3	—	V
Battery Charge Termination Current (% of Fast Charge Current)		—	10	—	%

Note:

1. Headroom = V_{ADAP_IN} - V_{BAT}.
2. When V_{ADAP_IN} - V_{BAT} > 2V, the maximum fast charge current is 175 mA for thermal protection.
3. These parameters are characterized, but not tested on manufactured device.

Table 8-6. LED DRIVER

Parameter	Min.	Typ.	Max.	Unit
Open-drain Voltage	—	—	3.6	V
Programmable Current Range	0	—	5.25	mA
Intensity Control	—	16	—	step
Current Step	—	0.35	—	mA
Power-Down Open-drain Current	—	—	1	µA
Shutdown Current	—	—	1	µA

Note:

1. Test condition: BK_O = 1.8V with temperature +25°C.
2. These parameters are characterized, but not tested on manufactured device.

Table 8-7. AUDIO CODEC DIGITAL TO ANALOG CONVERTER

Parameter (Condition)	Min.	Typ.	Max.	Unit
Output Sampling Rate	—	128	—	f_s
Resolution	16	—	20	Bit
Output Sample Rate	8	—	48	kHz
Signal-to-Noise Ratio (**Note 2**) (SNR @Capless mode) for 48 kHz	—	96	—	dB

.....continued

Parameter (Condition)		Min.	Typ.	Max.	Unit
Signal-to-Noise Ratio (**Note 2**) (SNR @single-ended mode) for 48 kHz		—	98	—	dB
Digital Gain		-54	—	4.85	dB
Digital Gain Resolution		—	2 to 6	—	dB
Analog Gain		-28	—	3	dB
Analog Gain Resolution		—	1	—	dB
Output Voltage Full-scale Swing (AVDD = 2.8V)		495	742.5	—	mV/rms
Maximum Output Power (16 Ohm load)		—	34.5	—	mW
Maximum Output Power (32 Ohm load)		—	17.2	—	mW
Allowed Load	Resistive	—	16	O.C.	Ohm
	Capacitive	—	—	500	pF
THD+N (16 Ohm load) (**Note 3**)		—	0.05	—	%
Signal-to-Noise Ratio (SNR @ 16 Ohm load) (**Note 4**)	—	—	98	—	dB

Note:

1. T = +25°C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz to 20 kHz.
2. f_{in} = 1 kHz, B/W = 20 HZ to 20 kHz, A-weighted, THD+N < 0.01%, 0 dBFS signal, Load = 100 kOhm.
3. f_{in} = 1 kHz, B/W = 20 HZ to 20 kHz, A-weighted, -1 dBFS signal, Load = 16 Ohm.
4. f_{in} = 1 kHz, B/W = 20 HZ to 20 kHz, A-weighted, THD+N < 0.05%, 0 dBFS signal, Load = 16 Ohm.
5. These parameters are characterized, but not tested on manufactured device.

Table 8-8. AUDIO CODEC ANALOG TO DIGITAL CONVERTER

Parameter (Condition)	Min.	Typ.	Max.	Unit
Resolution	—	—	16	Bit
Output Sample Rate	8	—	48	kHz
Signal-to-Noise Ratio (**Note 2**) (SNR @MIC or Line-in mode)	—	92	—	dB
Digital Gain	-54	—	4.85	dB
Digital Gain Resolution	—	2 to 6	—	dB
MIC Boost Gain	—	20	—	dB
Analog Gain	—	—	60	dB
Analog Gain Resolution	—	2.0	—	dB
Input full scale at maximum gain (differential)	—	4	—	mV/rms
Input full scale at minimum gain (differential)	—	800	—	mV/rms

.....continued				
Parameter (Condition)	**Min.**	**Typ.**	**Max.**	**Unit**
3 dB bandwidth	—	20	—	kHz
Microphone mode (input impedance)	—	24	—	kOhm
THD+N (microphone input) at 30 mVrms input	—	0.02	—	%

Note:

1. T = +25°C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz to 20 kHz
2. f_{in} = 1 kHz, B/W = 20 Hz to 20 kHz, A-weighted, THD+N < 1%, 150 mVpp input.
3. These parameters are characterized, but not tested on manufactured device.

Table 8-9. TRANSMITTER SECTION FOR BDR AND EDR

Parameter	Min.	Typ.	Max.	Bluetooth specification	Unit
Transmit power	—	2(3)	4	-6 to 4	dBm
EDR/BDR relative transmit power	-4	-1.8	1	-4 to 1	dB

Note:

1. The RF Transmit power is modulation value.
2. The RF Transmit power is calibrated during production using the MP tool software and MT8852 Bluetooth test equipment.
3. Test condition: VCC_RF = 1.28V, temperature +25℃.

Table 8-10. RECEIVER SECTION FOR BDR AND EDR

Parameter	Packet Type	Min.	Typ.	Max.	Bluetooth specification	Unit
Sensitivity at 0.1% BER	GFSK	—	-89	—	≤-70	dBm
Sensitivity at 0.01% BER	π/4 DQPSK	—	-93	—	≤-70	dBm
	8 DPSK	—	-86	—	≤-70	dBm

Note:

1. Test condition: VCC_RF = 1.28V, temperature +25ºC.
2. These parameters are characterized, but not tested on manufactured device.

Table 8-11. IS2062GM SYSTEM CURRENT CONSUMPTION

System Status	Typ.	Max.	Unit
System Off mode	—	10	µA
Stop Advertising (Samsung S5 (SM-G900I)/Android™ 4.4.2)			
Standby mode	0.57	—	mA
Link mode	0.5	—	mA
ESCO Link	15.1	—	mA
A2DP Link	14.3	—	mA

.....continued			
System Status	**Typ.**	**Max.**	**Unit**
Stop Advertising (iPhone®6 / iOS 8.4)			
Standby mode	0.6	—	mA
Link mode	0.6	—	mA
SCO Link	15.3	—	mA
A2DP Link	15.4	—	mA

Note:

1. Standby mode: Power-on without Bluetooth link; Link mode: With Bluetooth link in Low-Power mode.
2. Current consumption values are considered with the BM62 EVB as a test platform, BAT_IN = 3.8V. The distance between smart phone and EVB is 30 cm and the speaker is without loading.

Table 8-12. IS2064GM-0L3 SYSTEM CURRENT CONSUMPTION

Modes	Condition	Role	Package Type	Class 1	Class 2	Unit
SCO/eSCO connection (mute at both far end and near end)	CVSD	Master	disable 3M	22.1	17.1	mA
			enable 3M	22.2	18.0	mA
		Slave	disable 3M	22.3	17.5	mA
			enable 3M	21.2	17.3	mA
	mSBC	Master	disable 3M	22.9	18.7	mA
			enable 3M	22.9	18.7	mA
		Slave	disable 3M	22.3	18.9	mA
			enable 3M	22.8	18.9	mA

.....continued

Modes	Condition	Role	Package Type	Class 1	Class 2	Unit
A2DP connection (1 kHz tone, mute)	SBC, 44.1 kHz, I2S output	Master	disable 3M	20.2	16.8	mA
			enable 3M	19.4	17.7	mA
		Slave	disable 3M	17.3	16.1	mA
			enable 3M	18.1	16.7	mA
	LDAC, 96.0 kHz, I2S output 330 KBPS	Master	disable 3M	29.5	24.5	mA
			enable 3M	29.5	22.8	mA
		Slave	disable 3M	28.1	21.4	mA
			enable 3M	28	21.7	mA
	LDAC, 96.0 kHz, I2S output 660 KBPS	Master	disable 3M	26.1	25.4	mA
			enable 3M	26.4	23	mA
		Slave	disable 3M	24.3	21.3	mA
			enable 3M	24.8	22.4	mA
	LDAC, 96.0 kHz, I2S output 990 KBPS	Master	disable 3M	28.2	25.5	mA
			enable 3M	28.1	24.98	mA
		Slave	disable 3M	25.36	22.67	mA
			enable 3M	26.15	22.9	mA
Sniff mode (linked to mobile)	sniff interval = 500 ms, 1 attempt	Master	-	900	690	uA
	sniff interval = 1280 ms, 1 attempt	Master	-	730	670	uA
Page Scan (not discoverable, yet ready to be connected)	Page Scan interval= 1.28s	-	-	810	730	uA
System off	-	-	-	70	16.1	uA

1. The measurements are taken on the BM64L EVB.
2. The distance between the DUT and the smartphone is 30cm. The values mentioned in the preceding table was measured using an Android phone with version 8.0.0.
3. BAT_IN is 3.7V.
4. The current consumption values reflect the average current consumption.

Table 8-13. IS2064S/B SYSTEM CURRENT CONSUMPTION

Modes	Condition	Role	Packet Type	IS2064B	IS2064S	Unit
Default UI (1 kHz tone, without LEDs)	Standalone BT mode, with default UI table	Master	-	10.3	10.1	mA
SCO/eSCO connection (mute at both far end and near end)	Mono audio codec output	Master	HV3	10.6	11	mA
			2EV3	9.3	10.7	mA
			3EV3	NS	NS	mA
		Slave	HV3	12.8	14.7	mA
			2EV3	13.6	14.7	mA
			3EV3	NS	NS	mA
A2DP connection (1 kHz tone, mute, no load)	Internal Codec, Android Slave	Master	DH5	11.4	11.1	mA
			2DH5	10.7	10.1	mA
	Internal Codec, iOS Master	Slave	DH5	10.3	9.7	mA
			2DH5	10.3	9.7	mA
			3DH5	10.3	9.7	mA
Sniff mode (linked to smartphone, BLE off)	Connection established, but no activity (system idle)	Master	-	423	427	µA
		Slave	-	423	427	µA
Inquiry Scan (discoverable by smartphone)	With LEDs	-	-	3.8	3.8	mA
	Without LEDs	-	-	1.1	1.2	mA
System-off	3.8V at BAT_IN	-	-	18	20	µA

Note:

1. NS = Not Supported.
2. The measurements are taken on the IS2064S-114 and IS2064B-114 Validation Platform.
3. The distance between the DUT and the smartphone is 20 cm.
4. iOS version 10.3.2 and Android version 5.1.1.
5. BAT_IN = 3.8V.
6. The current consumption values reflect the average current consumption.

8.1 Timing Specifications

The following figures illustrate the timing diagram of the IS2062/64 SoC in I^2S and PCM modes.

Figure 8-1. TIMING DIAGRAM FOR I²S MODES (MASTER/SLAVE)

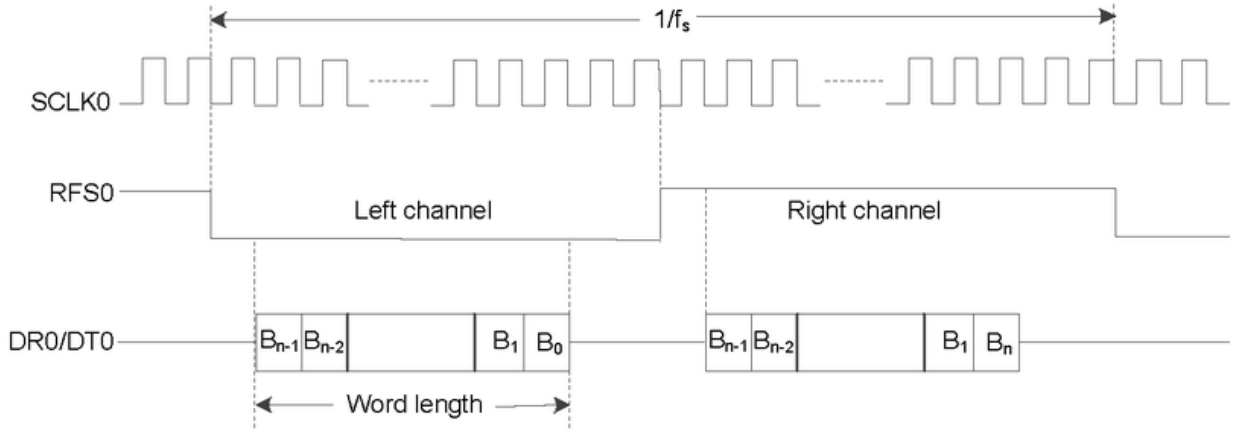
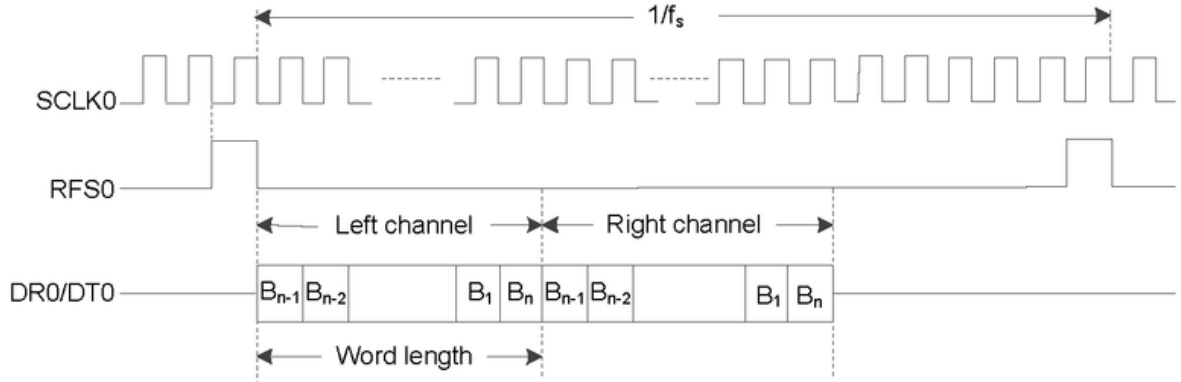


Figure 8-2. TIMING DIAGRAM FOR PCM MODES (MASTER/SLAVE)

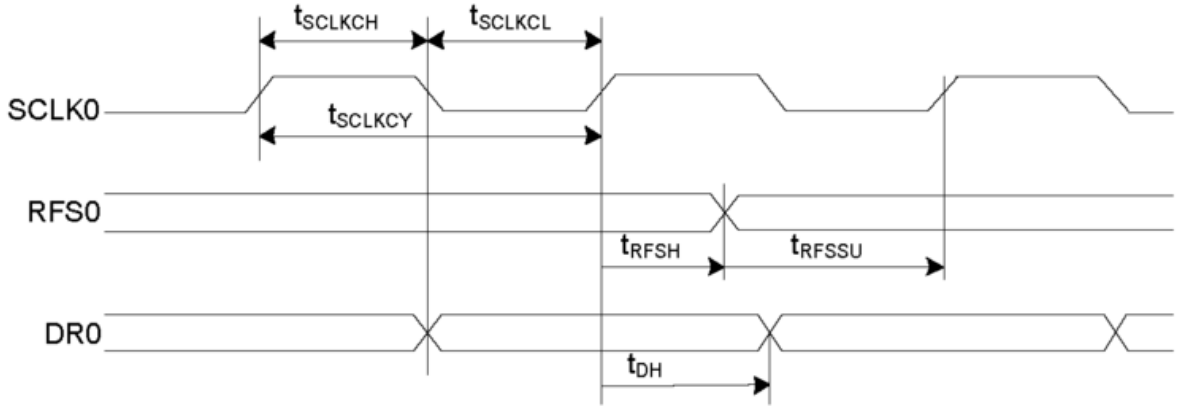


Note:

1. f_s: 8, 16, 32, 44.1, 48, 88.2 and 96 kHz.
2. SCLK0: 64 x f_s / 256 x f_s.
3. Word length: 16-bit and 24-bit.

The following figure illustrates the audio interface timing diagram.

Figure 8-3. AUDIO INTERFACE TIMING



The following table provides the timing specifications of the audio interface.

Table 8-14. AUDIO INTERFACE TIMING SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK0 duty ratio	d_{SCLK}	—	50	—	%
SCLK0 cycle time	t_{SCLKCY}	50	—	—	ns
SCLK0 pulse width high	t_{SCLKCH}	20	—	—	ns
SCLK0 pulse width low	t_{SCLKCL}	20	—	—	ns
RFS0 setup time to SCLK0 rising edge	t_{RFSSU}	10	—	—	ns
RFS0 hold time from SCLK0 rising edge	t_{RFSH}	10	—	—	ns
DR0 hold time from SCLK0 rising edge	t_{DH}	10	—	—	ns

Note: Test Conditions: Slave mode, f_s = 48 kHz, 24-bit data and SCLK0 period = 256 f_s

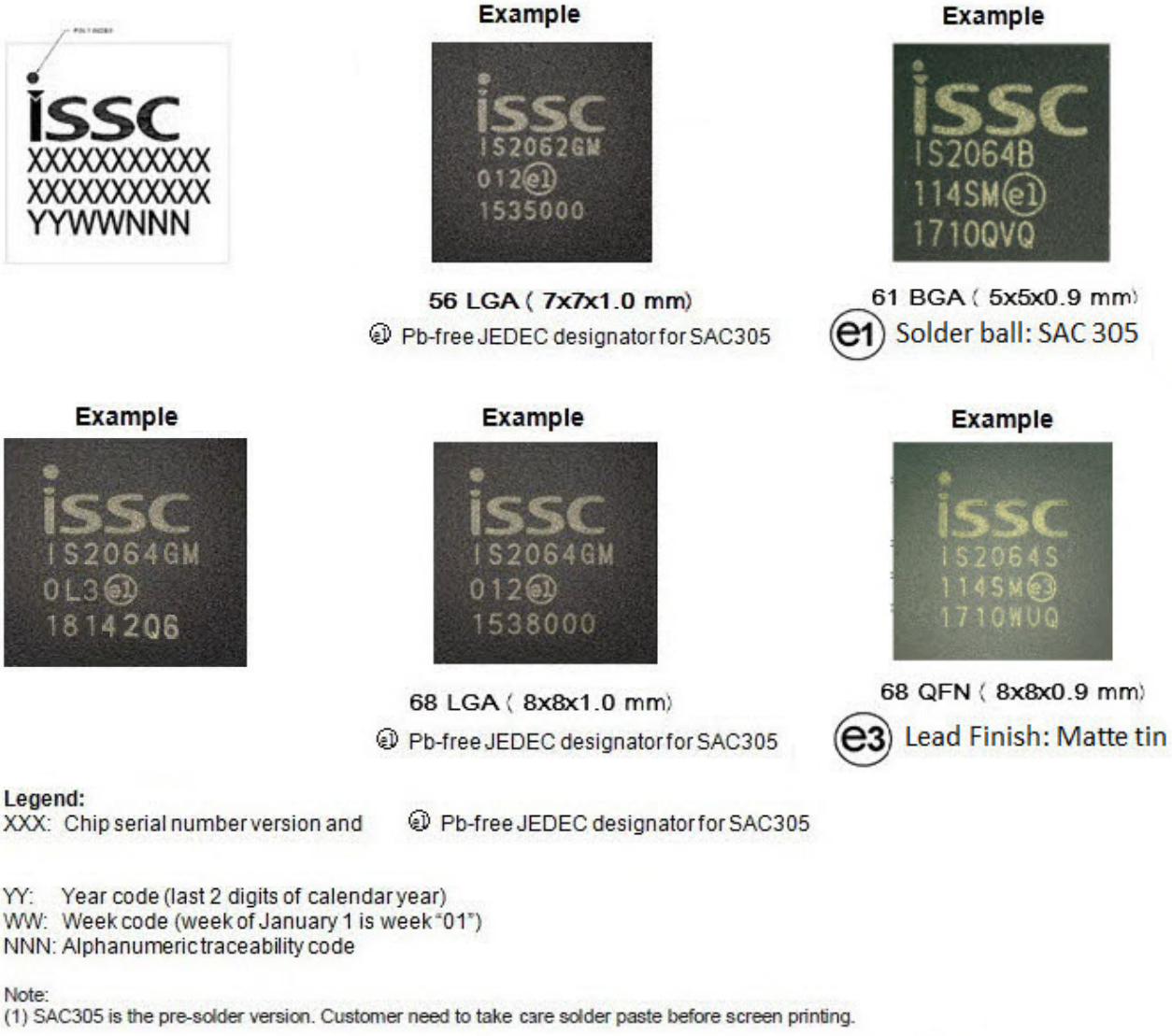
9. Packaging Information

This section provides information on package marking, package details and footprint dimensions of the IS2062/64 SoC.

9.1 Package Marking Information

The following figures illustrate the package marking information of the IS2062GM, IS2064GM, IS2064S and IS2064B.

Figure 9-1. PACKAGE MARKING INFORMATION



Legend:
XXX: Chip serial number version and e1 Pb-free JEDEC designator for SAC305

YY: Year code (last 2 digits of calendar year)
WW: Week code (week of January 1 is week "01")
NNN: Alphanumeric traceability code

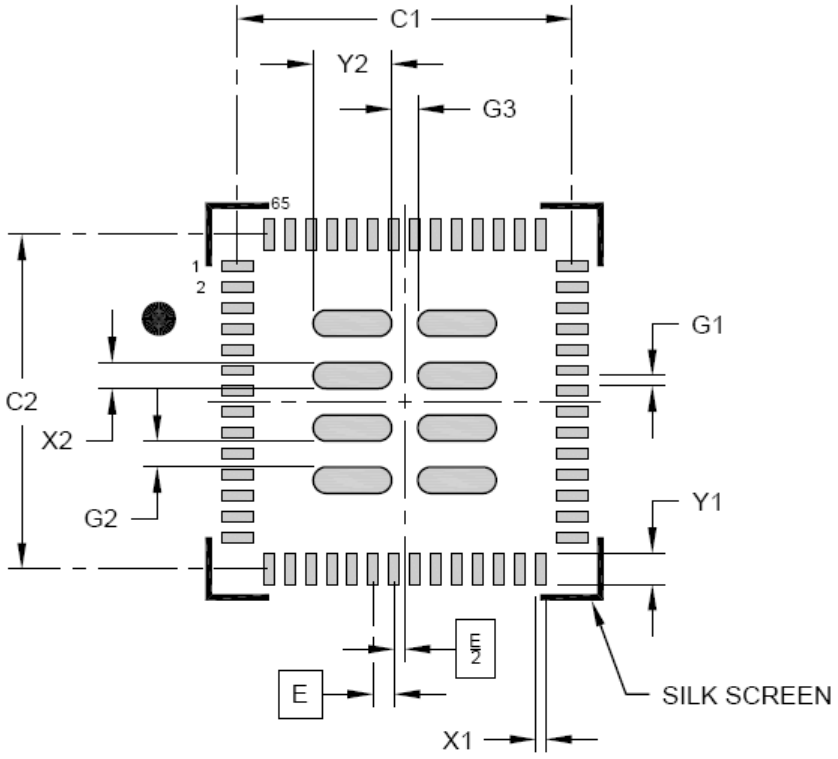
Note:
(1) SAC305 is the pre-solder version. Customer need to take care solder paste before screen printing.

9.2 Package Details

9.2.1 56-Lead Land Grid Array (VZ) - 7x7x1 mm Body (LGA)

The following figure illustrates the footprint dimensions of the IS2062GM SoC.

Figure 9-2. IS2062GM FOOTPRINT DIMENSIONS



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width (X8)	X2			0.50
Center Pad Length (X8)	Y2			1.50
Contact Pad Spacing	C1		6.40	
Contact Pad Spacing	C2		6.40	
Contact Pad Width (X56)	X1			0.20
Contact Pad Length (X56)	Y1			0.60
Contact Pad to Pad (X52)	G1	0.20		
Center Pads Clearance (X6)	G2		0.50	
Center Pads Clearance X4)	G3		0.50	

Note:

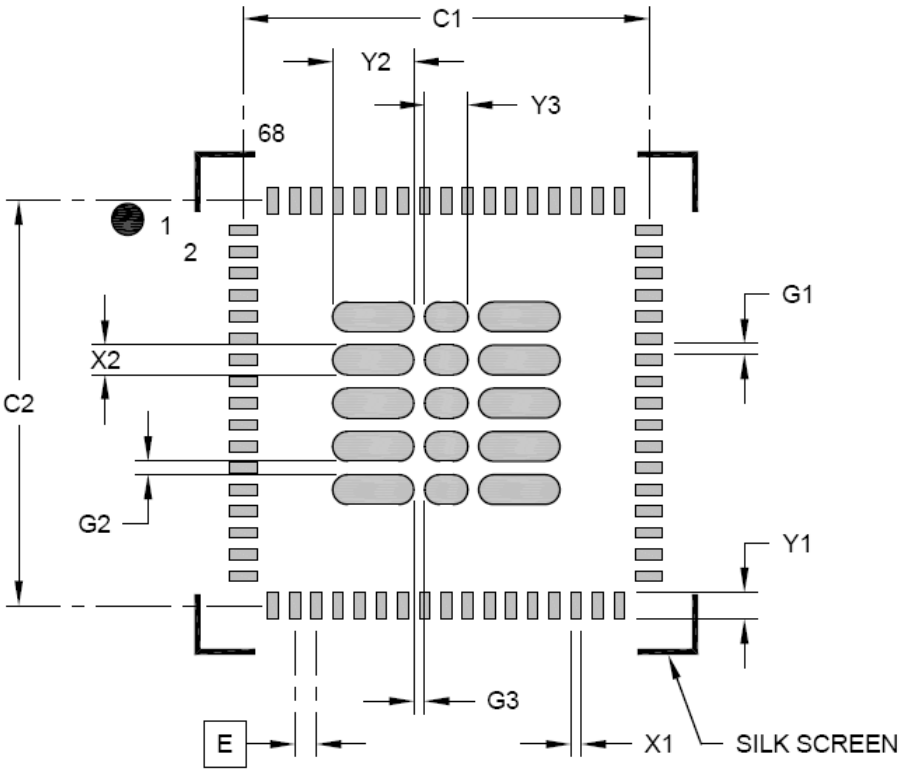
1. Dimensioning and tolerance per ASME Y14.5M
   – BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias if used, must be filled or tended to avoid solder loss during reflow process.

3. For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

9.2.2 68-Lead Land Grid Array (VZ) - 8x8x1 mm Body (LGA)

The following figure illustrates the footprint dimensions of the IS2064GM SoC.

Figure 9-3. IS2064GM FOOTPRINT DIMENSIONS



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Center Pad Width (X10)	X2			0.55
Center Pad Length (X10)	Y2			1.50
Center Pad Length (X5)	Y3			0.80
Contact Pad Spacing	C1		7.50	
Contact Pad Spacing	C2		7.50	
Contact Pad Width (X68)	X1			0.20
Contact Pad Length (X68)	Y1			0.50
Contact Pad to Pad (X68)	G1	0.20		
Center Pads Clearance (X12)	G2	0.20		
Center Pads Clearance (X10)	G3	0.20		

Note:

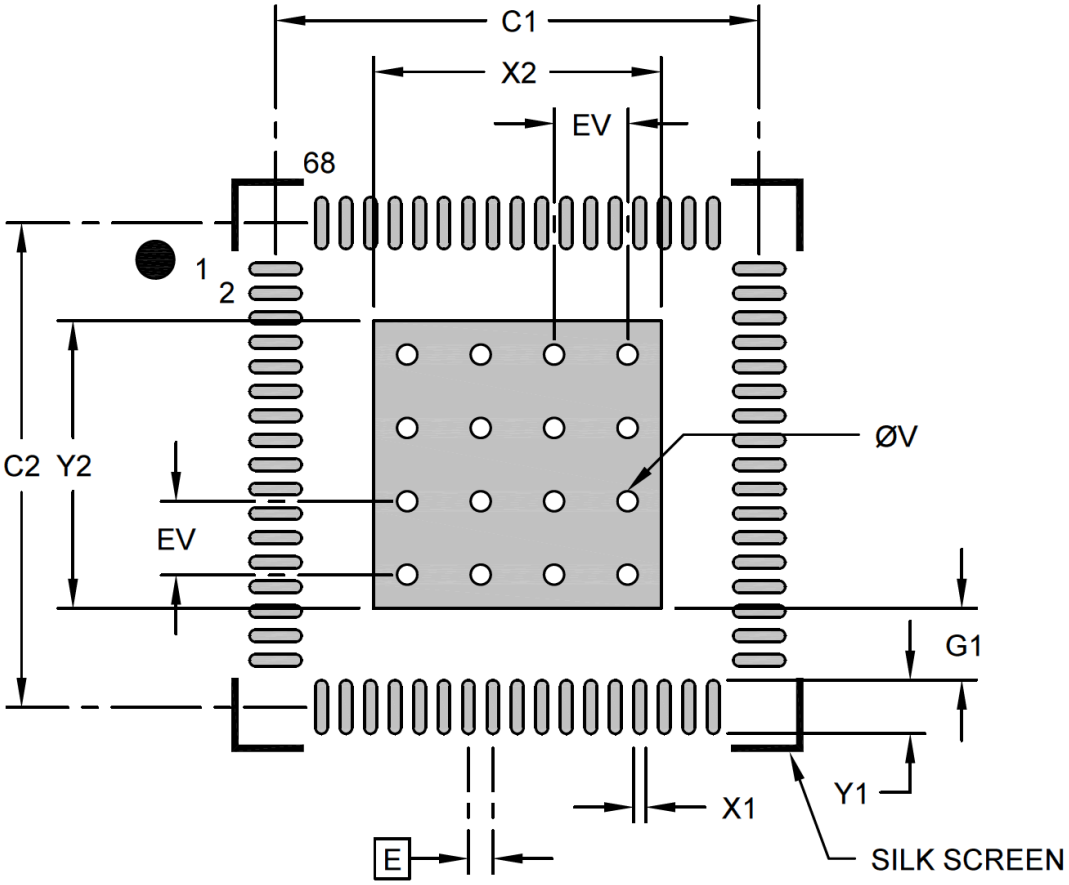
1. Dimensioning and tolerance per ASME Y14.5M
   – BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias if used, must be filled or tended to avoid solder loss during reflow process.

3. For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

9.2.3 68-Lead Very Thin Plastic Quad Flat, No Lead Package (VZ) - 8x8x0.9 mm Body (VQFN)

The following figure illustrates the footprint dimensions of the IS2064S SoC.

Figure 9-4. IS2064S FOOTPRINT DIMENSIONS



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			4.70
Optional Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (X68)	X1			0.20
Contact Pad Length (X68)	Y1			0.85
Contact Pad to Center Pad (X68)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

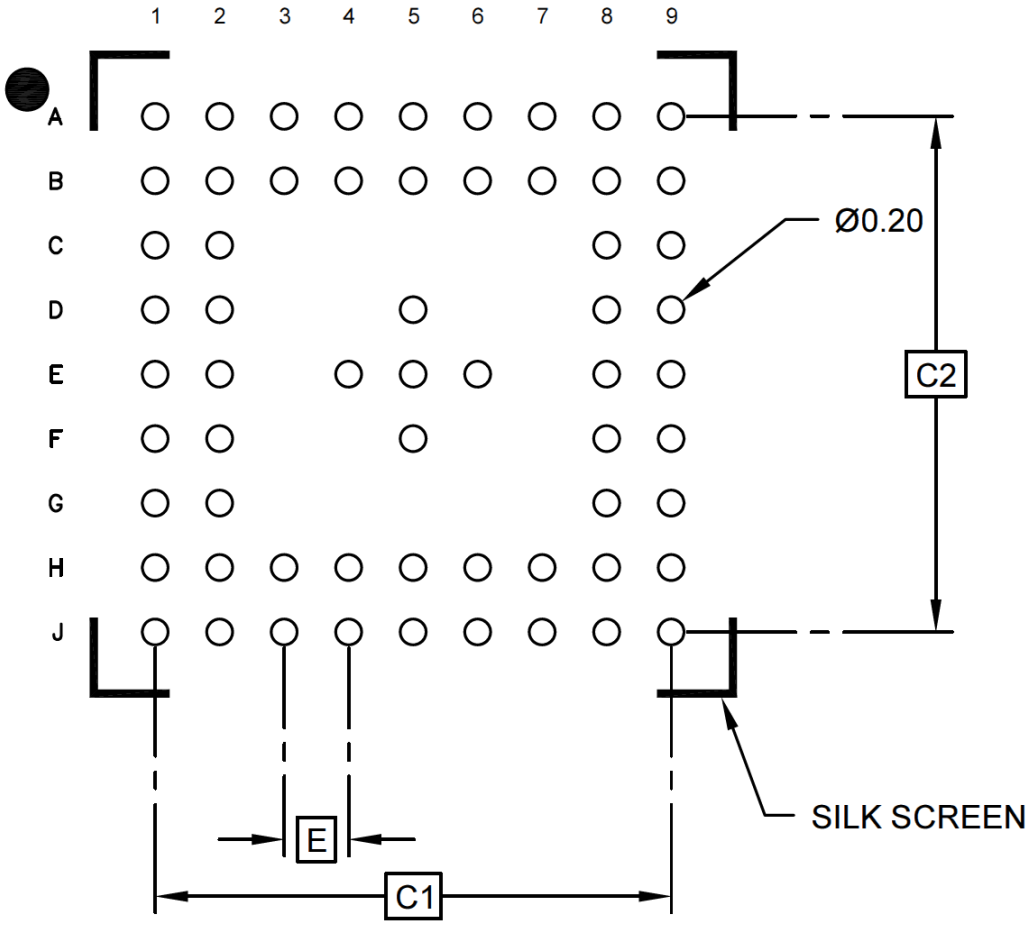
Note:

1. Dimensioning and tolerance per ASME Y14.5M
   – BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias if used, must be filled or tended to avoid solder loss during reflow process.
3. For the most current package drawings, see the Microchip Packaging Specifications located at http://www.microchip.com/packaging.

9.2.4 61-Ball Very Thin Fine Pitch Ball Grid Array (5HX) - 5x5x0.9 mm Body (VFBGA)

The following figure illustrates the footprint dimensions of the IS2064B SoC.

Figure 9-5. IS2064B FOOTPRINT DIMENSIONS



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Diameter (X61)	X1			0.20

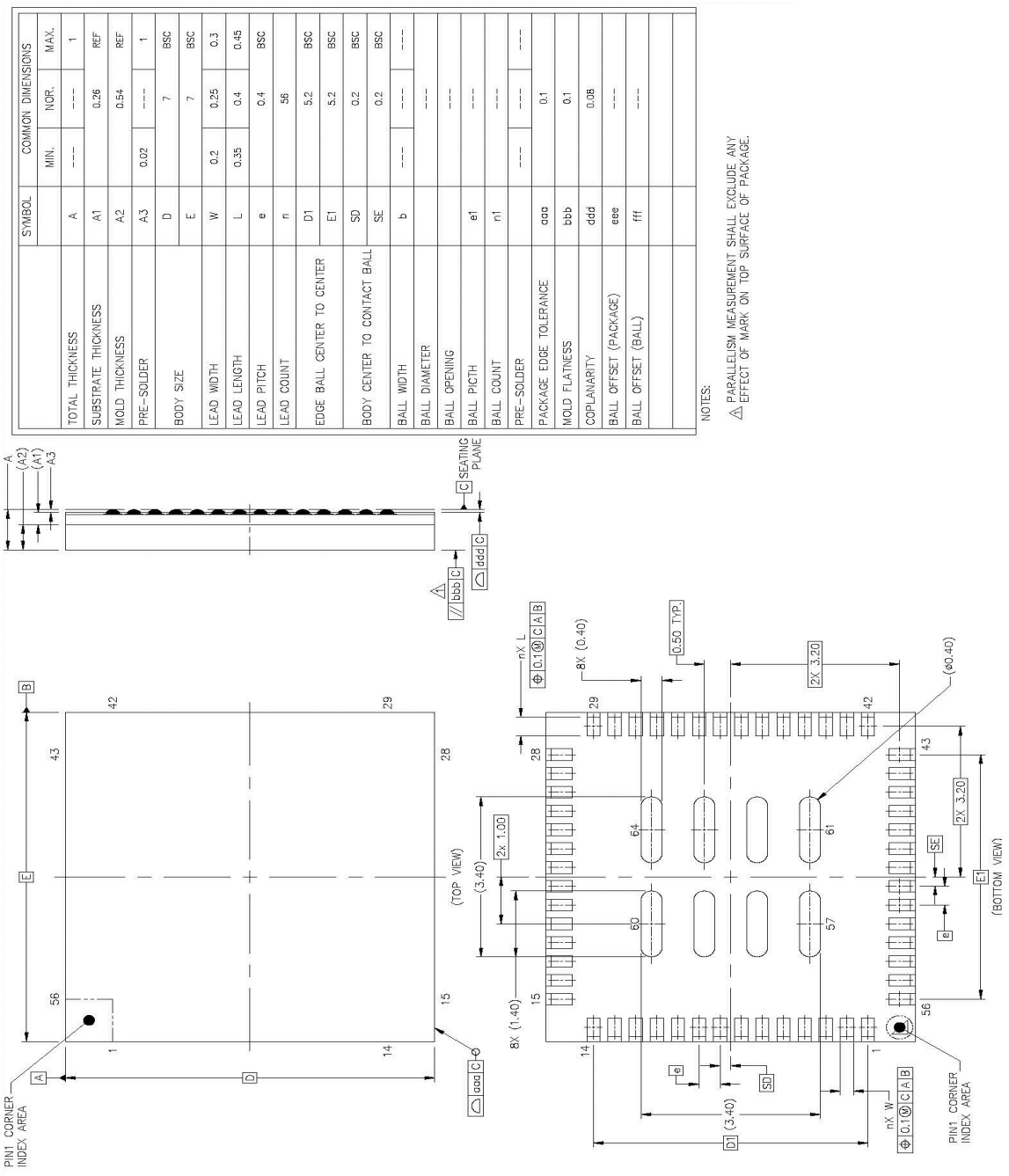
Note:

1. Dimensioning and tolerance per ASME Y14.5M
   – BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

9.2.5 IS2062GM-SAC305

The following figure illustrates the package details of the IS2062GM-SAC305.

Figure 9-6. IS2062GM-SAC305 PACKAGE DETAILS

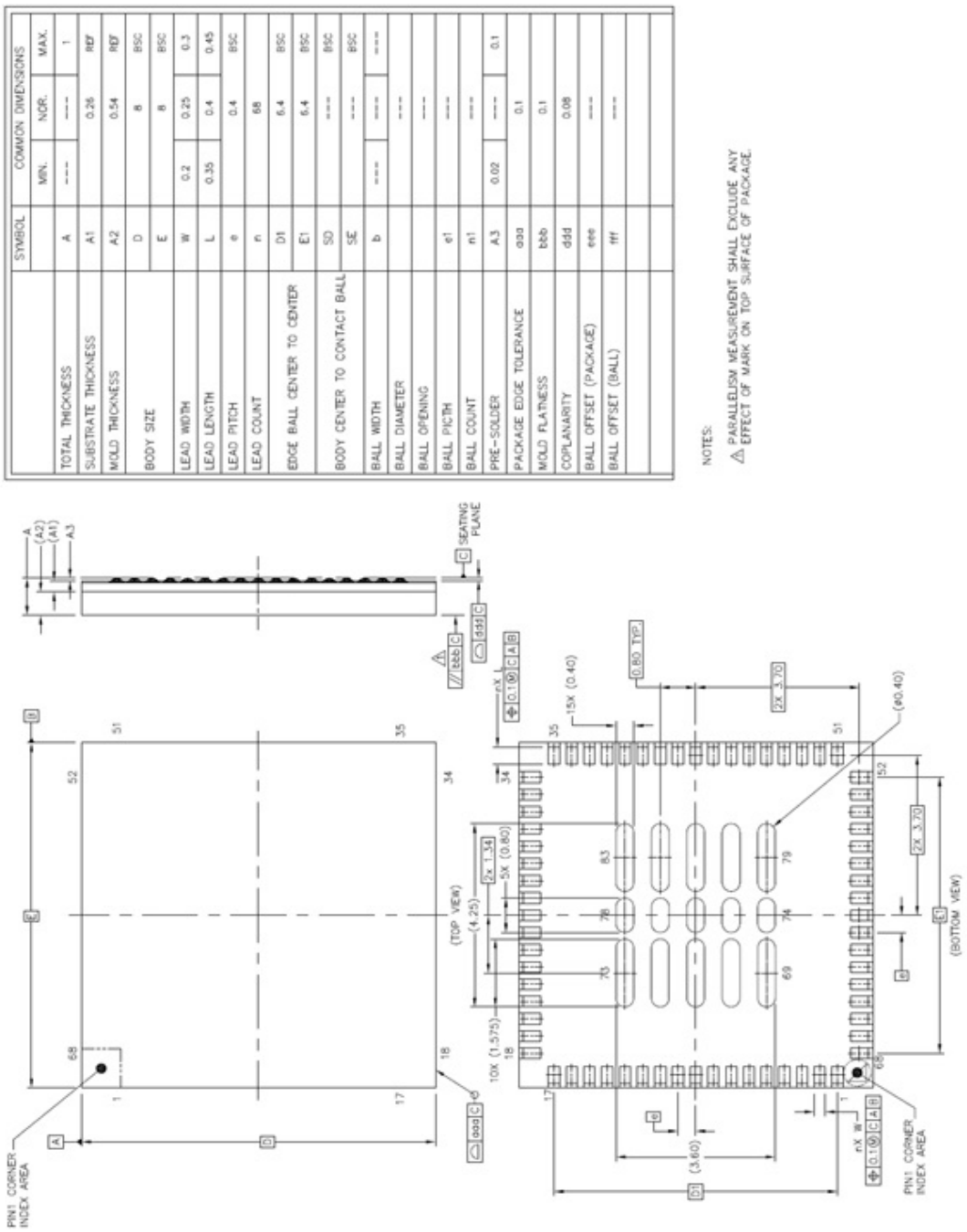


Note: For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

9.2.6 IS2064GM-SAC305

The following figure illustrates the package details of the IS2064GM-SAC305.

Figure 9-7. IS2064GM-SAC305 PACKAGE DETAILS



Note: For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

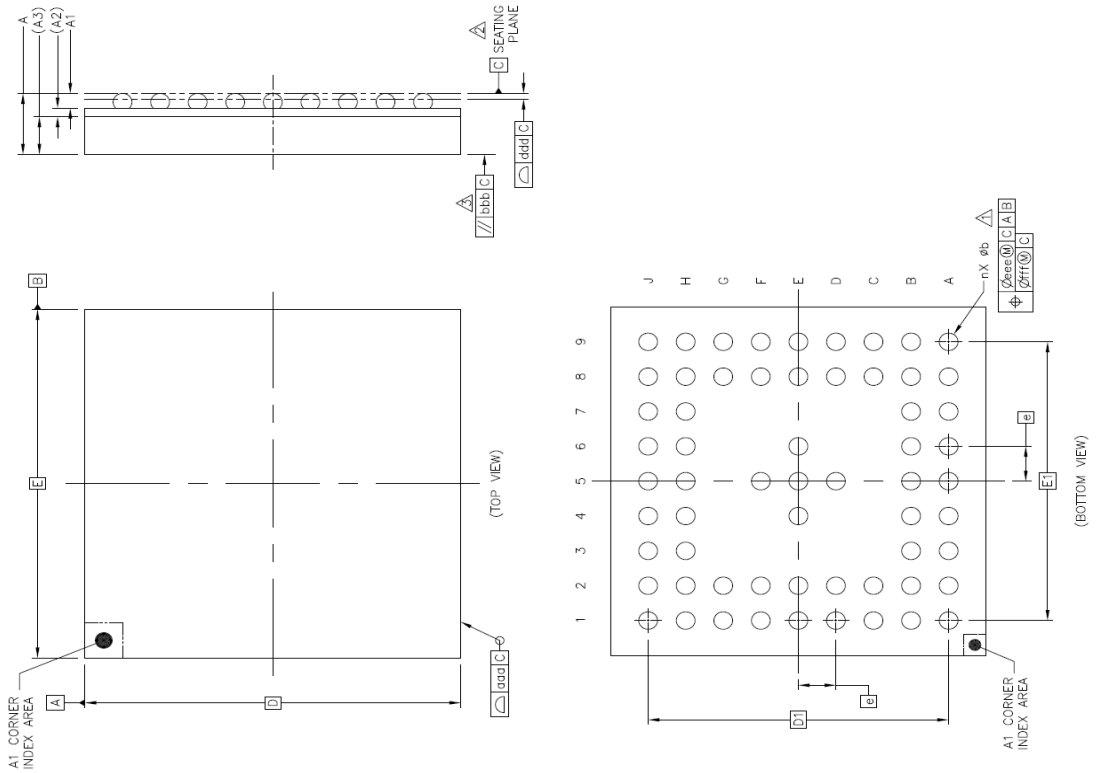
9.2.7 IS2064S-QFN

The following figure illustrates the package details of the IS2064S-QFN.

Figure 9-8. IS2064S-QFN PACKAGE DETAILS

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.9
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.125	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		5	BSC
	E		5	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.5	BSC
BALL COUNT	n		61	
EDGE BALL CENTER TO CENTER	D1		4	BSC
	E1		4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:
1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.



Note: For the most current package drawings, see the Microchip Packaging Specifications located at http://www.microchip.com/packaging.

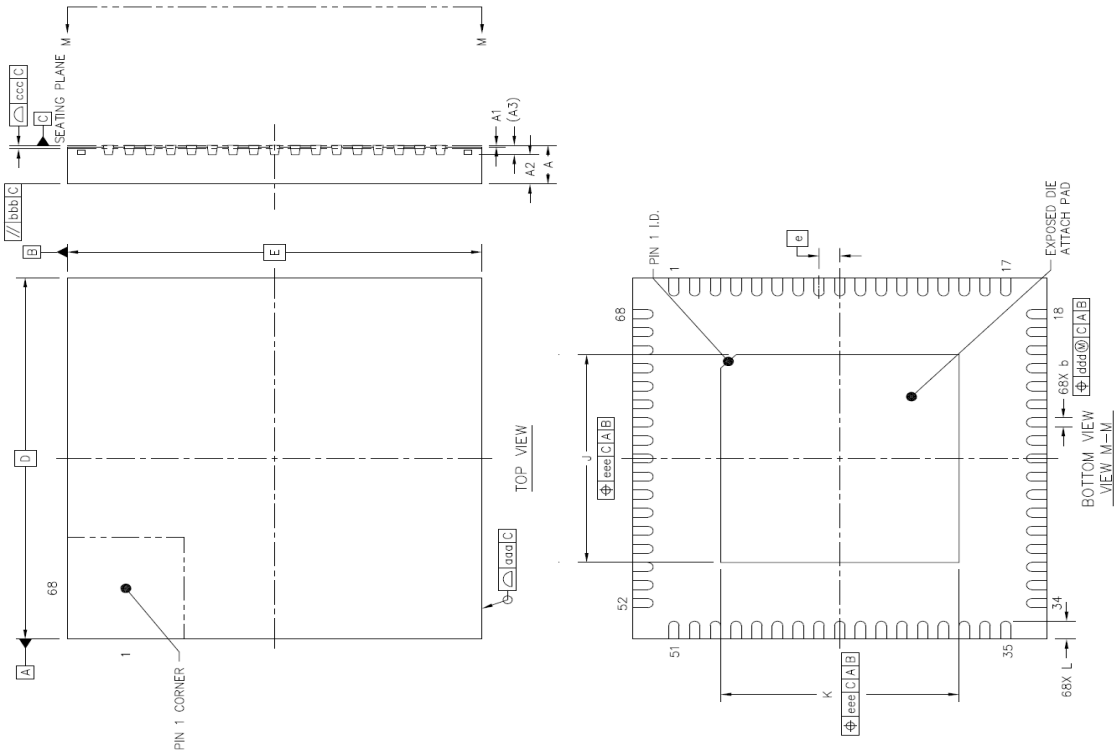
9.2.8 IS2064B-BGA

The following figure illustrates the package details of the IS2064B-BGA.

Figure 9-9. IS2064B-BGA PACKAGE DETAILS

	SYMBOL		MIN	NOM	MAX
TOTAL THICKNESS	A		0.8	0.85	0.9
STAND OFF	A1		0	0.035	0.05
MOLD THICKNESS	A2		---	0.65	0.67
L/F THICKNESS	A3			0.203 REF	
LEAD WIDTH	b		0.15	0.2	0.25
BODY SIZE	D	X		8 BSC	
	E	Y		8 BSC	
LEAD PITCH	e			0.4 BSC	
EP SIZE	J	X	4.5	4.6	4.7
	K	Y	4.5	4.6	4.7
LEAD LENGTH	L		0.35	0.4	0.45
PACKAGE EDGE TOLERANCE	aaa			0.1	
MOLD FLATNESS	bbb			0.1	
COPLANARITY	ccc			0.08	
LEAD OFFSET	ddd			0.1	
EXPOSED PAD OFFSET	eee			0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.



Note: For the most current package drawings, see the Microchip Packaging Specifications located at http://www.microchip.com/packaging.

10. Reflow Profile and Storage Condition

This section describes about the Solder Reflow Recommendation and Storage Condition of the IS2062GM/64GM SoC.

10.1 Solder Reflow Recommendation

Refer to Microchip Technology Application Note *"AN233 Solder Reflow Recommendation"* (DS00000233) for the soldering reflow recommendations from the Microchip website: http://ww1.microchip.com/downloads/en/appnotes/00233d.pdf.

10.2 Storage Condition

Users must follow these specific storage conditions for the IS2062/64 SoC.

- Calculated shelf life in the sealed bag: 24 months at <40℃ and <90% Relative Humidity (RH)
- Once the bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, that is <30℃ /60% RH

The following figure illustrates the IS2062/64 SoC bag label details.

Figure 10-1. STORAGE CONDITIONS

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
3
If blank, see adjacent bar code label

1. Calculated shelf life in sealed bag : 24 months at < 40°C and <90% relative humidity (RH)
2. Peak package body temperature:_____°C
   If blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within:___168___ hours of factory conditions
      If blank, see adjacent bar code label
      ≤30°C/60% RH, or
   b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23± 5°C
   b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date: _____
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

11. Ordering Information

The following table provides the ordering information of the IS2062/64 SoC.

Table 11-1. ORDERING INFORMATION

Device	Description	Package	Part Number
IS2062GM	Bluetooth Audio Dual mode, Flash SoC, 2 microphones, Analog output	• 7x7x1.0 mm • 56-LGA	IS2062GM-012
IS2064GM	Bluetooth Audio Dual mode, Flash SoC, 1 microphone, Analog and I^2S output	• 8x8x1.0 mm • 68-LGA	IS2064GM-012
	Bluetooth Audio Dual mode, Flash SoC, 1 microphone, LDAC and I^2S output		IS2064GM-0L3
IS2064S	Bluetooth Audio Dual mode, ROM SoC, 1 microphone, Analog and I^2S output	• 8x8x0.9 mm • 68-QFN	IS2064S-114SM
IS2064B	Bluetooth Audio Dual mode, ROM SoC, 2 microphone, Analog and I^2S output	• 5x5x0.9 mm • 61-BGA	IS2064B-114SM

Note: The IS2062/64 SoC is purchased through a Microchip representative. Visit http://www.microchip.com/ for ordering information.

12. Reference Circuit

This section provides the reference schematics of IS2062GM, IS2064GM, IS2064S and IS2064B used in a stereo headset application.

The following figures illustrate the IS2062GM reference schematics for the stereo headset application.

Figure 12-1. IS2062GM REFERENCE CIRCUIT FOR STEREO HEADSET

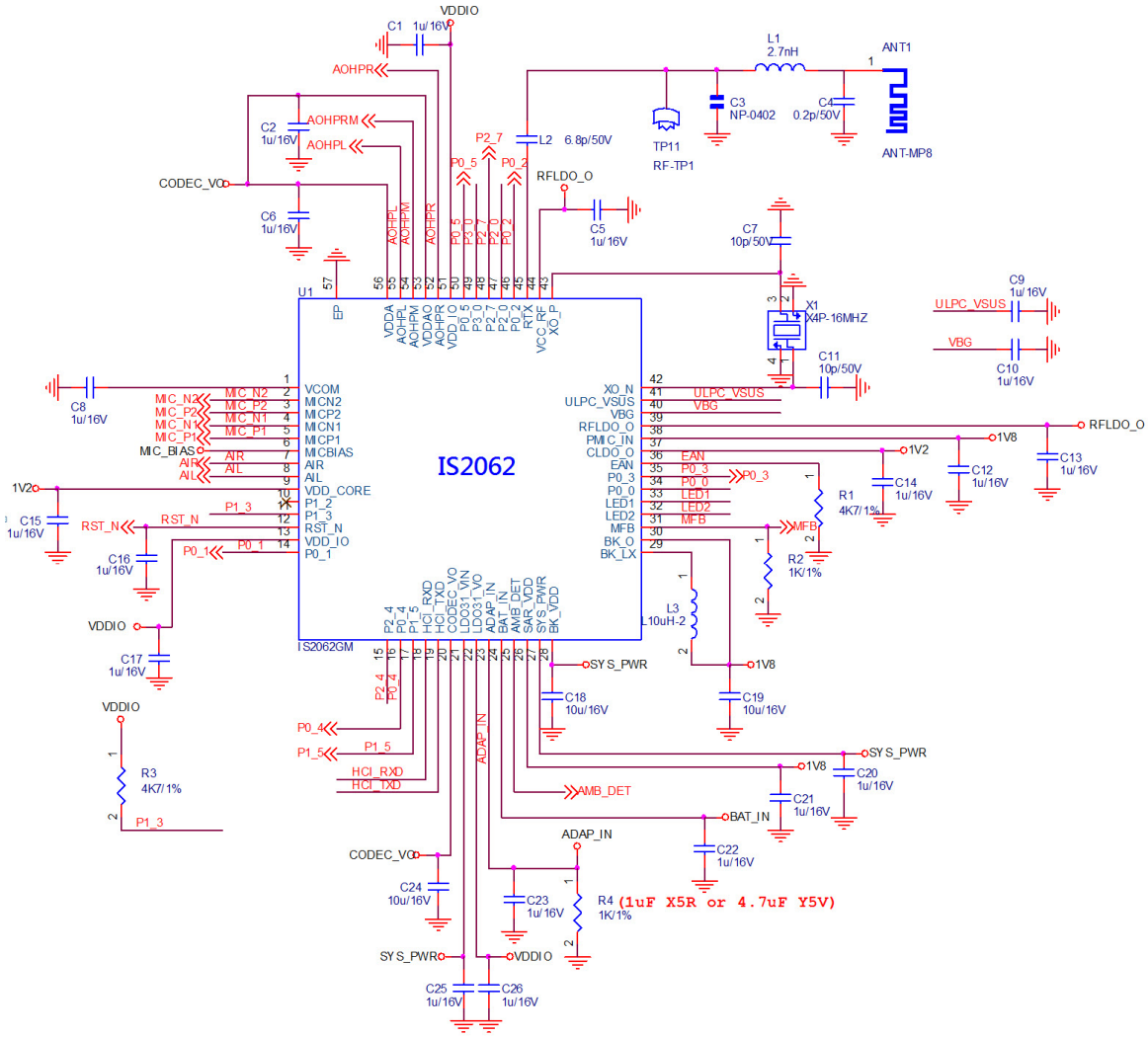
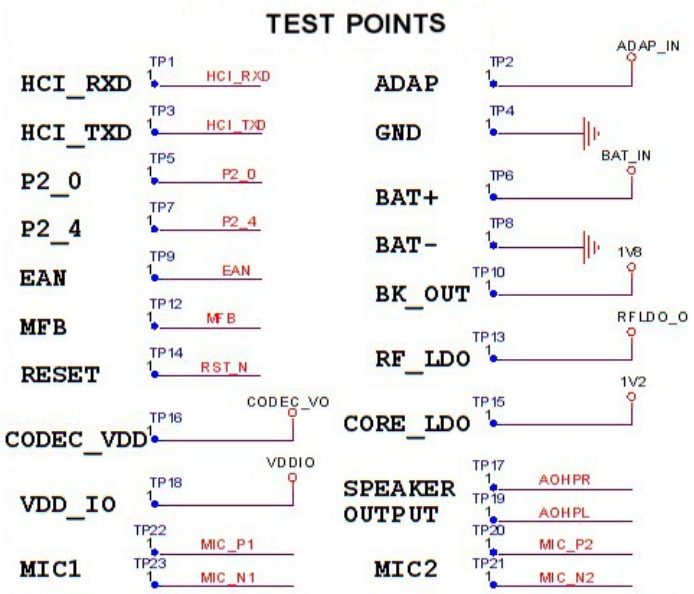
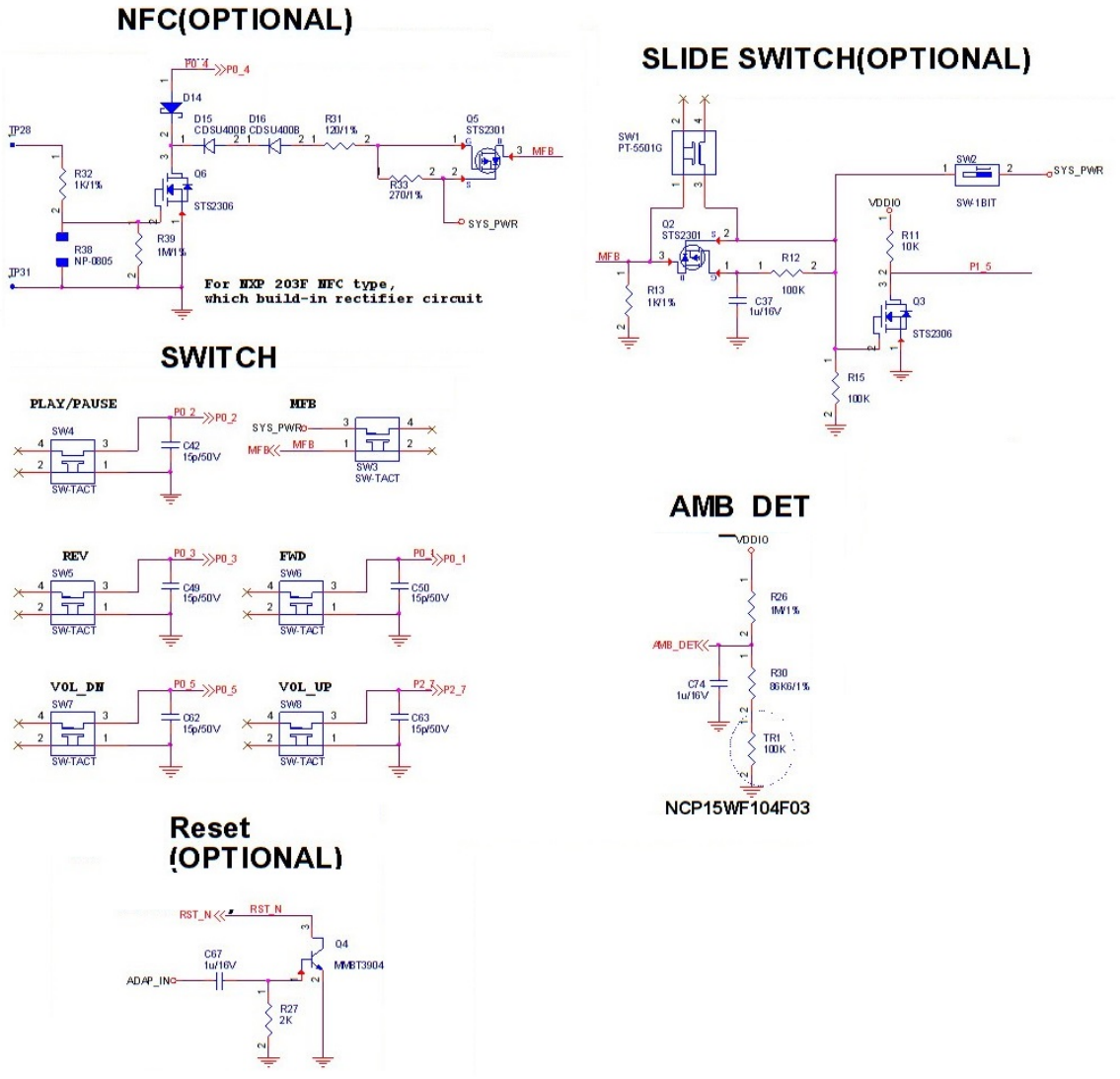


Figure 12-2. IS2062GM REFERENCE CIRCUIT FOR STEREO HEADSET



	GPIO Description (General)
P0_0	TX_IND
P0_1	FWD
P0_2	Play/Pause
P0_3	REV
P0_4	NFC
	External Amplifier Enable
P0_5	Volume down
P1_5	SLIDE SWITCH
	External Amplifier Enable
P2_0	System Configuration
P2_4	System Configuration
P2_7	Volume up
P3_0	Line-in detection

Figure 12-3. IS2062GM REFERENCE CIRCUIT FOR STEREO HEADSET



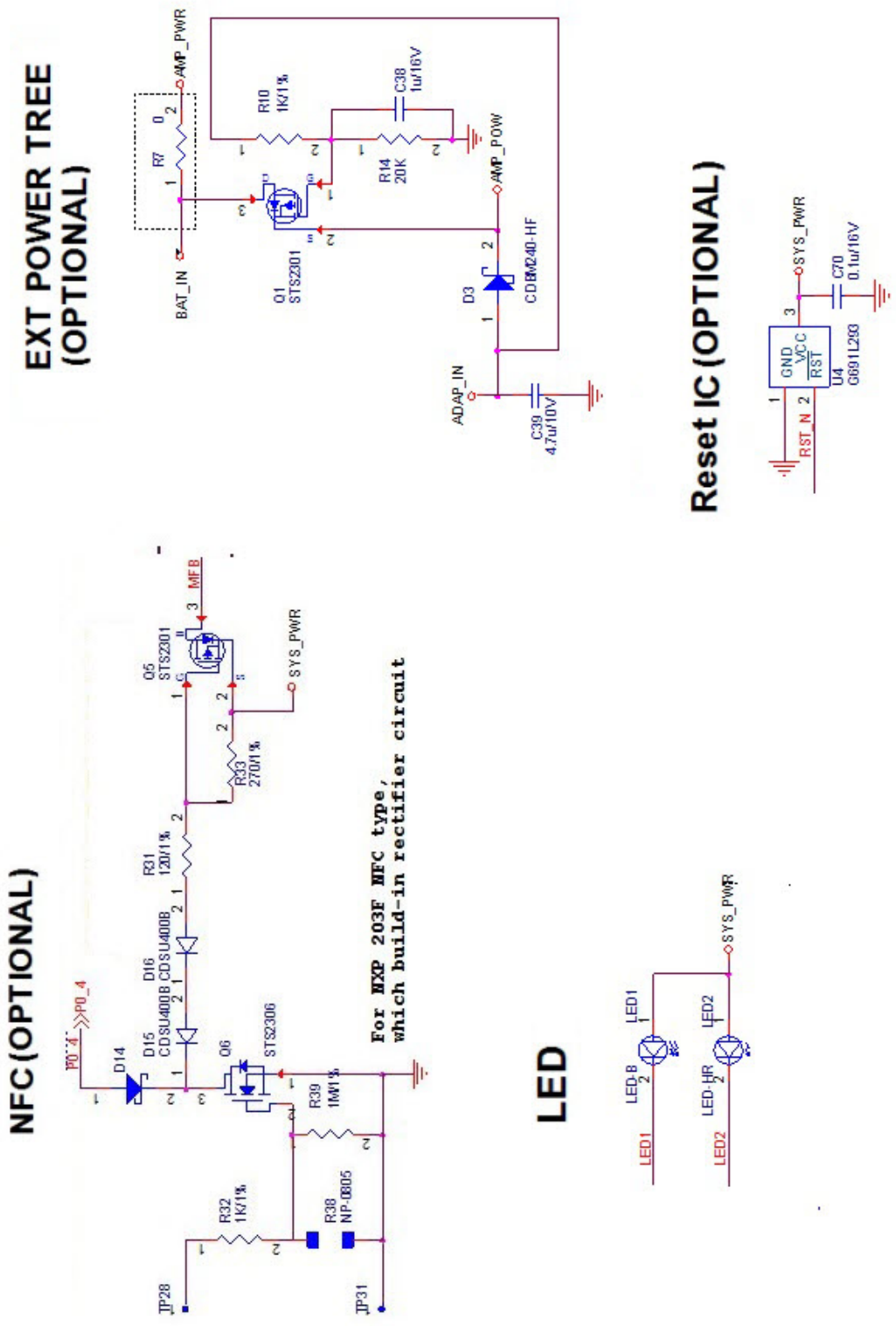


Figure 12-4. IS2062GM REFERENCE CIRCUIT FOR STEREO HEADSET

Figure 12-5. IS2062GM REFERENCE CIRCUIT FOR STEREO HEADSET

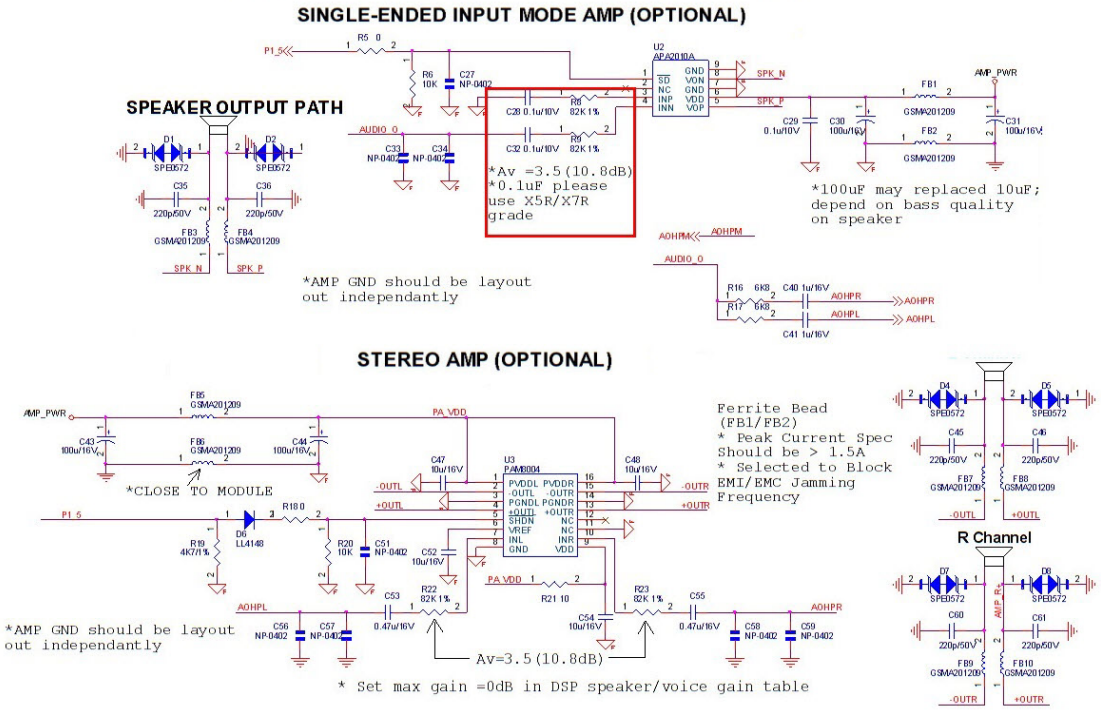
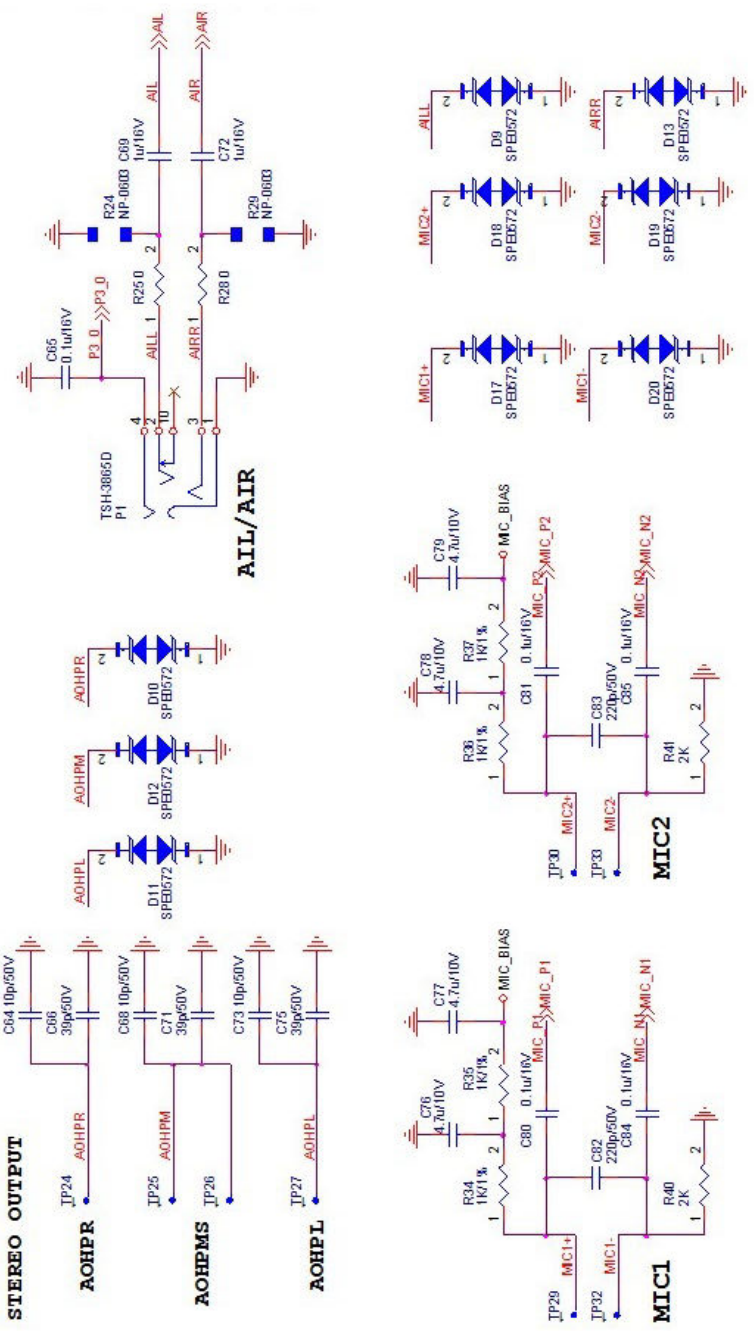


Figure 12-6. IS2062GM REFERENCE CIRCUIT FOR STEREO HEADSET



Note: All ESD diodes in these schematics are reserved for the testing.

The following figures illustrate the IS2064GM (IS2064GM-012/IS2064GM-0L3) reference schematics for the stereo headset application.

Note: The AOHPR, AOHPL, and AOHPM pins shown in the following schematic are not applicable for IS2064GM-0L3 as there is no analog audio output pin. These pins should be left unconnected.

Figure 12-7. IS2064GM REFERENCE CIRCUIT FOR STEREO HEADSET

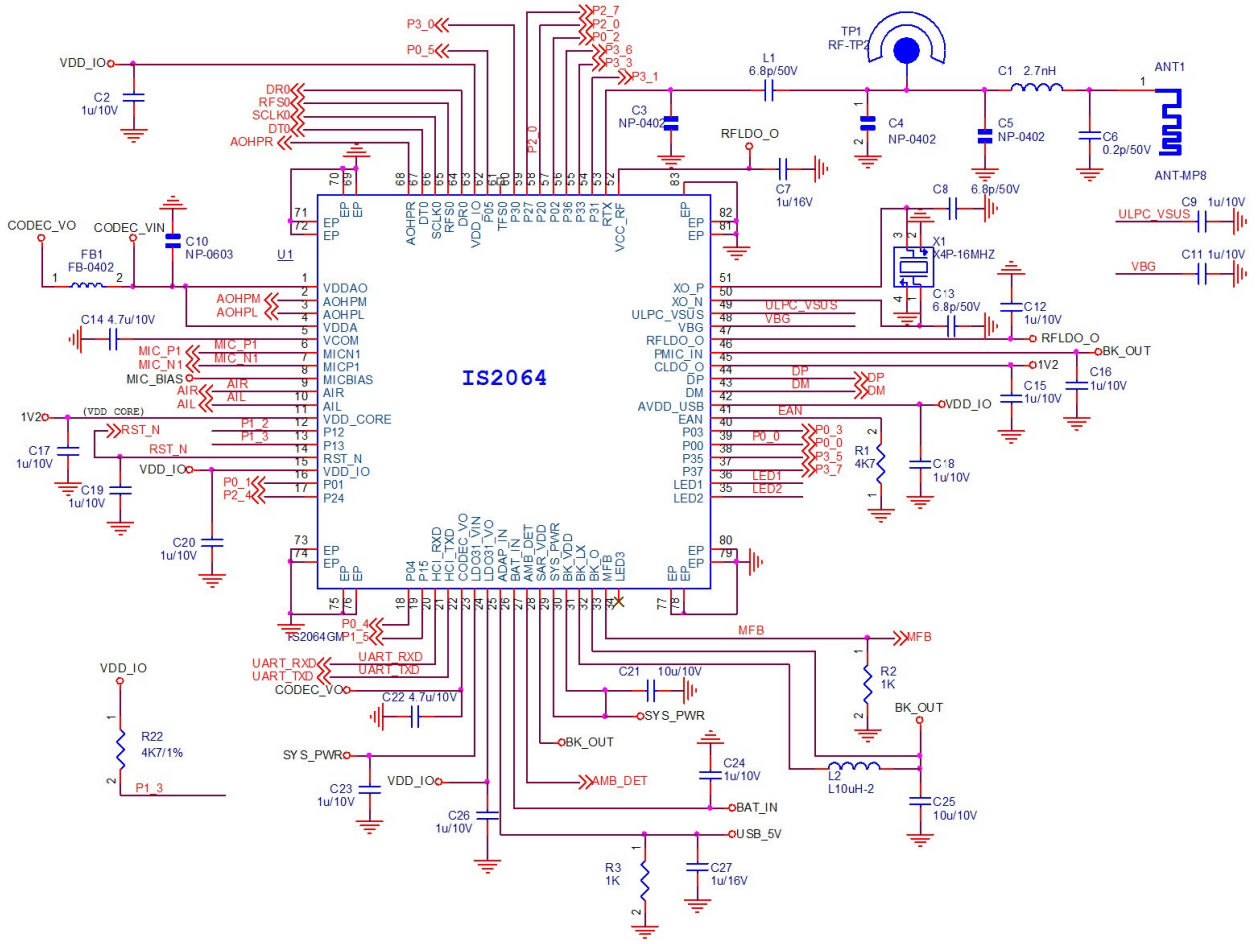
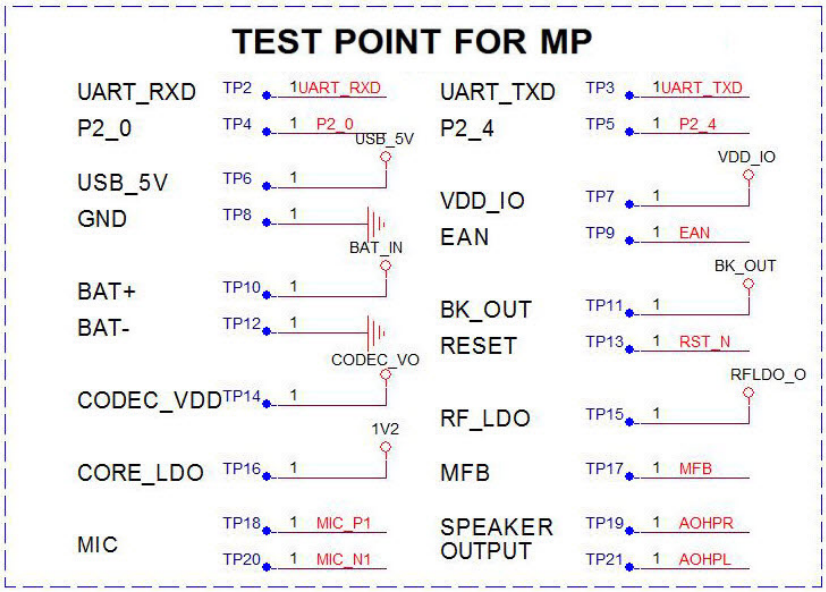


Figure 12-8. IS2064GM REFERENCE CIRCUIT FOR STEREO HEADSET



GPIO DESCRIPTION

MFB	UART_RX_IND; MFB
P0_0	SLIDE SWITCH
P0_2	PLAY/PAUSE
P0_4	AMP_EN/NFC
P0_5	VOL-
P2_7	VOL+
P3_0	AUX IN Detection
P3_7	UART_TX_IND
P1_5	AMP_EN/SLIDE SWITCH
	Single/Double setting
P3_6	Single/Double setting
P2_0	System Configuration
EAN	System Configuration

Figure 12-9. IS2064GM REFERENCE CIRCUIT FOR STEREO HEADSET

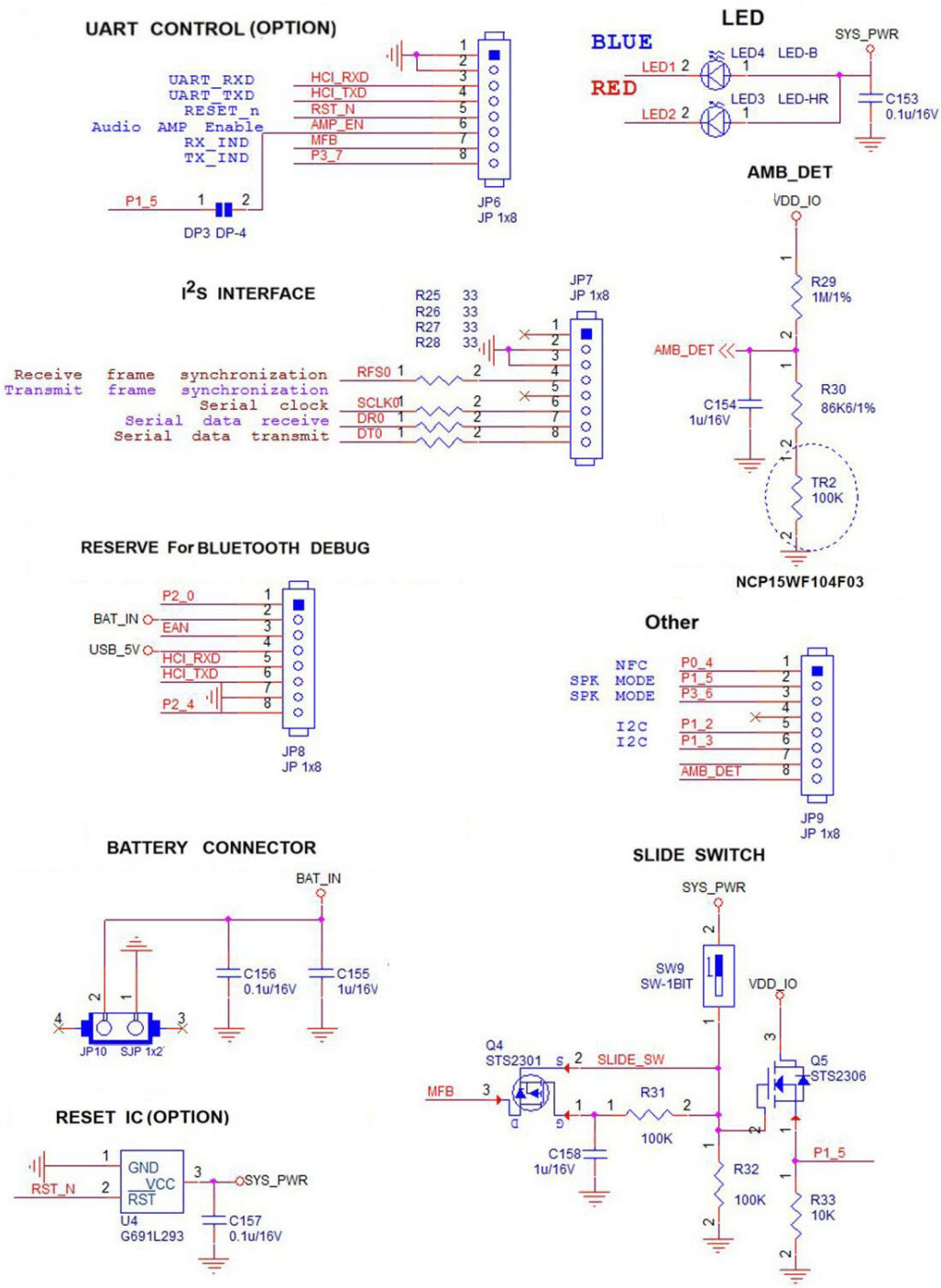
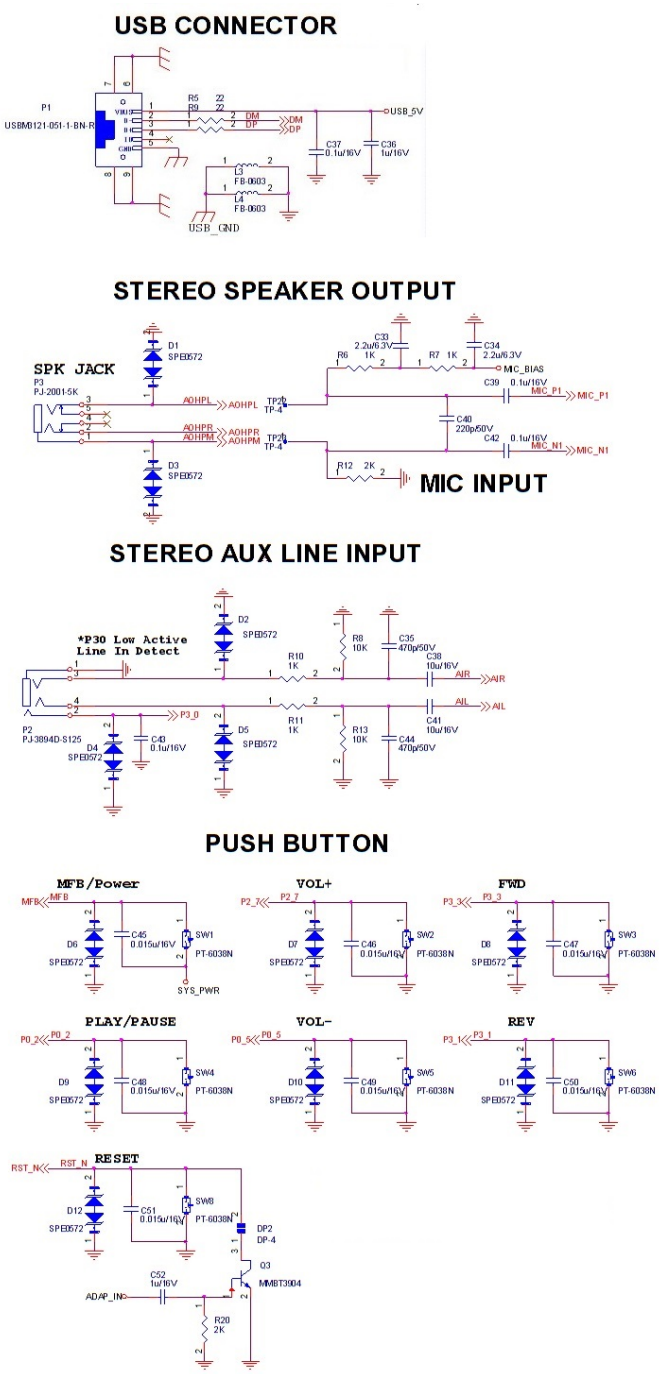


Figure 12-10. IS2064GM REFERENCE CIRCUIT FOR STEREO HEADSET



Note: All ESD diodes in these schematics are reserved for the testing.

The following figures illustrate the IS2064S reference schematics for a stereo headset application.

Figure 12-11. IS2064S REFERENCE CIRCUIT FOR STEREO HEADSET

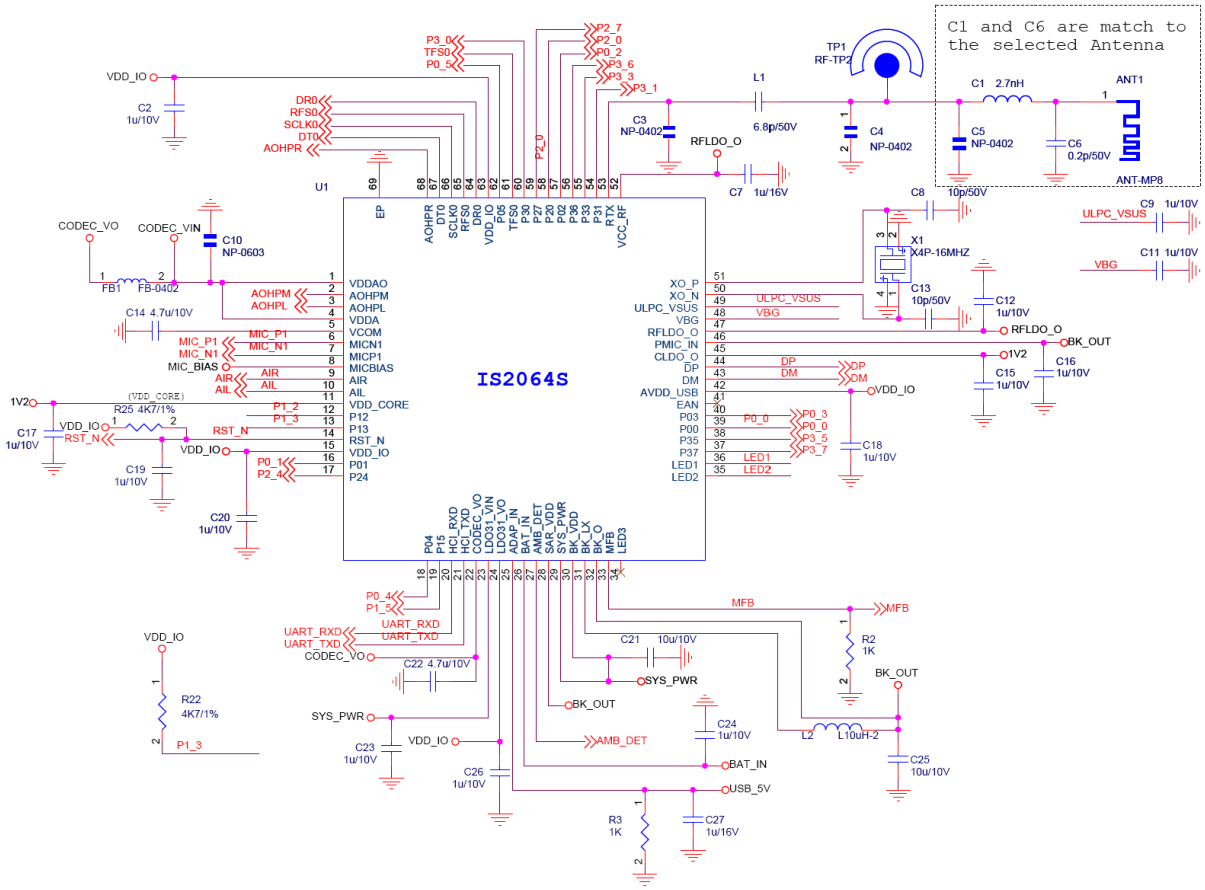


Figure 12-12. IS2064S REFERENCE CIRCUIT FOR STEREO HEADSET

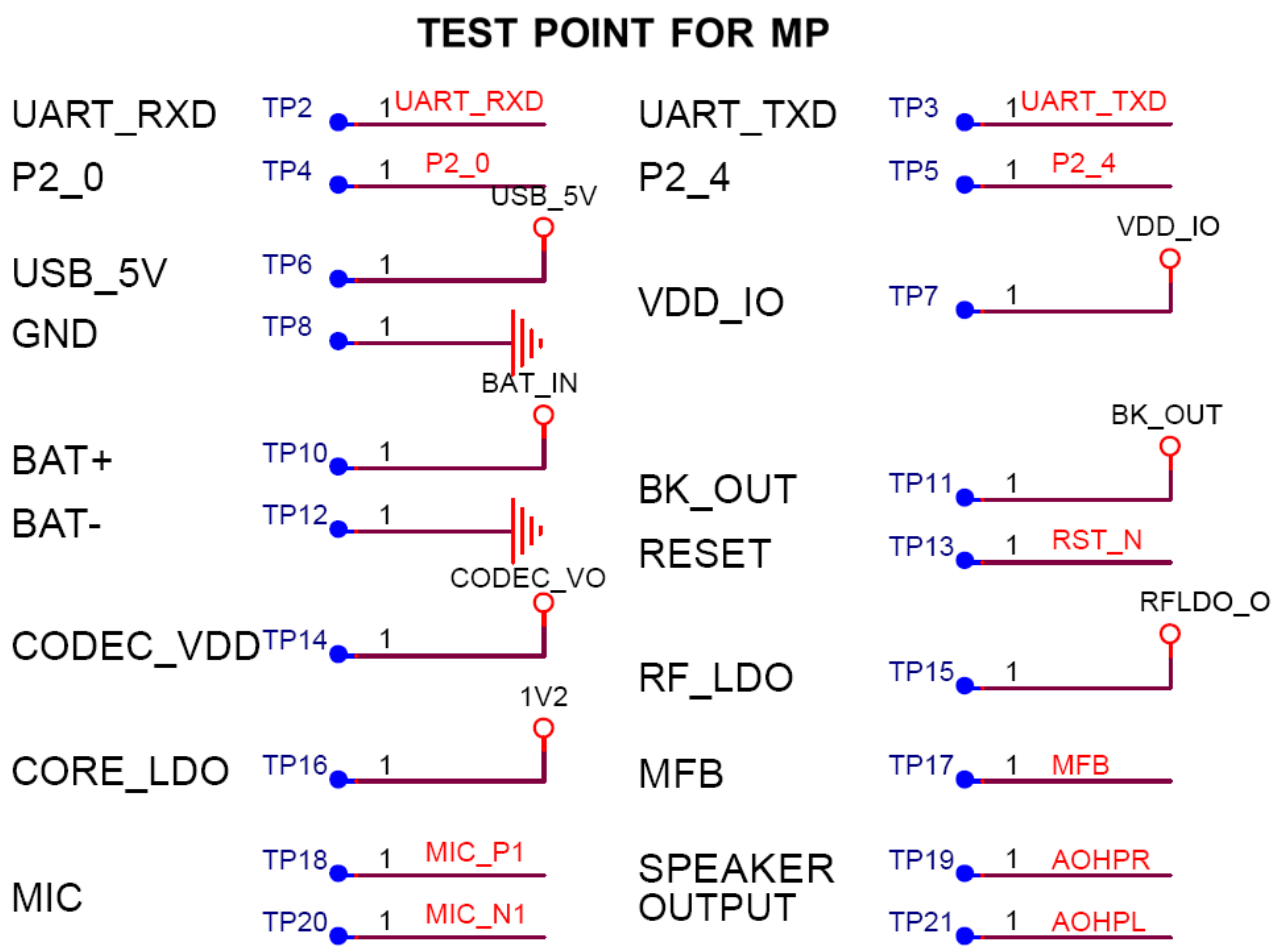
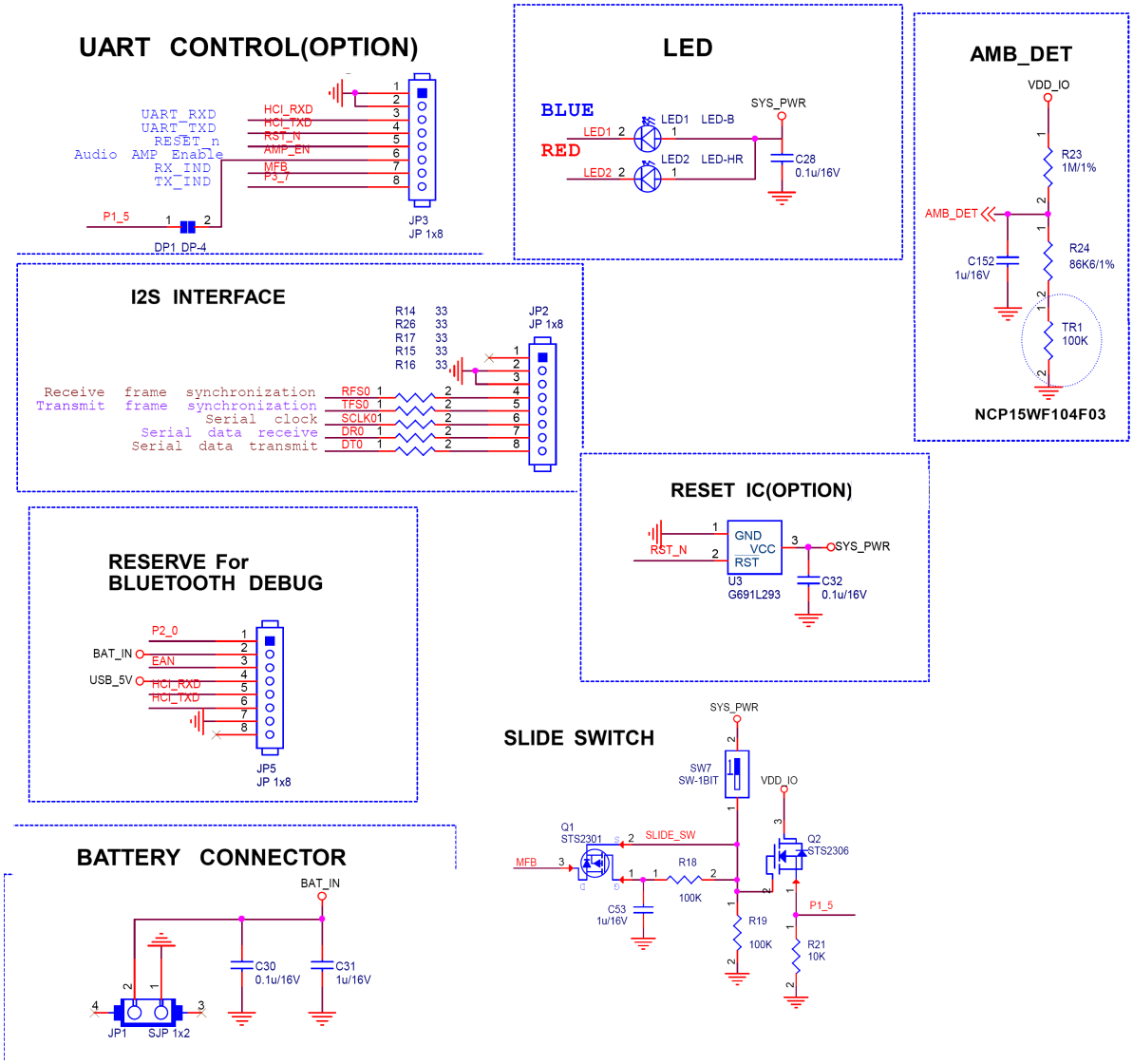


Figure 12-13. IS2064S REFERENCE CIRCUIT FOR STEREO HEADSET



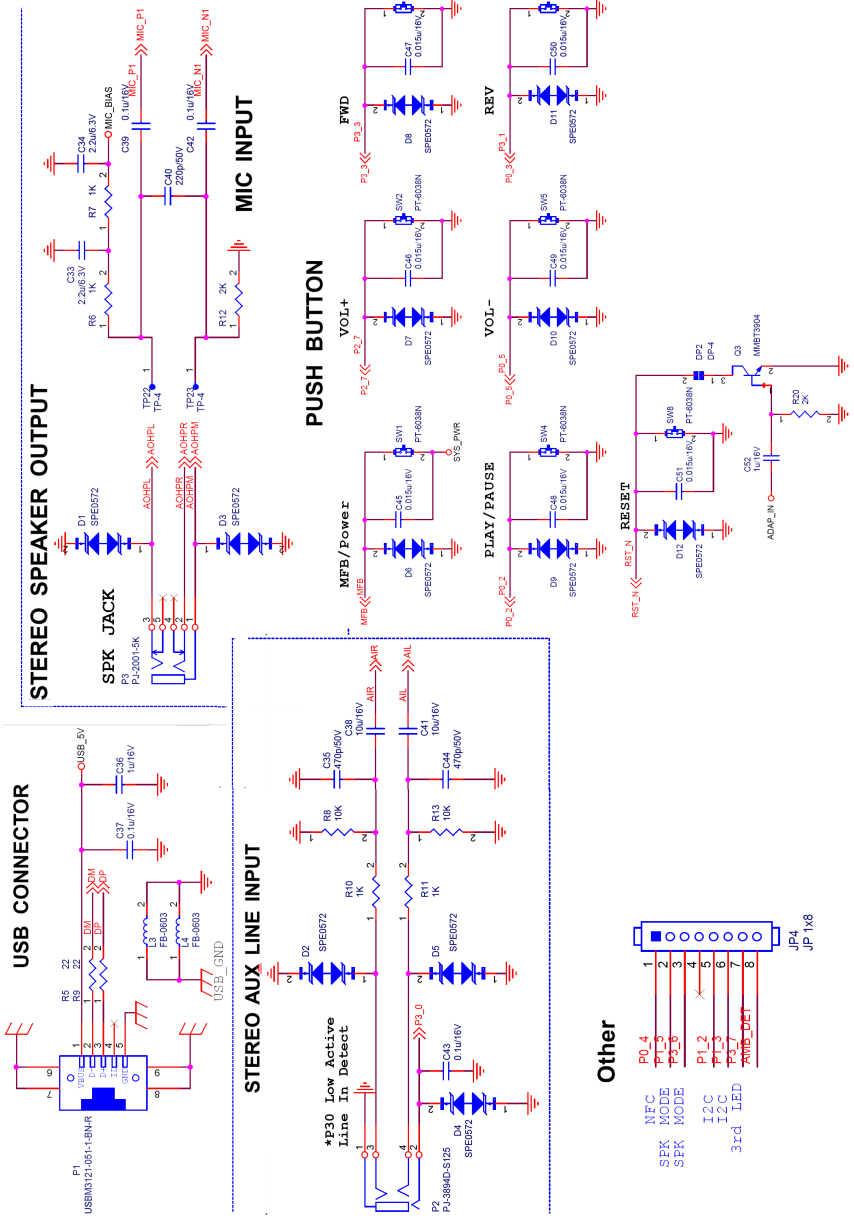


Figure 12-14. IS2064S REFERENCE CIRCUIT FOR STEREO HEADSET

Note: All EDS diodes in these schematics are reserved for testing and can be removed, if ESD is passed without adding it.

The following figures illustrate the IS2064B reference schematics for the stereo headset application.

Figure 12-15. IS2064B REFERENCE CIRCUIT FOR STEREO HEADSET

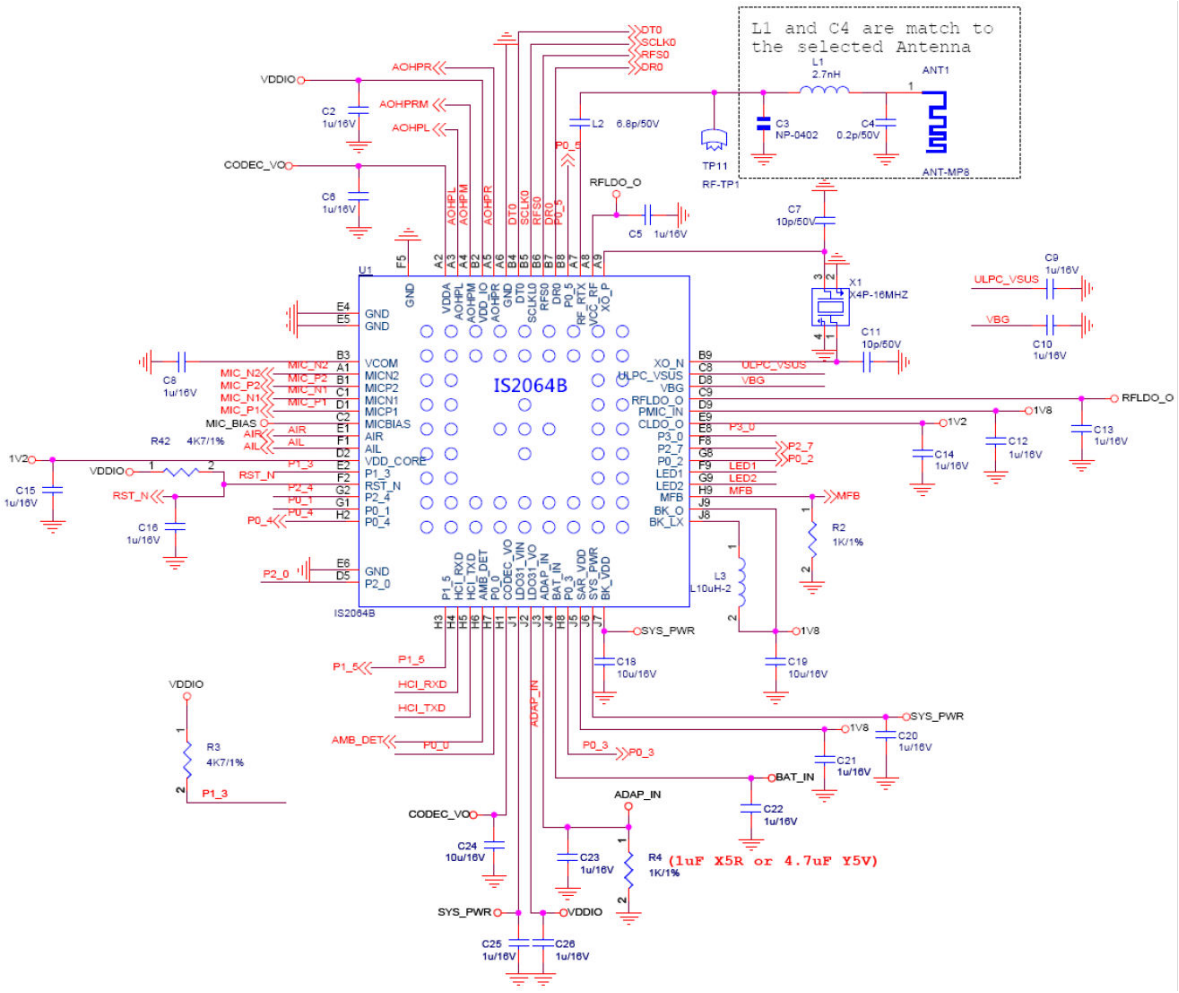


Figure 12-16. IS2064B REFERENCE CIRCUIT FOR STEREO HEADSET

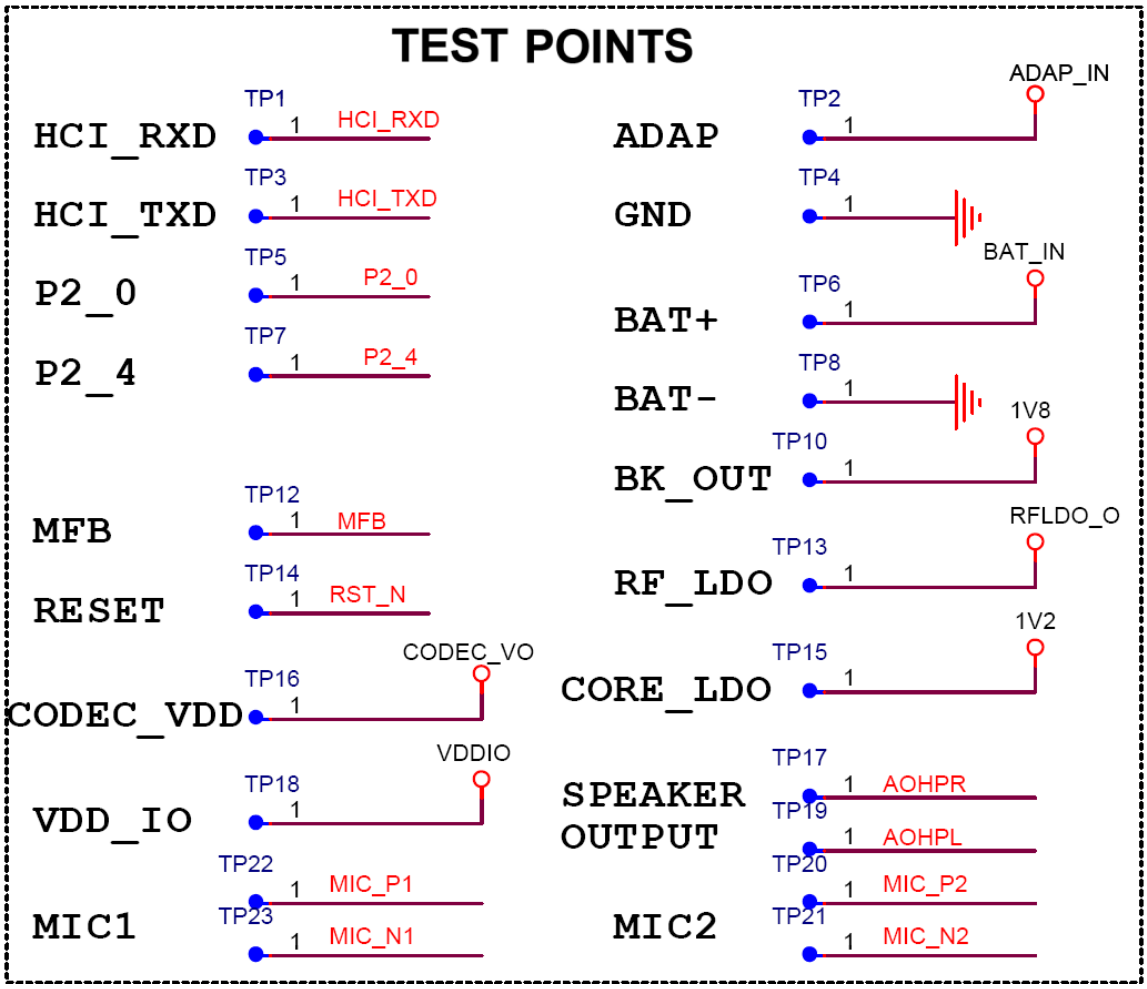
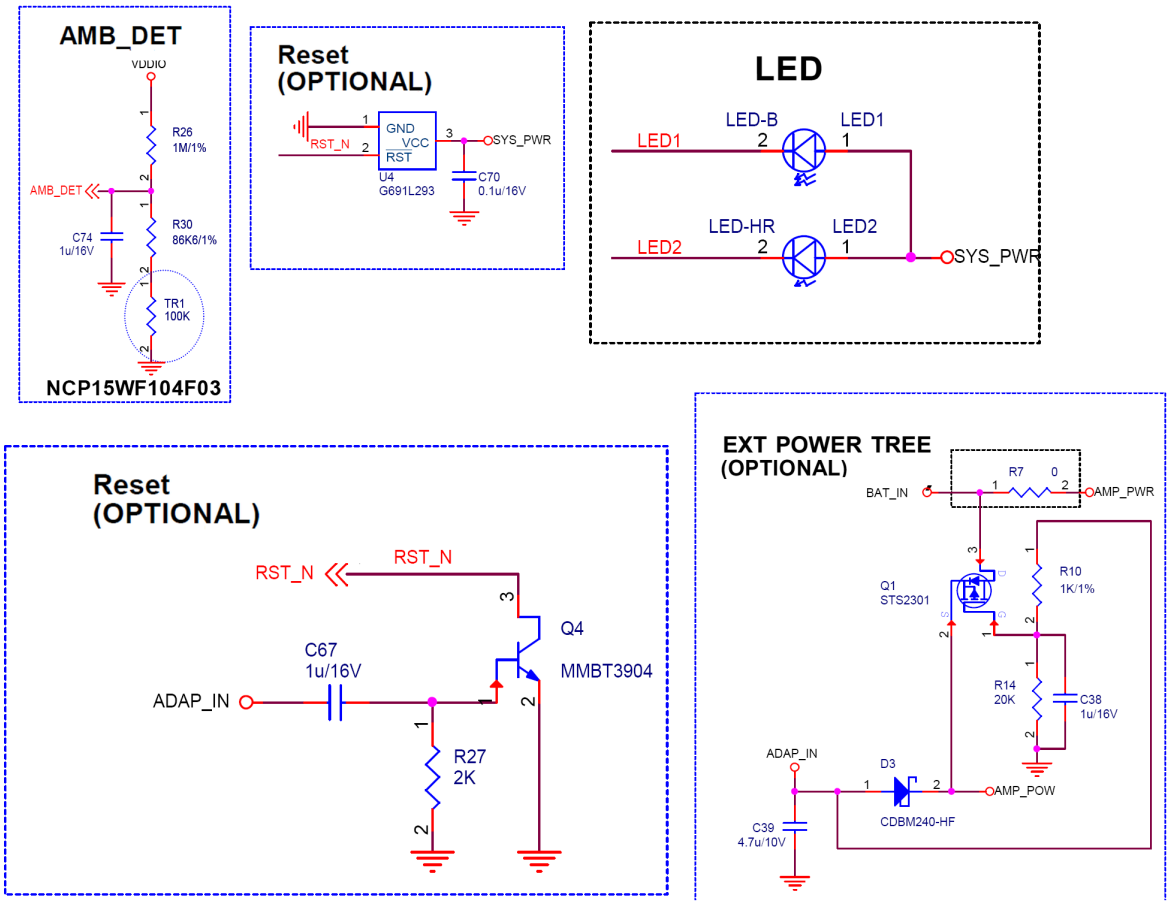


Figure 12-17. IS2064B REFERENCE CIRCUIT FOR STEREO HEADSET



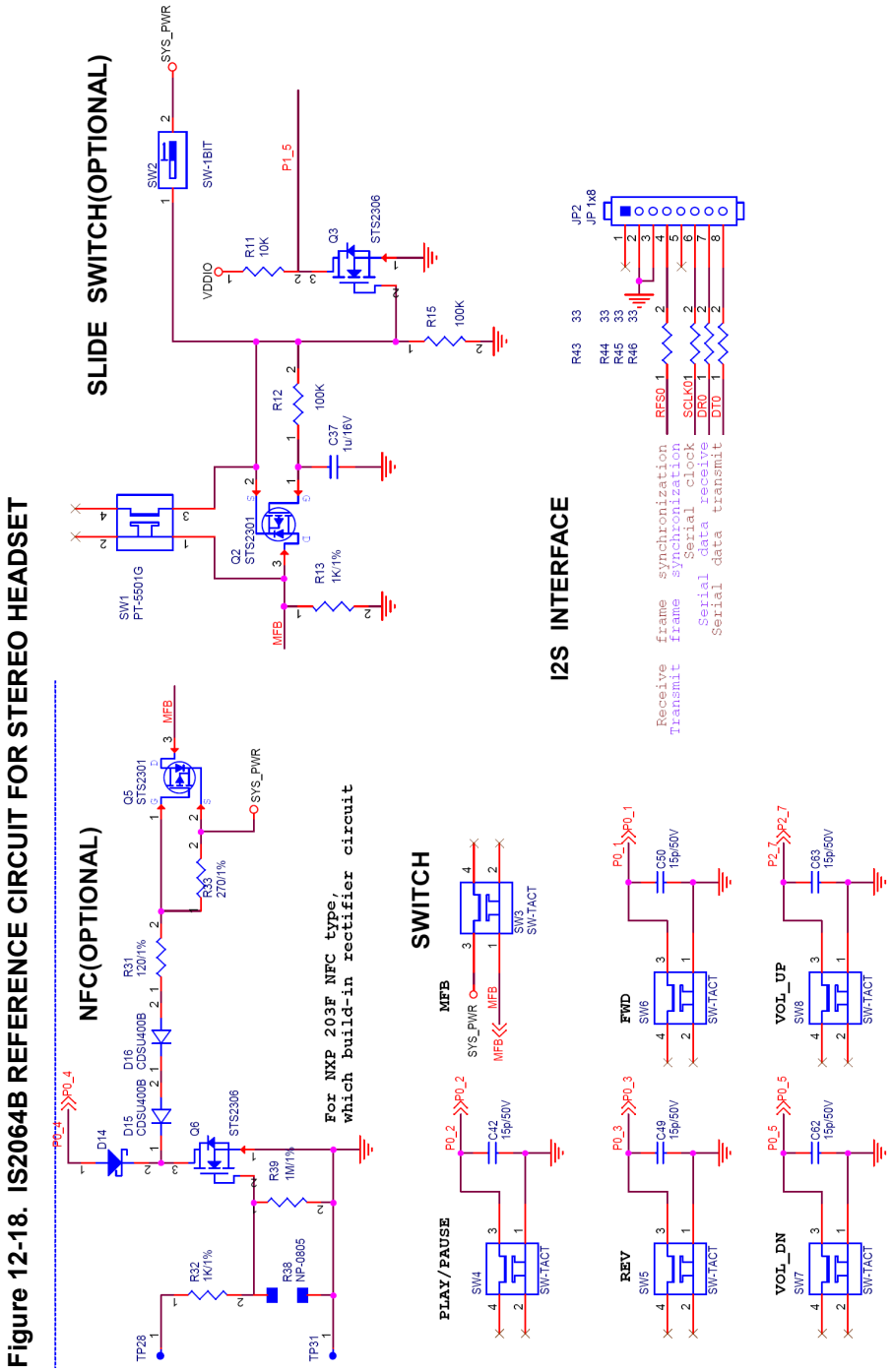


Figure 12-18. IS2064B REFERENCE CIRCUIT FOR STEREO HEADSET

Figure 12-19. IS2064B REFERENCE CIRCUIT FOR STEREO HEADSET

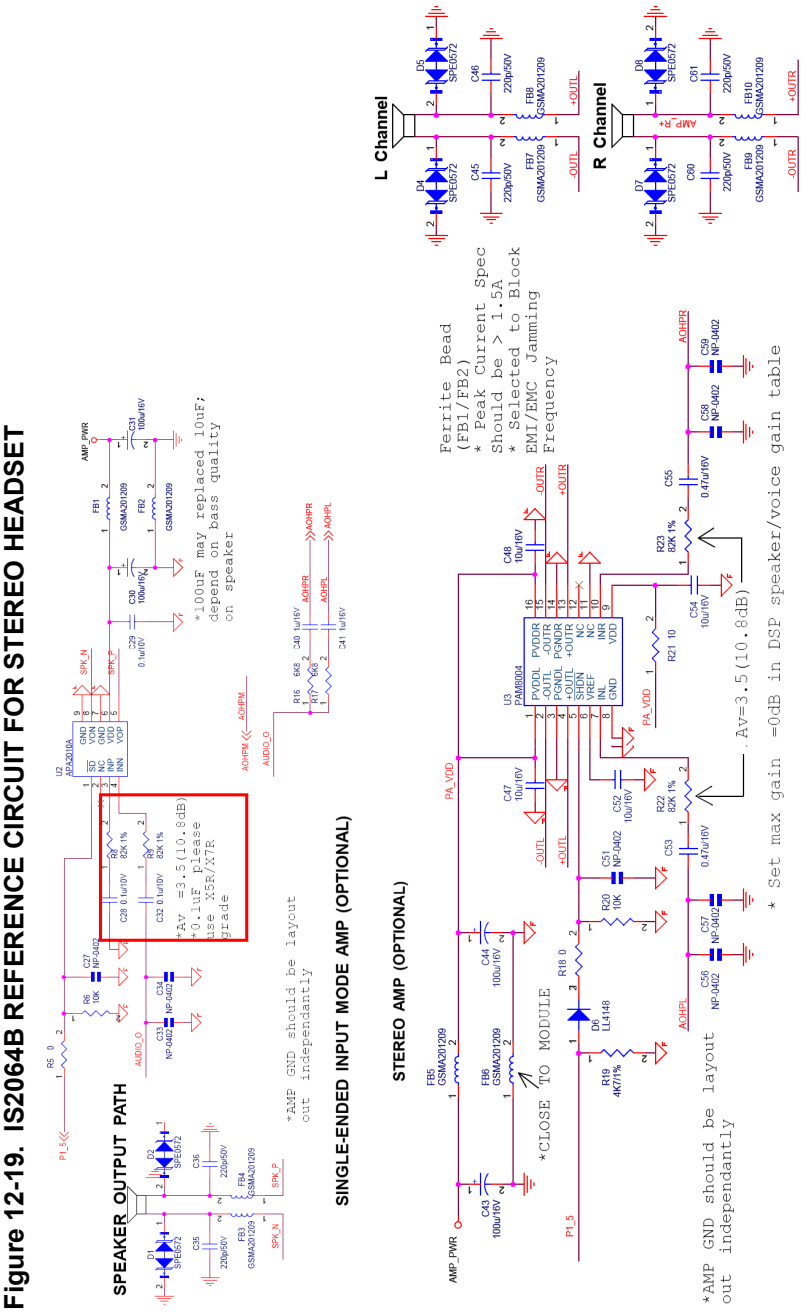
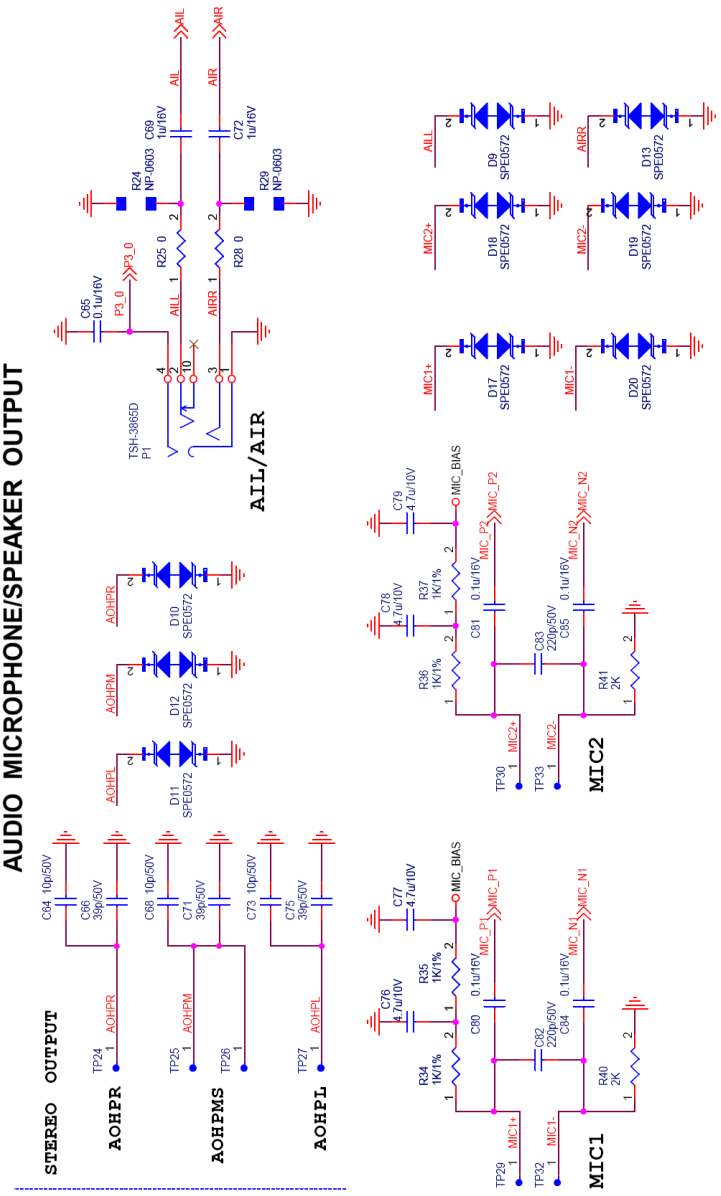


Figure 12-20. IS2064B REFERENCE CIRCUIT FOR STEREO HEADSET



Note: All ESD diodes in these schematics are reserved for testing and can be removed, if ESD is passed without adding it.

13. Document Revision History

Revision A (May 2016)

This is the initial released version of this document.

Revision B (December 2016)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Table 13-1. MAJOR SECTION UPDATES

Section	Changes
Audio Codec	Updated the I^2S digital audio applicability.
Peripherals	Updated the USB version details.
Device Overview	Updated Figure 1-1 and Figure 1-2. Added “USB” details and updated “Customized voice prompt” details in Table 1-1. Updated Table 1-1 through Table 1-3.
Codec	Added a note for internal codec support and addition of trailing zeros.
Application Information	Added Note 2 for usage of BAT_IN or ADAP_IN pins. Updated Figure 6-1. Updated Table 6-4 and deleted Table 6-5.
Reference Circuit	Updated Figure 12-8 and Figure 12-9.

Revision C (July 2017)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Table 13-2. MAJOR SECTION UPDATES

Section	Changes
Document	• Added ROM variant information of IS2062/64 family. • Updated the document as per latest template.

Revision D (June 2017)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Table 13-3. MAJOR SECTION UPDATES

Section	Changes
Document	• Added ROM variant information of IS2062/64 family. • Updated the document as per latest template.

Revision E (August 2018)

This revision includes the update related to IS2064GM-0L3 device variant and text update, which were incorporated throughout the document.

Table 13-4. MAJOR SECTION UPDATES

Section	Changes
Document	Updated Bluetooth version 4.2 to 5.0
Introduction	Updated Flash-based devices description
Audio Codec	Updated with LDAC decoding for IS2064GM-0L3 devices
1.1 Key Features	Updated the table with IS2064GM-0L3 device features
Figure 1-2	Updated an image with '*' and added a note
Table 1-2	Updated the table IS2064GM-0L3 device details
Figure 2-2	Updated an image with LDAC feedback
Table 6-1	Updated System Configuration Settings table
Table 8-12	Added a table
Figure 9-1	Updated an images with IS2064GM-0L3 device
Table 11-1	Updated the table with IS2064GM-0L3 device variant ordering details

Revision F (September 2018)

Section	Changes
Features	Added BLE data rate feature
Figure 6-8	Updated figure and figure footnotes

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