



Description

The HXY4612S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

General Features

$V_{DS} = 60V$ $I_D = 5A$

$R_{DS(ON)} < 70m\Omega @ V_{GS}=10V$

$V_{DS} = -60V$ $I_D = -4A$

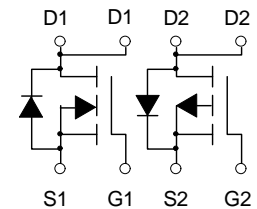
$R_{DS(ON)} < 140m\Omega @ V_{GS}=-10V$

Application

Wireless charging

Boost driver

Brushless motor



N-Channel and P-Channel

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HXY4612S	SOP-8	4612XXX	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	60	-60	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5	-4	A
$I_D @ T_A=70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.2	-2.6	A
IDM	Pulsed Drain Current ²	15	-13	A
EAS	Single Pulse Avalanche Energy ³	22	28.8	mJ
IAS	Avalanche Current	21	-24	A
$P_D @ T_A=25^{\circ}C$	Total Power Dissipation ⁴	2	2	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85		$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	62.5		$^{\circ}C/W$



N-Channel Electrical Characteristics (T_J =25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	65	---	V
ΔBVDSS/ΔTJ	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.063	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A	---	60	70	mΩ
		V _{GS} =4.5V, I _D =4A	---	78	90	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	1.75	2.5	V
ΔVGS(th)	V _{GS(th)} Temperature Coefficient		---	-5.24	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =48V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =4A	---	28	---	S
Q _g	Total Gate Charge (4.5V)	V _{DS} =48V, V _{GS} =4.5V, I _D =4A	---	19	---	nC
Q _{gs}	Gate-Source Charge		---	2.6	---	
Q _{gd}	Gate-Drain Charge		---	4.1	---	
Td(on)	Turn-On Delay Time	V _{DD} =30V, V _{GS} =10V , R _G =3.3Ω, I _D =4A	---	3	---	ns
T _r	Rise Time		---	34	---	
Td(off)	Turn-Off Delay Time		---	23	---	
T _f	Fall Time		---	6.0	---	
Ciss	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1027	---	pF
Coss	Output Capacitance		---	65	---	
Crss	Reverse Transfer Capacitance		---	45	---	
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	2.5	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation



P-Channel Electrical Characteristics (T_J =25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-60	-65	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.03	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-3A	---	120	140	mΩ
		V _{GS} =-4.5V, I _D =-2A	---	190	210	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.2	1.75	-2.5	V
IDSS	Drain-Source Leakage Current	V _{DS} =-48V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-48V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	8.5	---	S
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-48V, V _{GS} =-4.5V, I _D =-3A	---	12.1	---	nC
Q _{gs}	Gate-Source Charge		---	2.2	---	
Q _{gd}	Gate-Drain Charge		---	6.3	---	
Td(on)	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	9.2	---	ns
T _r	Rise Time		---	20.1	---	
Td(off)	Turn-Off Delay Time		---	46.7	---	
T _f	Fall Time		---	9.4	---	
Ciss	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1137	---	pF
Coss	Output Capacitance		---	76	---	
Crss	Reverse Transfer Capacitance		---	50	---	
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-2.5	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



N-Channel Typical Characteristics

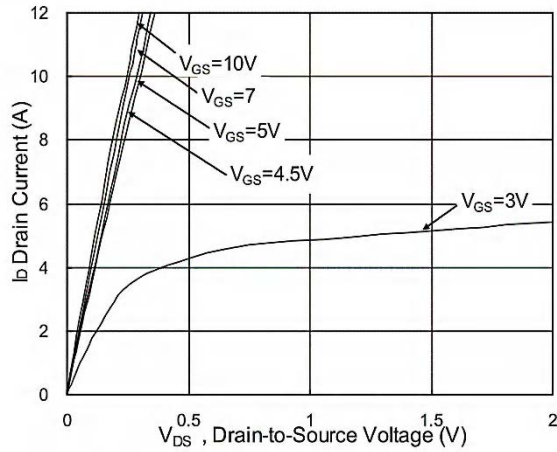


Fig.1 Typical Output Characteristics

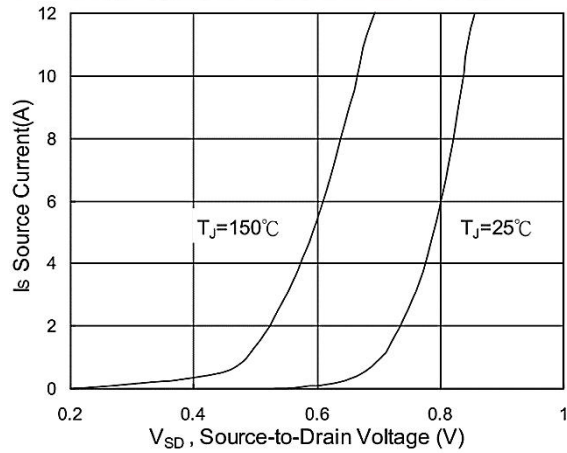


Fig.3 Source Drain Forward Characteristics

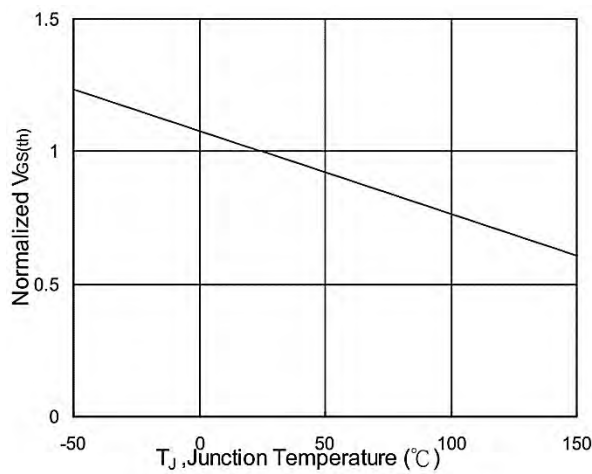


Fig.5 Normalized V_{GS(th)} vs. T_J

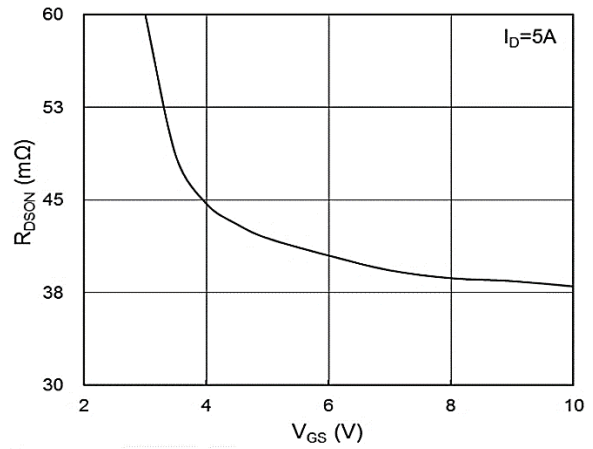


Fig.2 On-Resistance vs. G-S Voltage

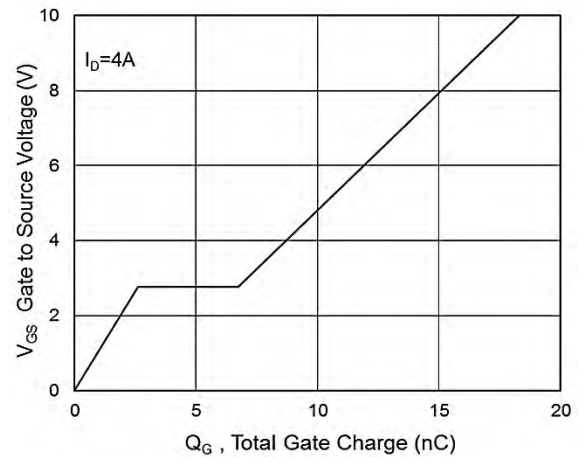


Fig.4 Gate-Charge Characteristics

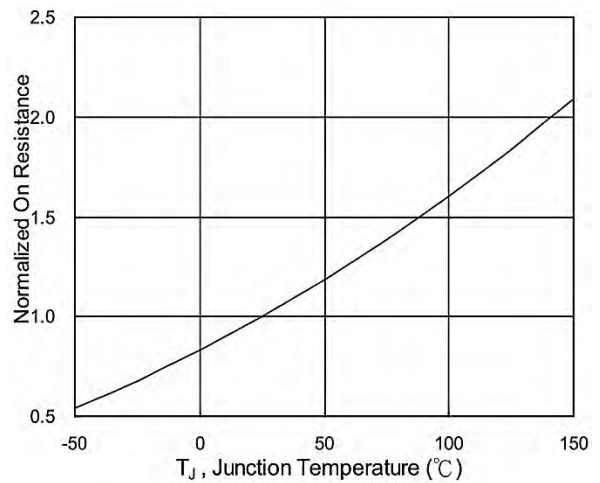


Fig.6 Normalized R_{DS(on)} vs. T_J

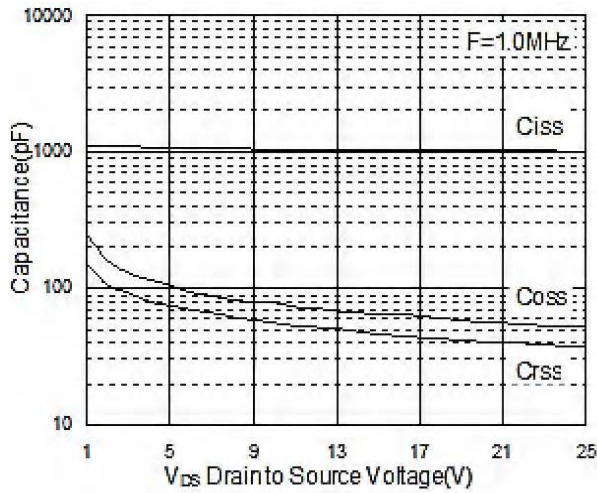


Fig.7 Capacitance

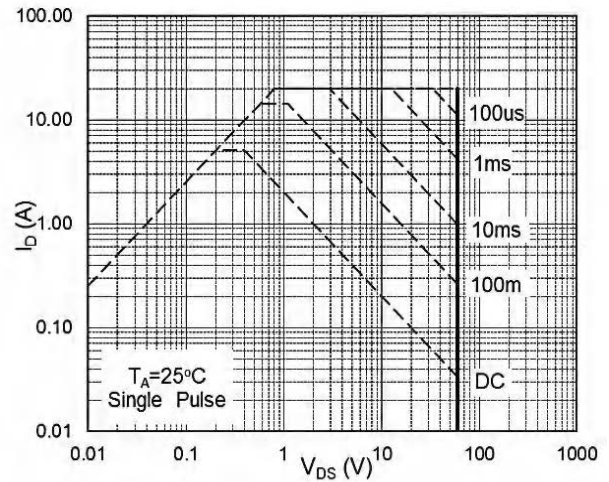


Fig.8 Safe Operating Area

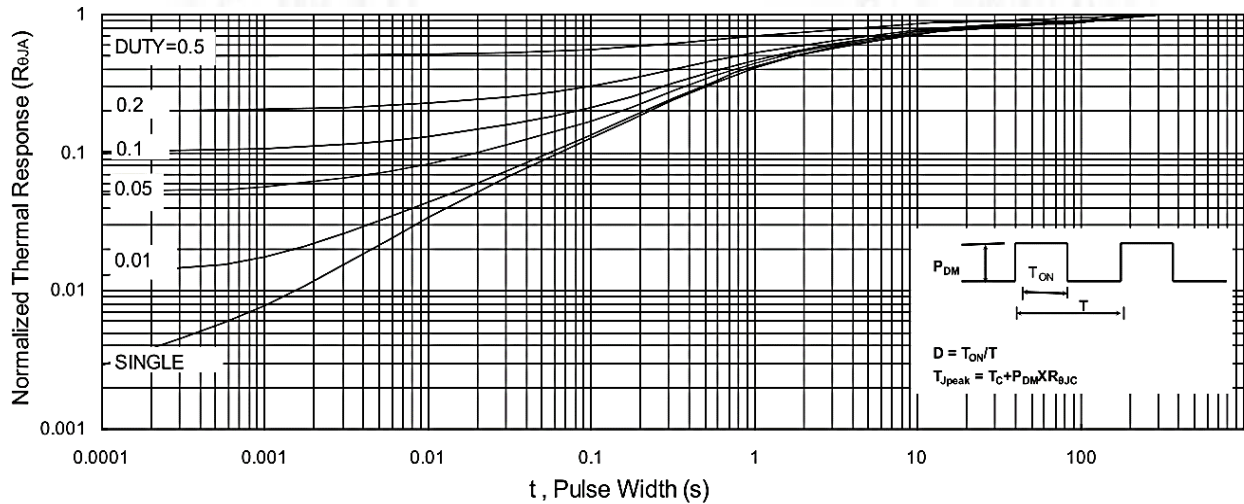


Fig.9 Normalized Maximum Transient Thermal Impedance

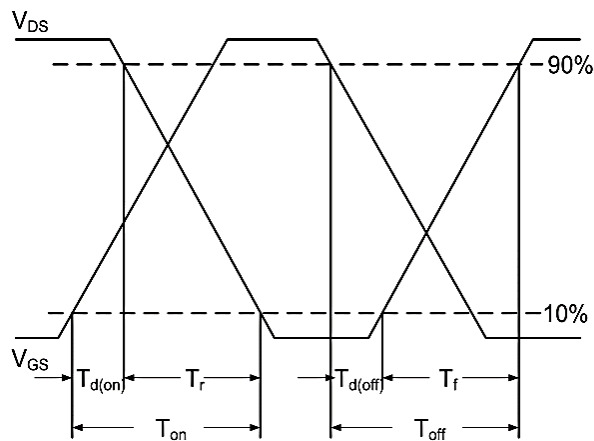


Fig.10 Switching Time Waveform

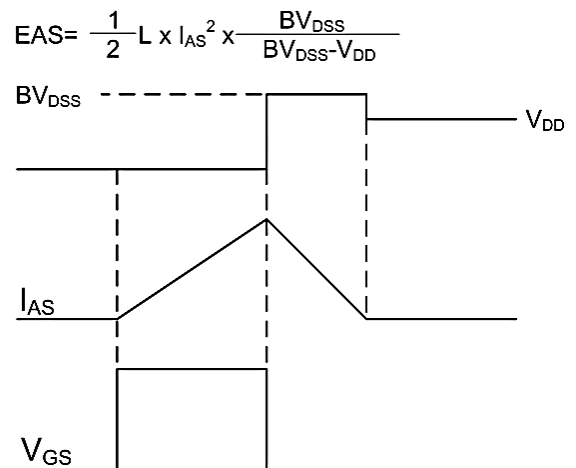


Fig.11 Unclamped Inductive Waveform



P-Channel Typical Characteristics

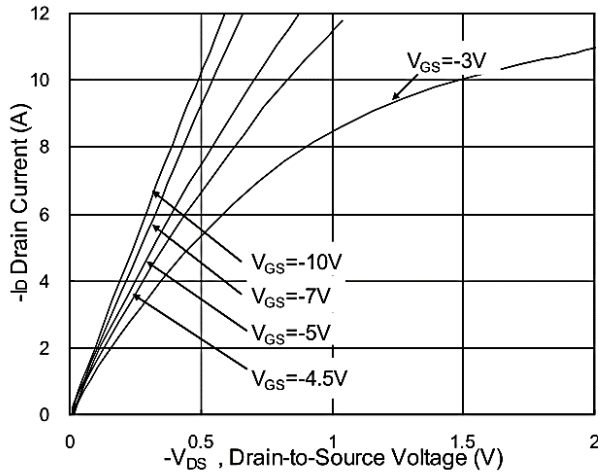


Fig.1 Typical Output Characteristics

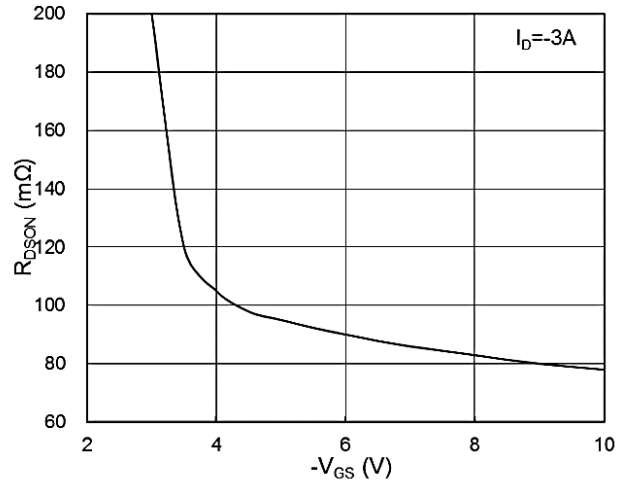


Fig.2 On-Resistance vs. G-S Voltage

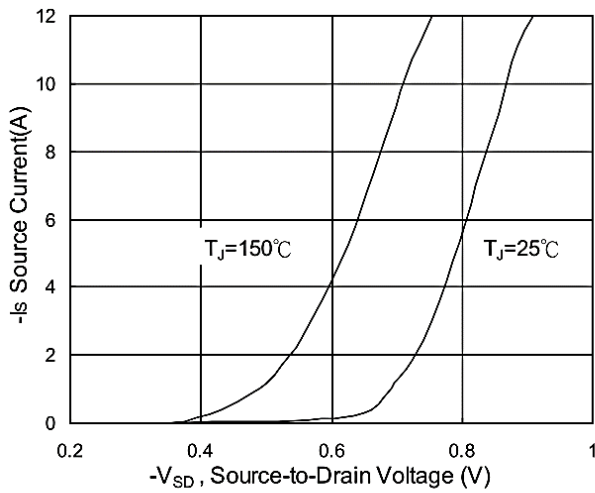


Fig.3 Source Drain Forward Characteristics

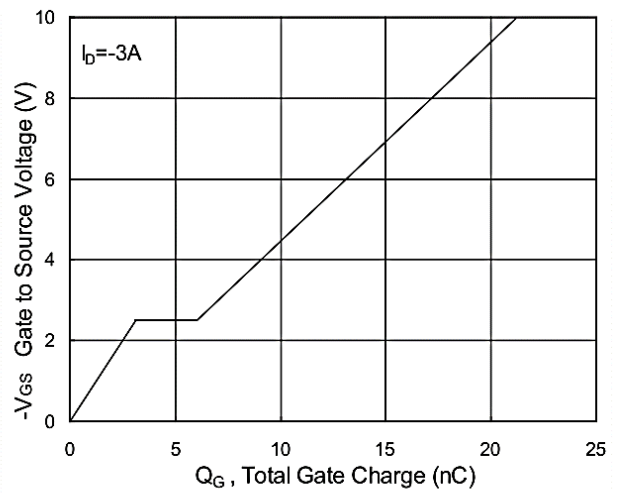


Fig.4 Gate-Charge Characteristics

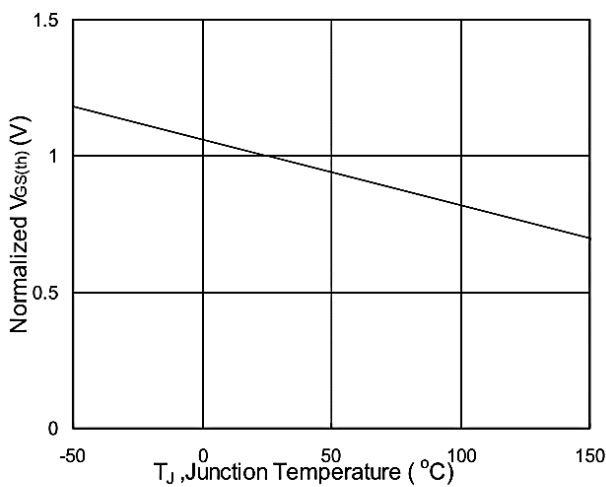


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

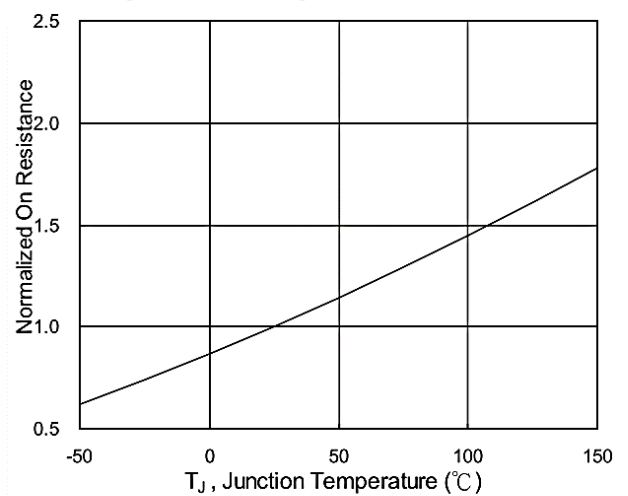


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

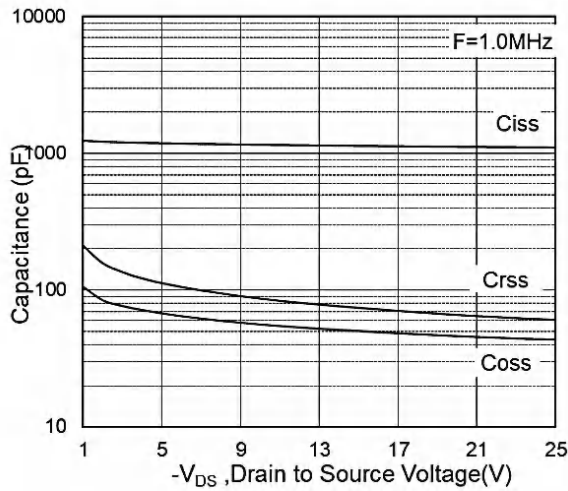


Fig.7 Capacitance

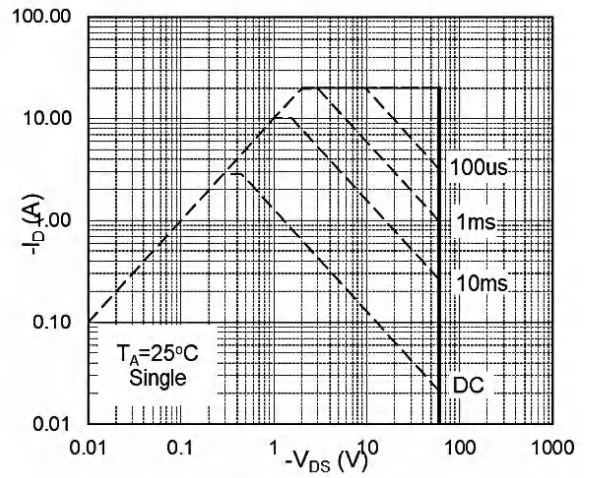


Fig.8 Safe Operating Area

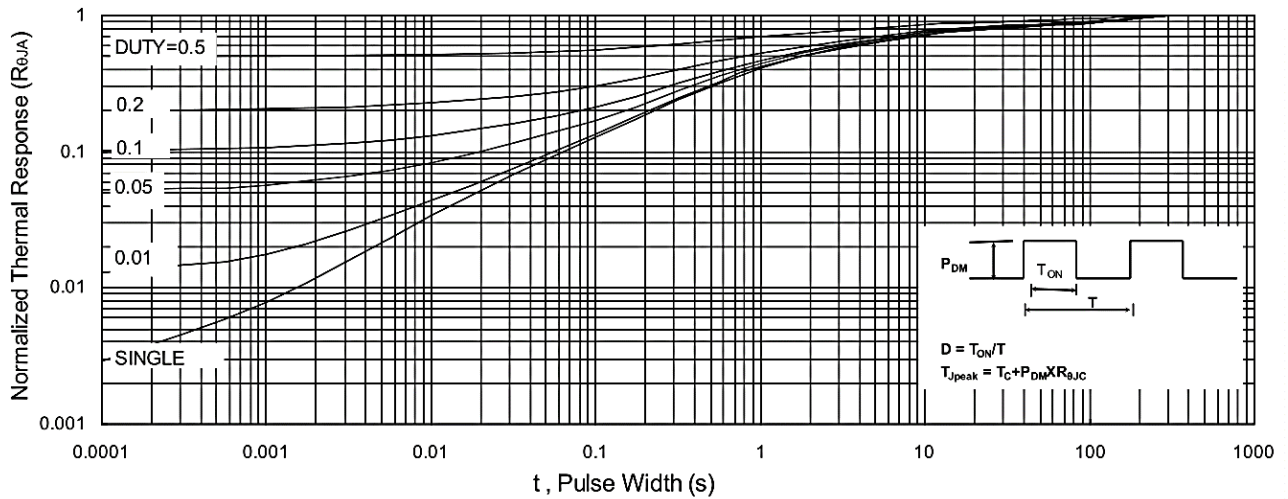


Fig.9 Normalized Maximum Transient Thermal Impedance

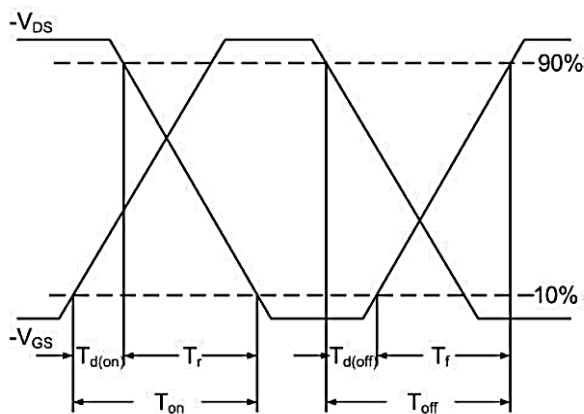


Fig.10 Switching Time Waveform

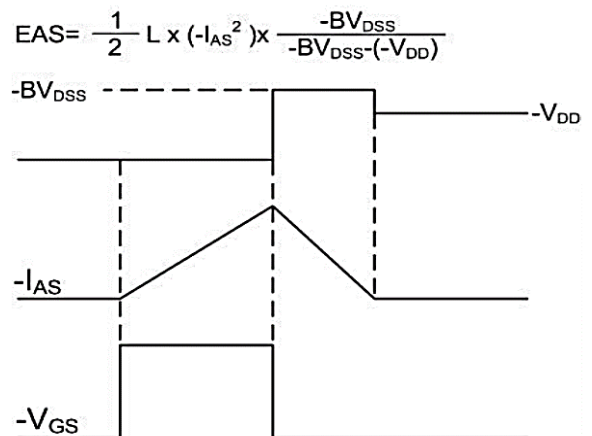
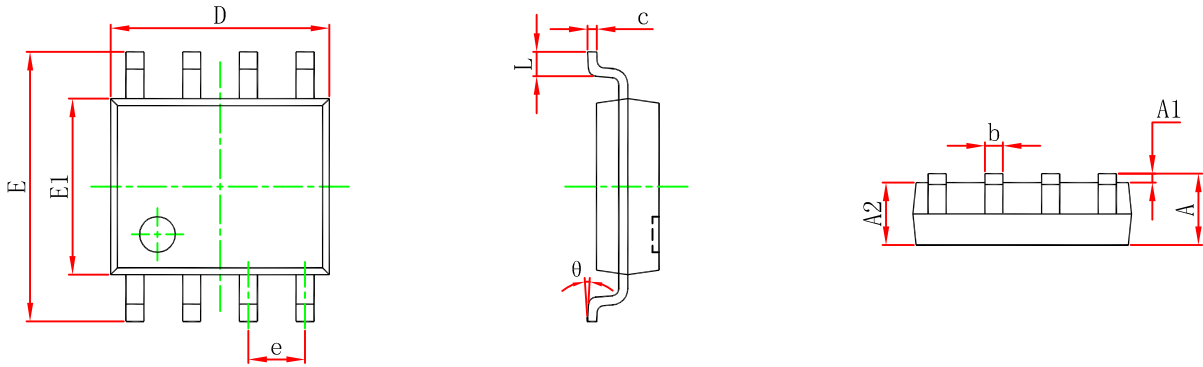


Fig.11 Unclamped Inductive Waveform

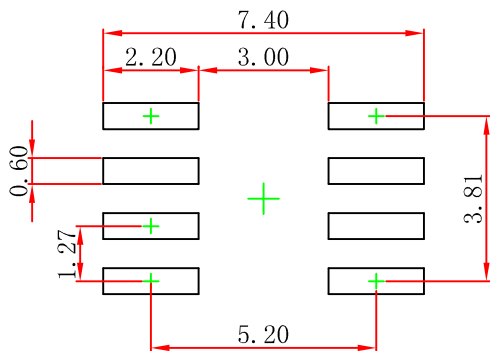
$$EAS = \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS} - (-V_{DD})}$$



SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.



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