SY56805A1

PoE Power Device

General Description

The SY56805A1 is a combined Power over Ethernet (PoE) powered device (PD) interface and primary side converter optimized specifically for isolated converter designs. The PoE interface supports the IEEE 802.3af standard as a 13W Type 1 powered device.

To achieve higher efficiency and better EMI performance, SY56805A1 drives Flyback converters in the Quasi-Resonant mode and adaptive PWM/PFM control. The flyback converter integrates a 150V, 0.14Ω MOSFET.

SY56805A1 features a detection signature pin which can also be used to disable the internal hotswap MOSFET. This allows the PoE function to be turned off during powered operation. Classification can be programmed to any of the defined Type 1 PD with a single resistor.

Features

- Power Up to 13W(input) PDs
- Supports the IEEE 802.3af Standard
- Primary Side Control
- QR-mode Operation for High Efficiency
- PWM/PFM Control for Higher Average Efficiency
- Adapter ORing Support
- 100 V, 0.45Ω Hotswap MOSFET
- Integrate 150V, 0.14Ω MOSFET for Converter
- RoHS Compliant and Halogen Free
- Compact Package: QFN5*5-32L

Applications

- IEEE 802.3af Compliant Devices
- Video and VoIP Telephones
- RFID Readers
- Multiband Access Points
- Security Cameras

Ordering Information

SY56805□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY56805A1QEC	QFN5*5-32L	----

Typical Applications

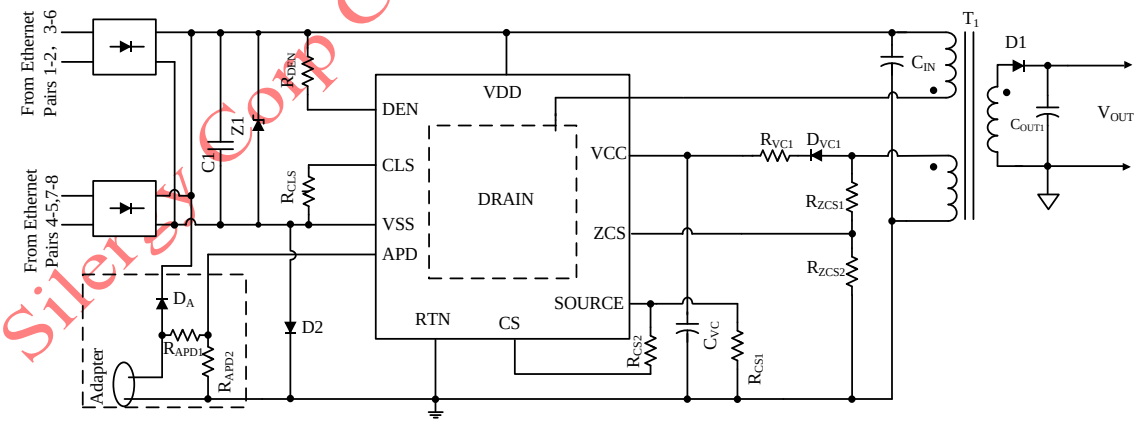
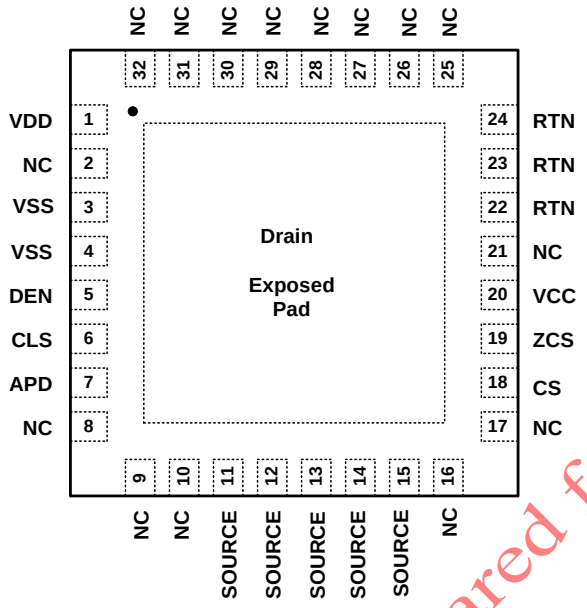


Figure 1. Schematic Diagram

Pinout (top view)

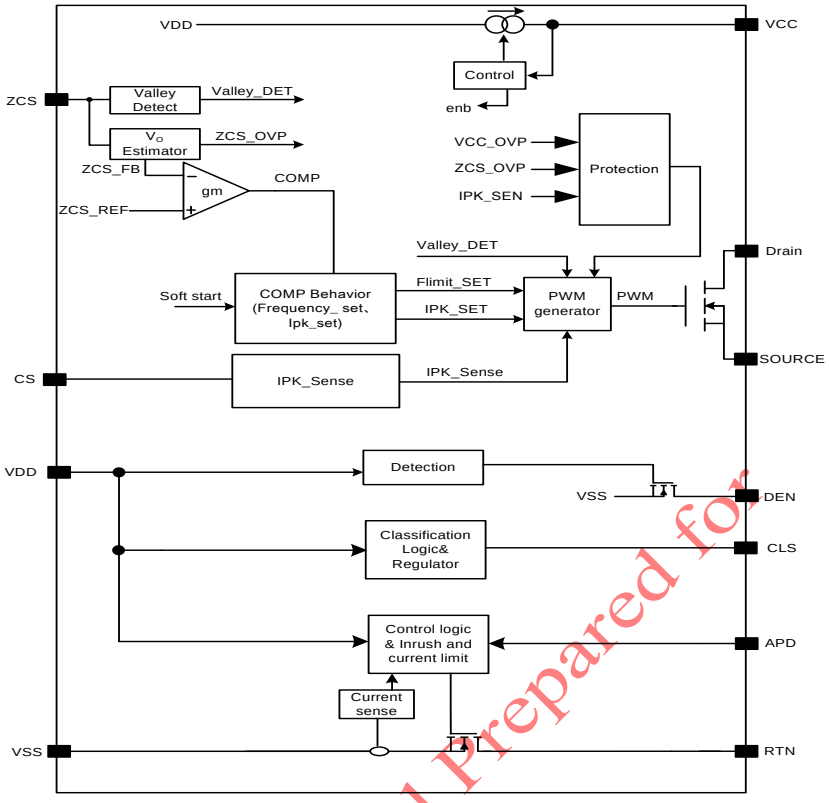


(QFN5*5-32L)

Top Mark: EBF*xyz* (device code: EBF, ***x=year code, y=week code, z= lot number code***)

Name	Pin	Description
VDD	1	Connect to the positive PoE input power rail. VDD powers the PoE interface circuits. Bypass with a 0.1 µF capacitor and protect with a TVS.
VSS	3,4	Connect to the negative power rail derived from the PoE source.
DEN	5	Connect a 24.9 kΩ resistor from DEN to VDD to provide the PoE detection signature. Pulling this pin to VSS during powered operation causes the internal hotswap MOSFET to turn off.
CLS	6	Connect a resistor from CLS to VSS to program classification current. 2.5 V is applied to the program resistor during classification to set class current.
APD	7	Pull APD above 1.5 V disables the internal hotswap switch. This forces power to come from an external VDD-RTN adapter. Connect APD to RTN when not used.
SOURCE	11,12,13,14	Source of the internal power MOSFET.
SOURCE	15	Internal connected to the source of the internal power MOSFET， this pin can be floating.
CS	18	Current sense pin.
ZCS	19	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
VCC	20	DC/DC converter bias voltage.
RTN	22,23,24	RTN is the output of the PoE hotswap MOSFET.
Drain	Exposed Pad	Drain of the internal power MOSFET.
NC	others	Not connected.

Block Diagram



Absolute Maximum Ratings (1)

Input voltage range [DEN, VDD, RTN (2)] to VSS ---------- -0.3-100V
Input voltage range [VDD, VCC] to RTN ---------- -0.3-100V
Input voltage range CLS (3) to VSS---------- -0.3- 5.5V
Input voltage range [ZCS, CS, APD] to RTN ---------- -0.3- 5.5V
Package Thermal Resistance (4)
QFN5*5-32L, θ_{JA} ---------- 25.13°C/W
QFN5*5-32L, θ_{JC} ---------- 16.85°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

Input voltage range [RTN, VDD] to VSS---------- 0- 72V
Input voltage range VDD to RTN ---------- 0- 72V
Input voltage range VCC to RTN ---------- 0- 18V
Junction Temperature Range ---------- -40°C to 125°C

Notes:

(1): Stresses beyond the “Absolute Maximum Ratings” may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2): I_{RTN}=0 for V_{RTN}>80V.

(3): Do not apply voltage to this pin.

(4): JESD 51-2，-5，-7，-8，-14 standard.

Electrical Characteristics

(Unless otherwise noted: C_{VCC}=0.1 µF, R_{DEN}=24.9 kΩ, R_{CLS} open, V_{VDD}-V_{VSS} = 48 V, 9 V ≤ VCC≤ 18 V. Typical specifications are at 25°C.)

DC-DC Controller Section

VSS=RTN, all voltages referred to RTN.

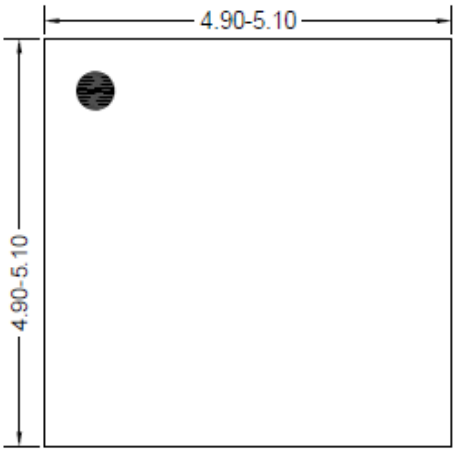
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC						
VCC Turn-on Threshold	V_{VCC_ON}		8.55	9	9.45	V
VCC UVLO Hysteresis	V_{VCC_HYS}			2.5		V
VCC SCP Threshold	V_{VCC_SCP}	V_{CC} falling	6.5	7	7.5	V
VCC OVP Voltage	V_{VCC_OVP}			22		V
Quiescent Current	I_Q		200	280	350	µA
Startup Current Source	I_{VCC}	V_{DD}=48V, V_{CC}=0V	0.5	1	2	mA
ZCS						
Voltage Reference	V_{ZCS_REF}		1.18	1.2	1.22	V
ZCS OVP Threshold	V_{ZCS_OVP}		1.35	1.45	1.55	V
Blanking Time for OFF Time	T_{OFF_MIN}		0.53	0.64	0.75	µs
CS						
Maximum Threshold Voltage	V_{LIMIT}		0.92	1.06	1.2	V
SWITCHING						
Max ON Time	T_{ON_MAX}			12		µs
Max OFF Time	T_{OFF_MAX}		400	550	700	µs
Maximum Switching Frequency	F_{MAX}		160	200	280	kHz
INTEGRATED MOSFET						
Breakdown Voltage	V_{BV}	V_{GS}=0V, I_{DS}=250µA	150			V
Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=12V, I_{DS}=0.1A		0.14		Ω
APD						
APD Threshold Voltage	V_{APD_EN}	V_{APD} rising	1.4	1.5	1.6	V
	V_{APD_H}	Hysteresis		0.3		V
APD Leakage Current		V_{APD}=5.5V			1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_J rising		150		°C
Hysteresis				20		°C

PD Interface Section

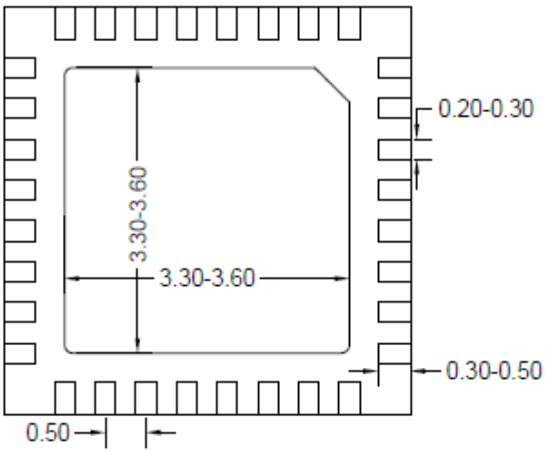
All voltages referred to VSS unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DETECTION	**DEN**	V_{VDD}= RTN=V_{SUPPLY} positive				
Detection Current		V_{VDD}=1.6V		60		μA
		V_{VDD}=10V		400		μA
Detection Bias Current		V_{VDD}=10V,float DEN, measure I_{SUPPLY}	4.5	7	10	μA
Hotswap Disable Threshold	V_{PD_DIS}		3	4	5	V
DEN Leakage Current		V_{DEN}=V_{VDD}=57V,measure I_{DEN}		0.1	5	μA
CLASSIFICATION	**CLS**	VDD= RTN=V_{SUPPLY} positive				
Classification Current	I_{CLS}	R_{CLS}=1270Ω		2		mA
		R_{CLS}=243Ω		10		mA
		R_{CLS}=137Ω		18		mA
		R_{CLS}=90.9Ω		28		mA
		R_{CLS}=63.4Ω		40		mA
Classification Regulator Lower Threshold	V_{CL_ON}	Regulator turns on, VDD rising	9	11	13	V
	V_{CL_H}	Hysteresis	1	2	3	V
Classification Regulator Upper Threshold	V_{CU_OFF}	Regulator turns off, VDD rising	21	22	23	V
	V_{CU_H}	Hysteresis	0.3	0.6	1	V
HOTSWAP MOSFET						
On Resistance				0.45	0.6	Ω
Current Limit				580		mA
Inrush Limit			50	60	85	mA
Leakage Current		V_{VDD}=V_{RTN}=100V, DEN=VSS			40	μA
UVLO						
UVLO Threshold	V_{UVLO_R}	VDD rising	34	35	36.8	V
	V_{UVLO_H}	Hysteresis		4.3		V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_J rising		150		°C
Hysteresis				20		°C

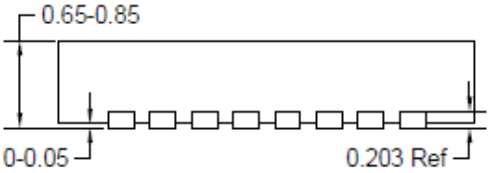
QFN5x5-32L Package Outline & PCB Layout



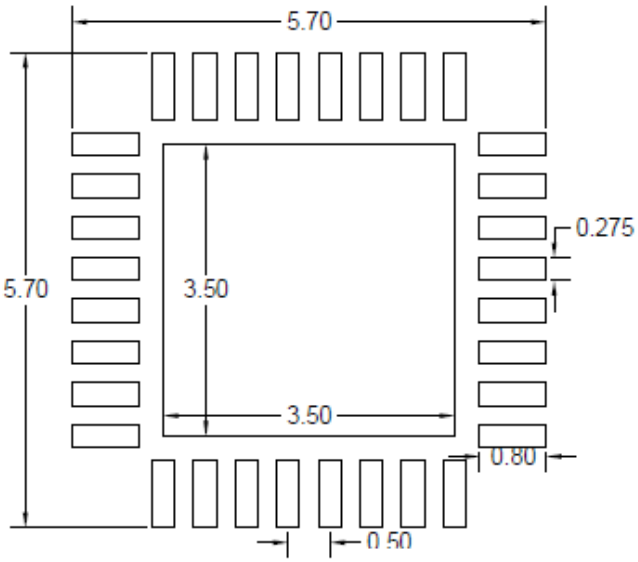
Top View



Bottom View



Side View

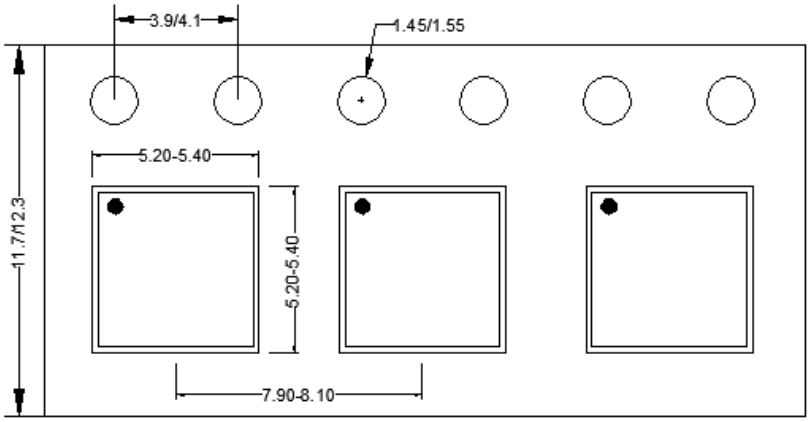


PCB layout (Recommended)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

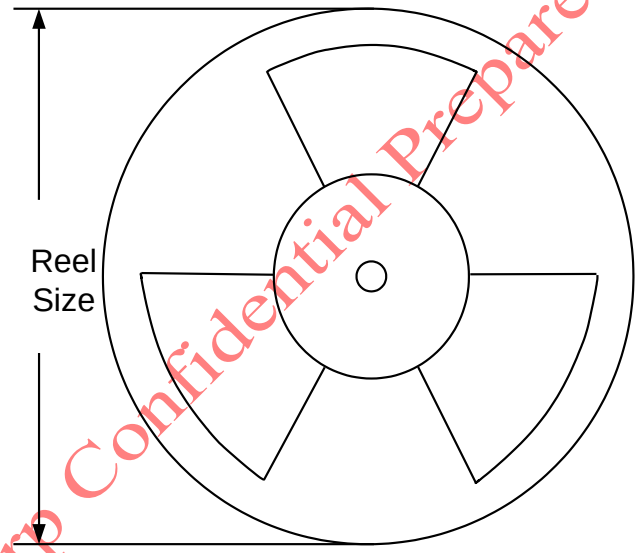
Taping & Reel Specification

1. Taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA