



OPA2211-EP 1.1-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Operational Amplifier

1 Features

- Low Voltage Noise: 1.1 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- Input Voltage Noise: 80 nV_{PP} (0.1 to 10 Hz)
- THD+N: –136 dB (G = 1, f = 1 kHz)
- Offset Voltage: 180 μV (Max)
- Offset Voltage Drift: 0.35 $\mu\text{V}/^\circ\text{C}$ (Typ)
- Low Supply Current: 3.6 mA/Ch (Typ)
- Unity-Gain Stable
- Gain Bandwidth Product:
80 MHz (G = 100)
45 MHz (G = 1)
- Slew Rate: 27 V/ μs
- 16-Bit Settling: 700 ns
- Wide Supply Range:
 $\pm 2.25\text{ V}$ to $\pm 18\text{ V}$, $+4.5\text{ V}$ to $+36\text{ V}$
- Rail-to-Rail Output
- Output Current: 30 mA
- **Supports Defense, Aerospace, and Medical Applications**
 - Controlled Baseline
 - One Assembly and Test Site
 - One Fabrication Site
 - Available in Military (-55°C to 125°C) Temperature Range ⁽¹⁾
 - Extended Product Life Cycle
 - Extended Product-Change Notification
 - Product Traceability

2 Applications

- PLL Loop Filter
- Low-Noise, Low-Power Signal Processing
- 16-Bit ADC Drivers
- DAC Output Amplifiers
- Active Filters
- Low-Noise Instrumentation Amplifiers
- Ultrasound Amplifiers
- Professional Audio Preamplifiers
- Low-Noise Frequency Synthesizers
- Infrared Detector Amplifiers
- Hydrophone Amplifiers
- Geophone Amplifiers
- Medical

(1) Additional temperature ranges available - contact factory

3 Description

The OPA2211-EP series of precision operational amplifiers achieves very-low 1.1-nV/ $\sqrt{\text{Hz}}$ noise density with a supply current of only 3.6 mA. This series also offers rail-to-rail output swing, which maximizes dynamic range.

The extremely low voltage and low current noise, high speed, and wide output swing of the OPA2211-EP series make these devices an excellent choice as a loop filter amplifier in PLL applications.

In precision data acquisition applications, the OPA2211-EP series of operational amplifiers provides 700-ns settling time to 16-bit accuracy throughout 10-V output swings. This AC performance, combined with only 125 μV of offset and 0.35 $\mu\text{V}/^\circ\text{C}$ of drift over temperature, makes the OPA2211-EP ideal for driving high-precision 16-bit analog-to-digital converters (ADCs) or buffering the output of high-resolution digital-to-analog converters (DACs).

The OPA2211-EP is specified over a wide dual-power supply range of $\pm 2.25\text{ V}$ to $\pm 18\text{ V}$, or for single-supply operation from 4.5 to 36 V.

The OPA2211-EP is available in a small DFN-8 (3-mm \times 3-mm) package. These operational amplifiers are specified from $T_J = -55^\circ\text{C}$ to 125°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2211-EP	WSON (8)	3.00 mm \times 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Voltage Noise Density vs Frequency

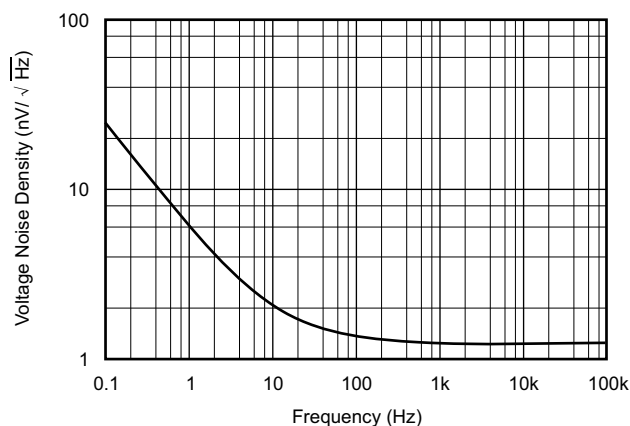


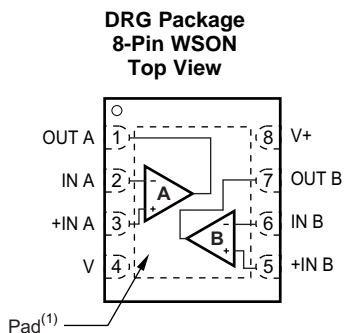
Table of Contents

1 Features	1	7.4 Device Functional Modes.....	16
2 Applications	1	8 Application and Implementation	17
3 Description	1	8.1 Application Information.....	17
4 Revision History	2	8.2 Typical Application	19
5 Pin Configuration and Functions	3	9 Power Supply Recommendations	22
6 Specifications	4	9.1 Operating Voltage	22
6.1 Absolute Maximum Ratings	4	10 Layout	22
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	22
6.3 Recommended Operating Conditions.....	4	10.2 Layout Example	23
6.4 Thermal Information	4	10.3 Thermal Considerations	23
6.5 Electrical Characteristics: $V_S = \pm 2.25$ to ± 18 V.....	5	11 Device and Documentation Support	24
6.6 Typical Characteristics	7	11.1 Community Resources.....	24
7 Detailed Description	14	11.2 Trademarks	24
7.1 Overview	14	11.3 Electrostatic Discharge Caution.....	24
7.2 Functional Block Diagram	14	11.4 Glossary	24
7.3 Feature Description.....	14	12 Mechanical, Packaging, and Orderable Information	24

4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release.

5 Pin Configuration and Functions



- (1) Exposed thermal die pad on underside; connect thermal die pad to V-. Soldering the thermal pad improves heat dissipation and provides specified performance

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input for channel A
–IN A	2	I	Inverting input for channel A
+IN B	5	I	Noninverting input for channel B
–IN B	6	I	Inverting input for channel B
OUT A	1	O	Output terminal for channel A
OUT B	7	O	Output terminal for channel B
V+	8	—	Positive supply voltage
V–	4	—	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	$V_S = (V+) - (V-)$		40	V
Input voltage		$(V-) - 0.5$	$(V+) + 0.5$	V
Input current (any pin except power-supply pins)		-10	10	mA
Output short-circuit ⁽²⁾		Continuous		
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to $V_S / 2$ (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage ($V+ - V-$)	4.5 (±2.25)		36 (±18)	V
Operating temperature, T_J	-55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA2211-EP	UNIT
		DRG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics: $V_S = \pm 2.25$ to ± 18 V

at $T_J = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V _{OS}	V _S = ±15 V		±50	±175	μV
Over temperature		T _J = −55°C to 125°C			±350	μV
Drift	dV _{OS} /dT	T _J = −55°C to 125°C		0.35		μV/°C
vs power supply	PSRR	V _S = ±2.25 V to ±18 V		0.1	1	μV/V
Over temperature					3	μV/V
INPUT BIAS CURRENT						
Input bias current	I _B	V _{CM} = 0 V, T _J = −55°C to 125°C		±50	±350	nA
Offset current	I _{OS}	V _{CM} = 0 V, T _J = −55°C to 125°C		±20	±200	nA
NOISE						
Input voltage noise	e _n	f = 0.1 Hz to 10 Hz		80		nV _{PP}
Input voltage noise density		f = 10 Hz		2		nV/√Hz
		f = 100 Hz		1.4		nV/√Hz
		f = 1 kHz		1.1		nV/√Hz
Input current noise density	I _n	f = 10 Hz		3.2		pA/√Hz
		f = 1 kHz		1.7		pA/√Hz
INPUT VOLTAGE RANGE						
Common-mode voltage range	V _{CM}	V _S ≥ ±5 V	(V−) + 1.8		(V+) − 1.4	V
		V _S < ±5 V	(V−) + 2		(V+) − 1.4	V
Common-mode rejection ratio	CMRR	V _S ≥ ±5V, (V−) + 2V ≤ V _{CM} ≤ (V+) − 2V, T _J = −55°C to 125°C	114	120		dB
		V _S < ±5V, (V−) + 2V ≤ V _{CM} ≤ (V+) − 2V, T _J = −55°C to 125°C	106	120		dB
INPUT IMPEDANCE						
Differential				20k 8		Ω pF
Common-mode				10 ⁹ 2		Ω pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A _{OL}	(V−) + 0.2 V ≤ V _O ≤ (V+) − 0.2V, R _L = 10 kΩ, T _J = −55°C to 125°C	114	130		dB
		(V−) + 0.6 V ≤ V _O ≤ (V+) − 0.6 V, R _L = 600 Ω	110	114		dB
Over temperature	A _{OL}	(V−) + 0.6 V ≤ V _O ≤ (V+) − 0.6V, I _O ≤ 15 mA, T _J = −55°C to 125°C	100			dB
FREQUENCY RESPONSE						
Gain-bandwidth product	GBW	G = 100		80		MHz
		G = 1		45		MHz
Slew rate	SR			27		V/μs
Settling time, 0.01%	t _s	V _S = ±15 V, G = −1, 10-V step, C _L = 100 pF		400		ns
0.0015% (16-bit)		V _S = ±15 V, G = −1, 10-V step, C _L = 100 pF		700		ns
Overload recovery time		G = −10		500		ns
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V _O = 3V _{RMS} , R _L = 600 Ω		0.000015 %		
				−136		dB

Electrical Characteristics: $V_S = \pm 2.25$ to ± 18 V (continued)

at $T_J = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage output	V _{OUT}	R _L = 10 kΩ, A _{OL} ≥ 114 dB, T _J = –55°C to 125°C	(V–) + 0.2		(V+) – 0.2	V
		R _L = 600 Ω, A _{OL} ≥ 110 dB	(V–) + 0.6		(V+) – 0.6	V
		I _O < 15 mA, A _{OL} ≥ 100 dB, T _J = –55°C to 125°C	(V–) + 0.6		(V+) – 0.6	V
Short-circuit current	I _{SC}		+30/–45			mA
Capacitive load drive	C _{LOAD}		See Typical Characteristics			pF
Open-loop output impedance	Z _O	f = 1MHz	5			Ω
POWER SUPPLY						
Specified voltage	V _S		±2.25		±18	V
Quiescent current (per channel)	I _Q	I _{OUT} = 0 A	3.6		4.5	mA
Over temperature		T _J = –55°C to 125°C	6			mA
TEMPERATURE RANGE						
Operating range		T _J	–55		125	°C

6.6 Typical Characteristics

At $T_J = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

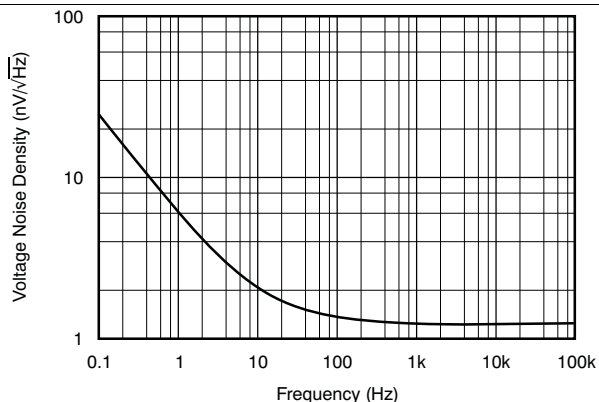


Figure 1. Input Voltage Noise Density vs Frequency

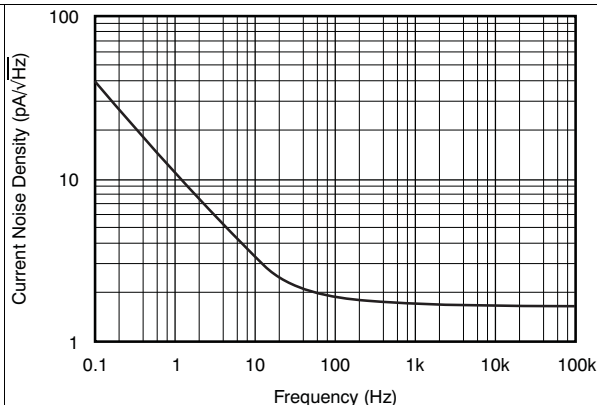


Figure 2. Input Current Noise Density vs Frequency

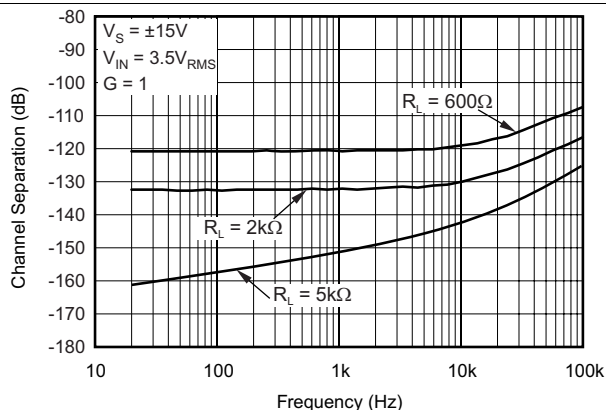


Figure 3. Channel Separation vs Frequency

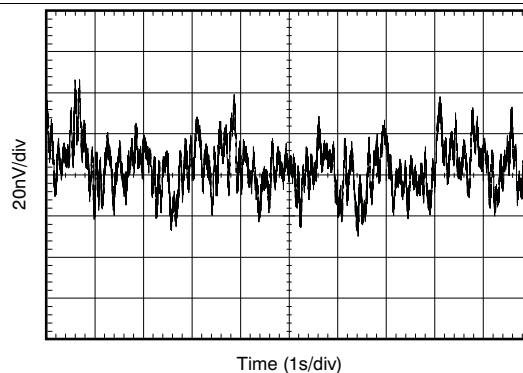


Figure 4. 0.1-Hz to 10-Hz Noise

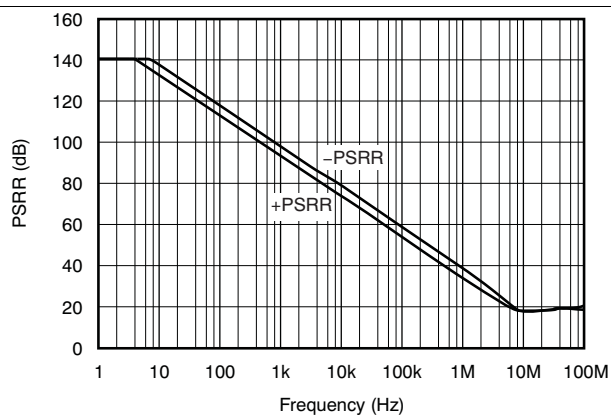


Figure 5. Power-Supply Rejection Ratio vs Frequency (Referred to Input)

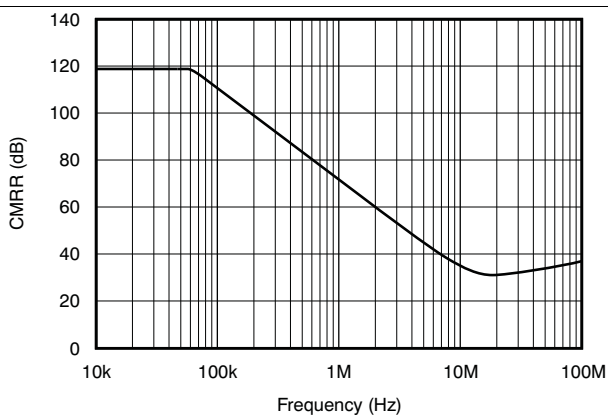


Figure 6. Common-Mode Rejection Ratio vs Frequency

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

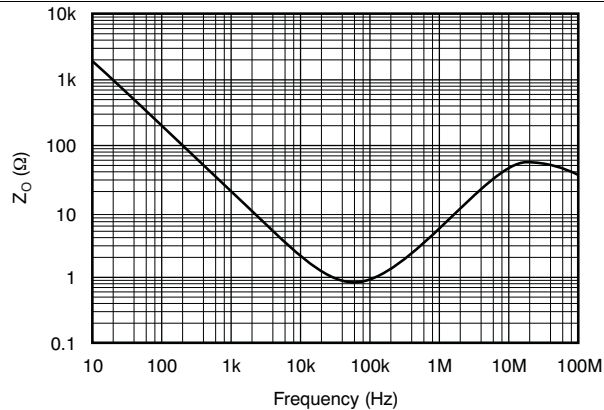


Figure 7. Open-Loop Output Impedance vs Frequency

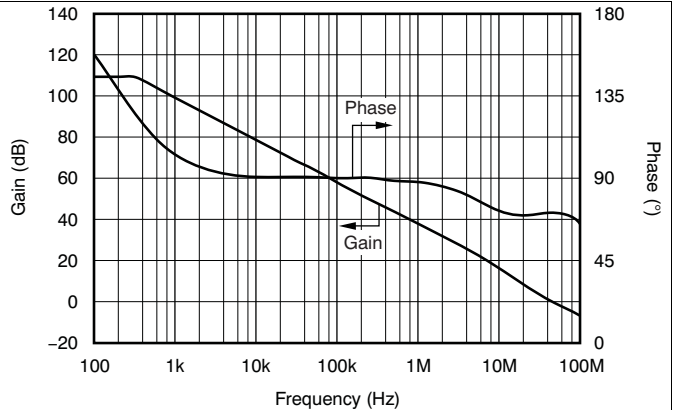


Figure 8. Gain and Phase vs Frequency

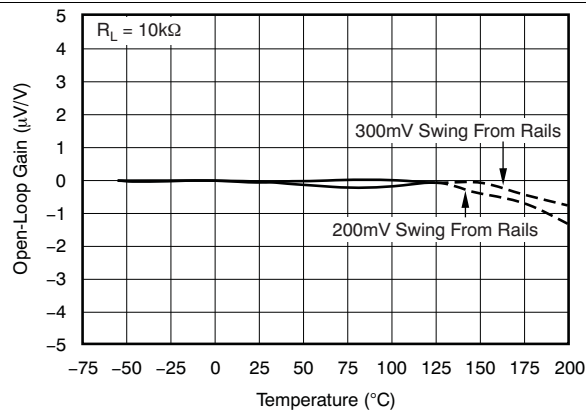


Figure 9. Normalized Open-Loop Gain vs Temperature

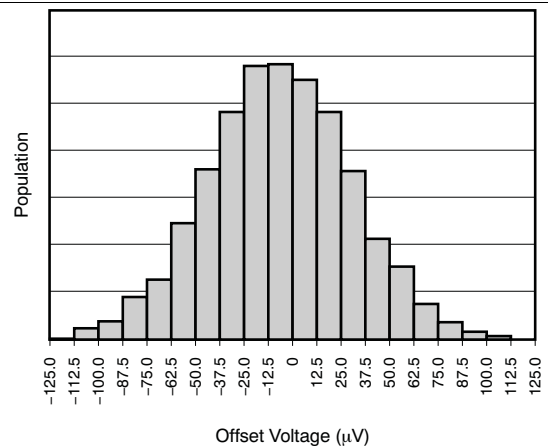


Figure 10. Offset Voltage Production Distribution

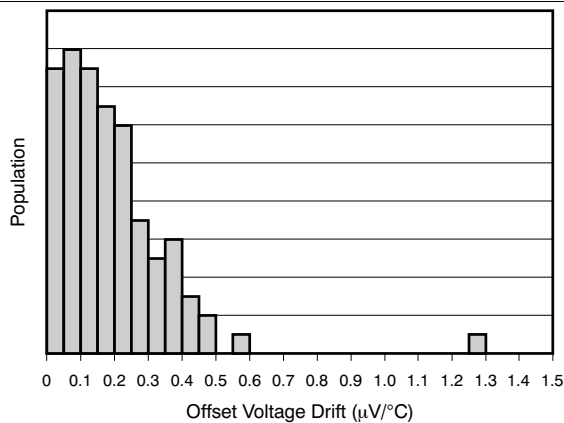


Figure 11. Offset Voltage Drift Production Distribution

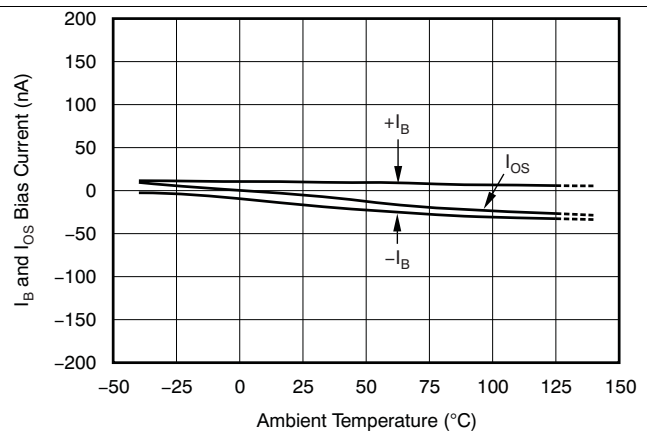


Figure 12. I_B and I_{OS} Current vs Temperature

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

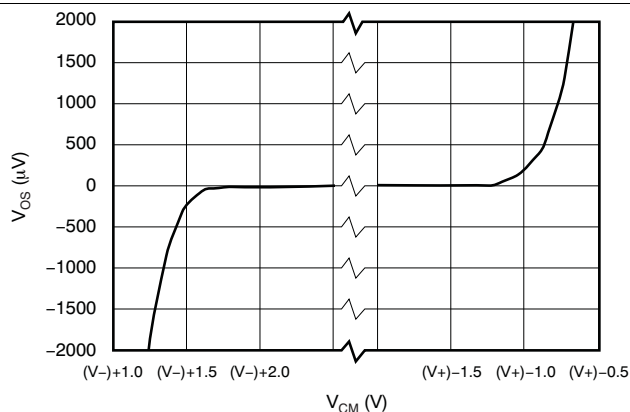


Figure 13. Offset Voltage vs Common-Mode Voltage

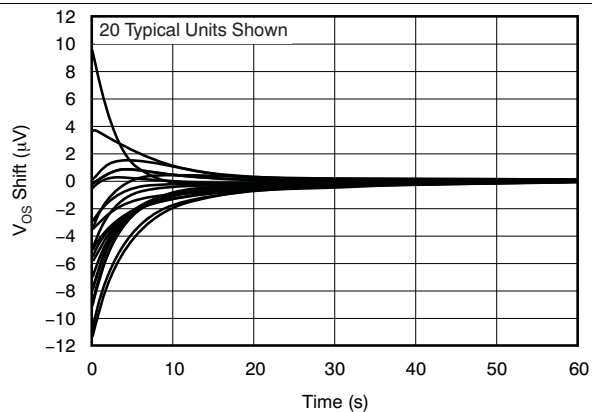


Figure 14. V_{OS} Warmup

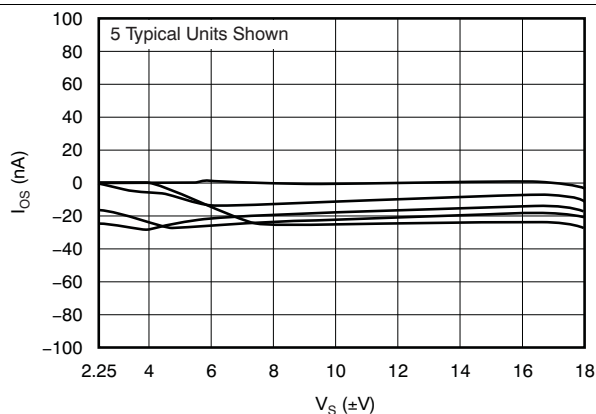


Figure 15. Input Offset Current vs Supply Voltage

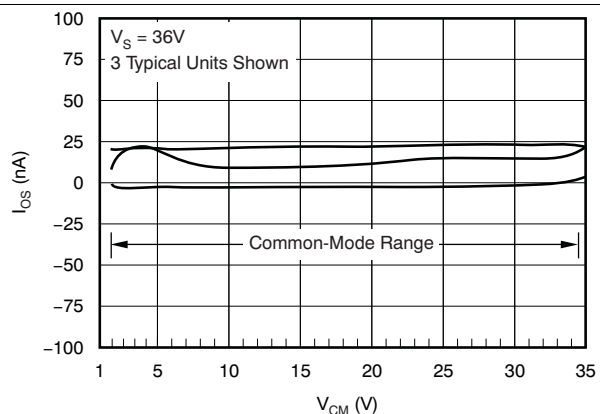


Figure 16. Input Offset Current vs Common-Mode Voltage

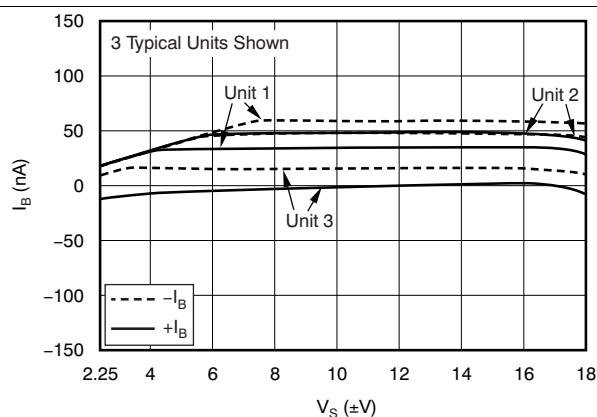


Figure 17. Input Bias Current vs Supply Voltage

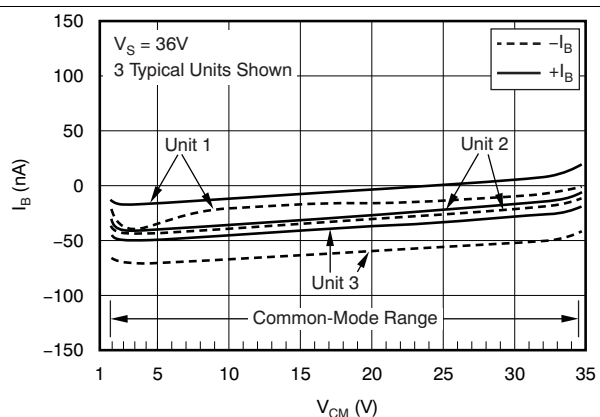


Figure 18. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

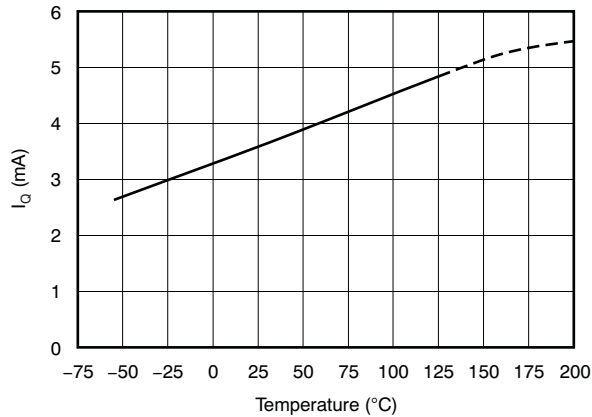


Figure 19. Quiescent Current vs Temperature

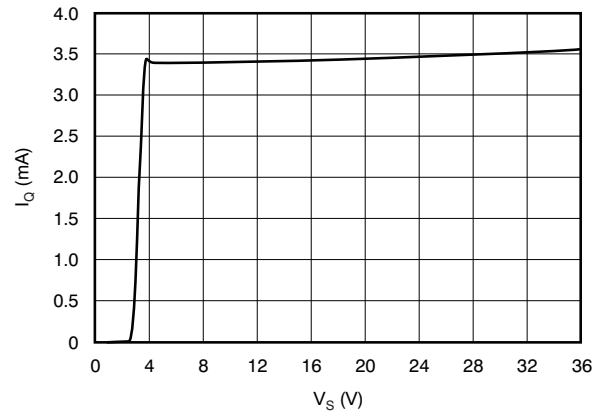


Figure 20. Quiescent Current vs Supply Voltage

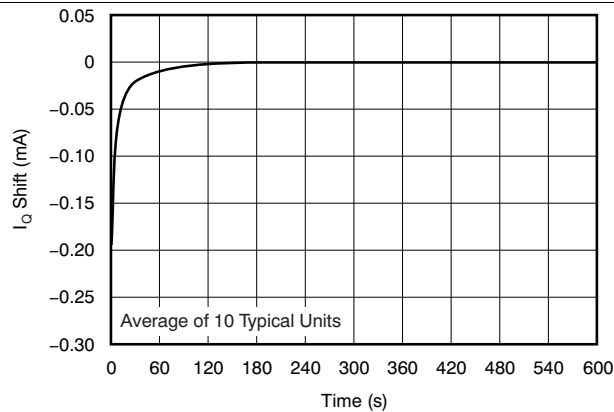


Figure 21. Normalized Quiescent Current vs Time

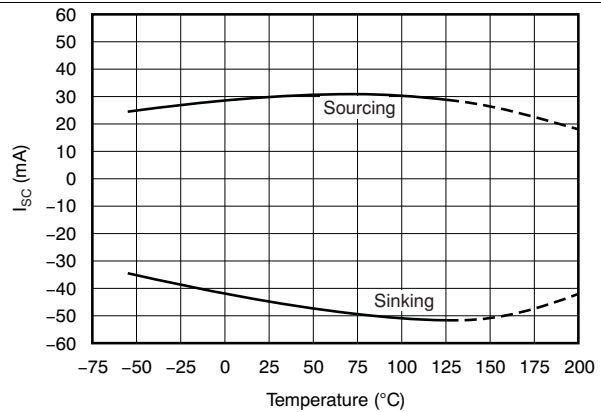


Figure 22. Short-Circuit Current vs Temperature

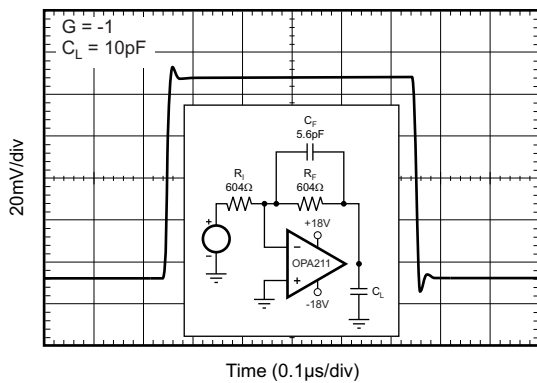


Figure 23. Small-Signal Step Response (100 mV)

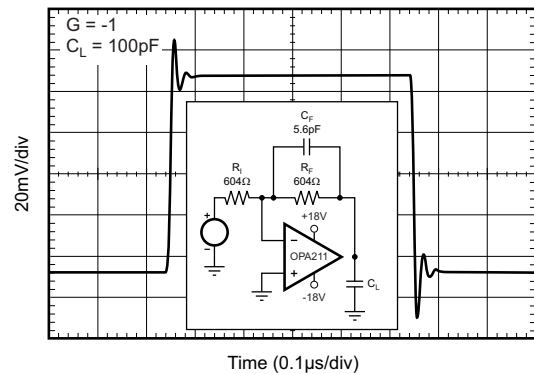


Figure 24. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

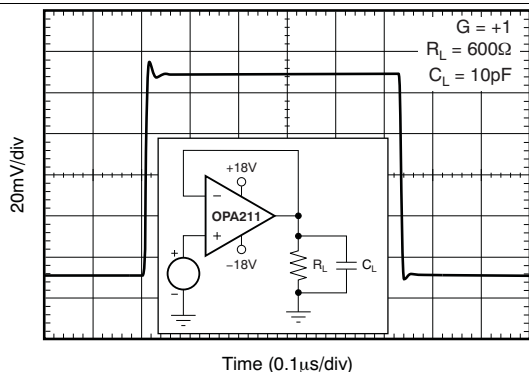


Figure 25. Small-Signal Step Response (100 mV)

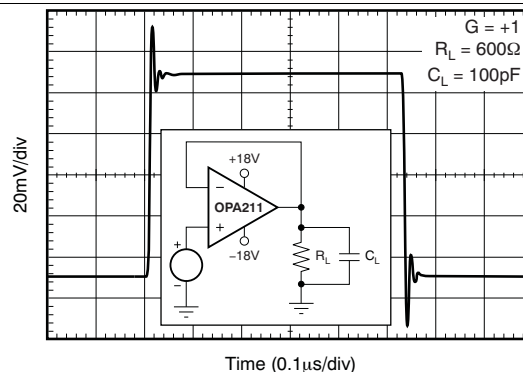


Figure 26. Small-Signal Step Response (100 mV)

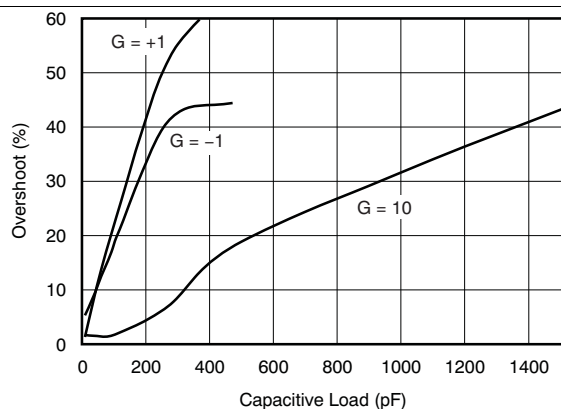


Figure 27. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

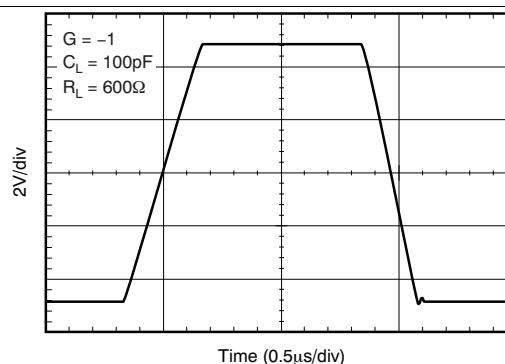


Figure 28. Large-Signal Step Response

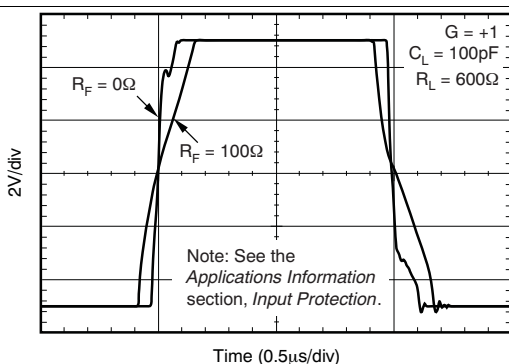


Figure 29. Large-Signal Step Response

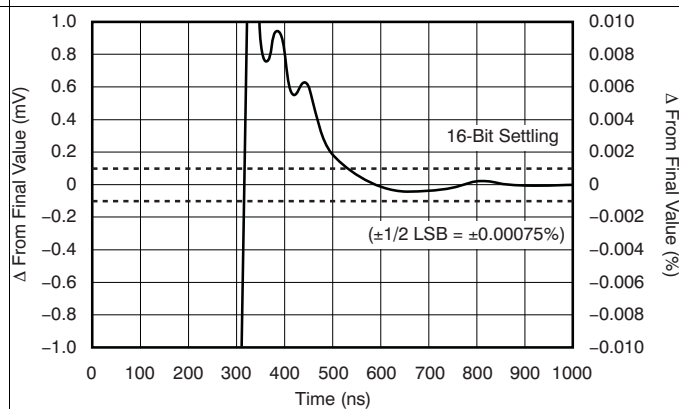


Figure 30. Large-Signal Positive Settling Time (10 V_{PP}, C_L = 100 pF)

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

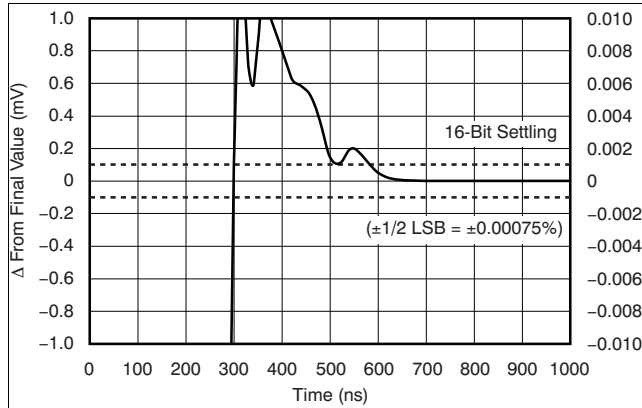


Figure 31. Large-Signal Positive Settling Time (10 V_{PP} , $C_L = 10\text{ pF}$)

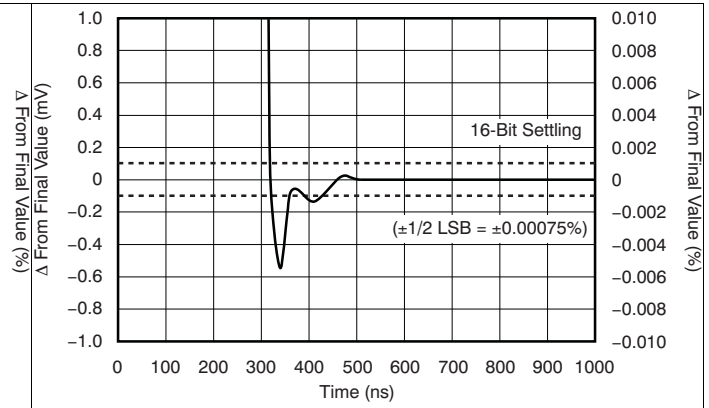


Figure 32. Large-Signal Negative Settling Time (10 V_{PP} , $C_L = 100\text{ pF}$)

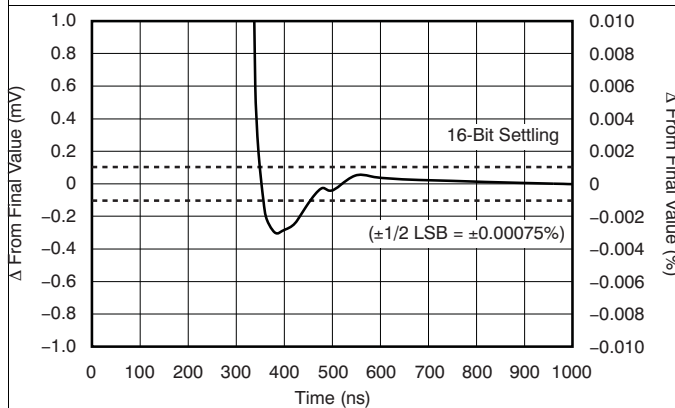


Figure 33. Large-Signal Negative Settling Time (10 V_{PP} , $C_L = 10\text{ pF}$)

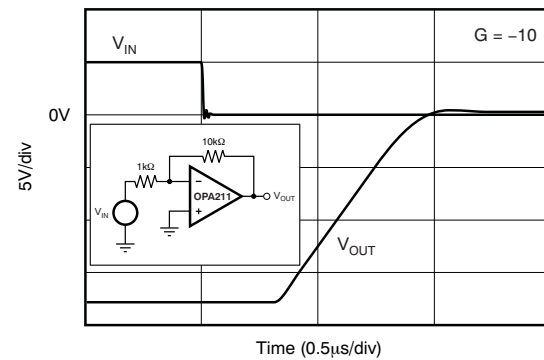


Figure 34. Negative Overload Recovery

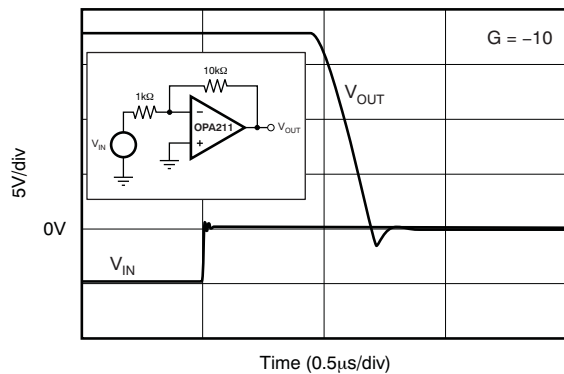


Figure 35. Positive Overload Recovery

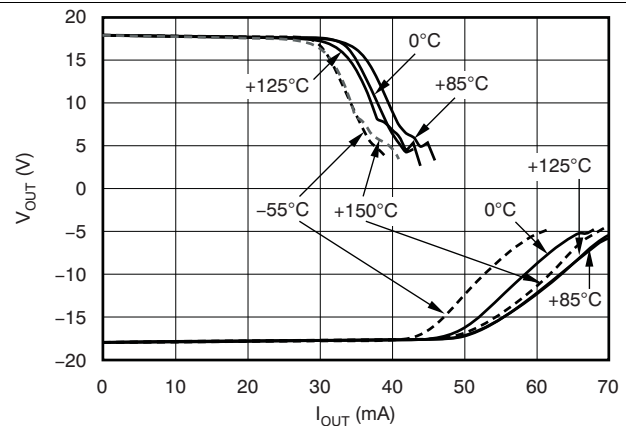


Figure 36. Output Voltage vs Output Current

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

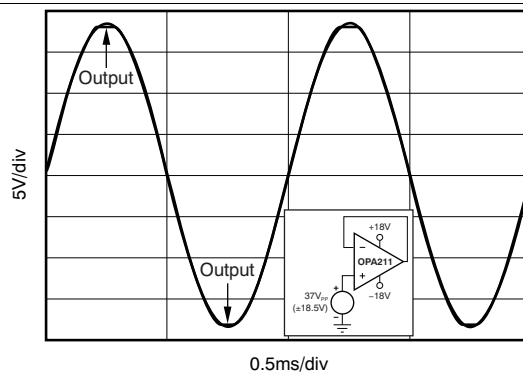


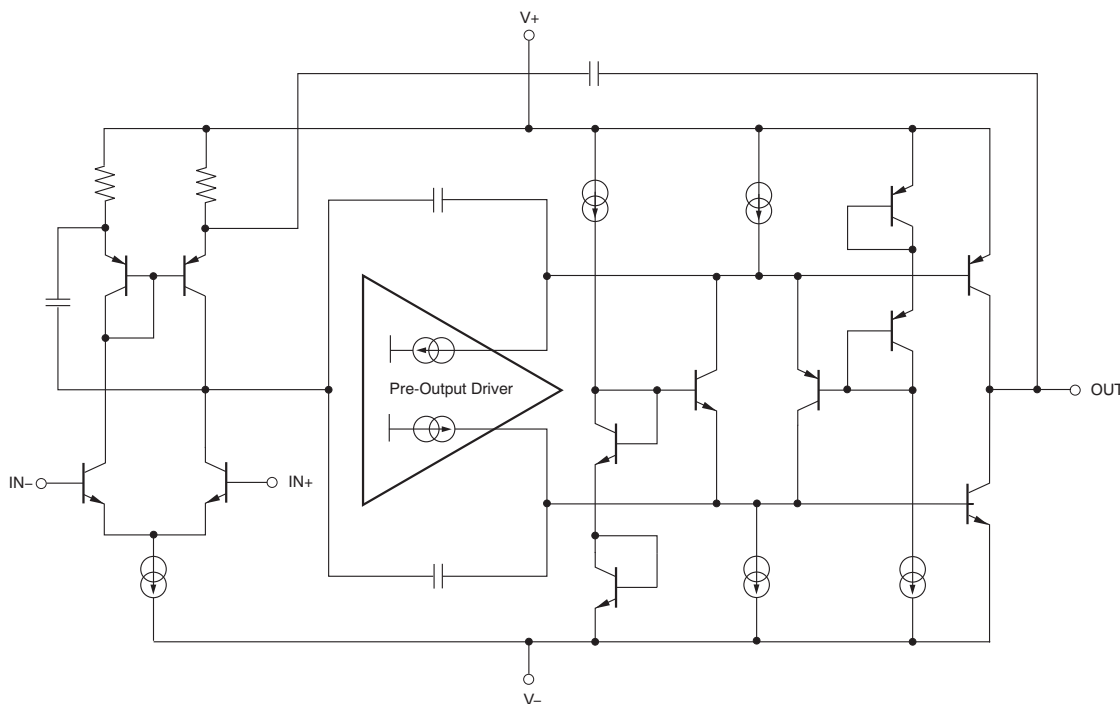
Figure 37. No Phase Reversal

7 Detailed Description

7.1 Overview

The OPA2211-EP is a unity-gain stable, precision operational amplifier with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- μ F capacitors are adequate. [Functional Block Diagram](#) shows a simplified schematic of the OPA2211-EP. This die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection

The input terminals of the OPA2211-EP [Figure 38](#) are protected from excessive differential voltage with back-to-back diodes, as shown in . In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or $G = 1$ circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in [Figure 29](#) in the [Typical Characteristics](#). If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA2211-EP, and is discussed in [Noise Performance](#). [Figure 38](#) shows an example implementing a current-limiting feedback resistor.

Feature Description (continued)

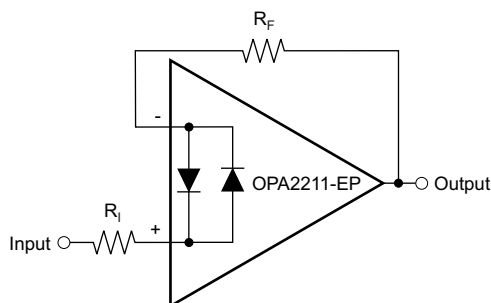


Figure 38. Pulsed Operation

7.3.2 Noise Performance

Figure 39 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA2211-EP has very low voltage noise, making it ideal for low source impedances (<2 kΩ). A similar precision operational amplifier, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 kΩ to 100 kΩ). Above 100 kΩ, a FET-input operational amplifier such as the OPA132 (very-low current noise) may provide improved performance. The equation in Figure 39 is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K, and T is temperature in K.

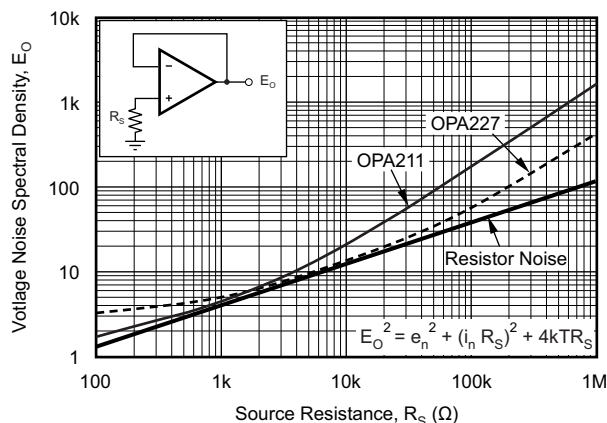


Figure 39. Noise Performance of the OPA2211-EP and OPA227 in Unity-Gain Buffer Configuration

7.3.3 Basic Noise Calculations

Design of low-noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 39. The source impedance is usually fixed; consequently, select the operational amplifier and the feedback resistors to minimize the respective contributions to the total noise.

Feature Description (continued)

[Figure 39](#) depicts total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

[Figure 41](#) shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

7.3.4 Total Harmonic Distortion Measurements

OPA2211-EP series operational amplifiers have excellent distortion characteristics. THD + Noise is below 0.0002% ($G = +1$, $V_{OUT} = 3 V_{RMS}$) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600- Ω load.

The distortion produced by OPA2211-EP series operational amplifiers is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in [Figure 42](#) can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. [Figure 42](#) shows a circuit that causes the operational amplifier distortion to be 101 times greater than that normally produced by the operational amplifier. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3 . The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

7.4 Device Functional Modes

The OPAx211 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (± 2.25 V). The maximum power supply voltage for the OPAx211 is 36 V (± 18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

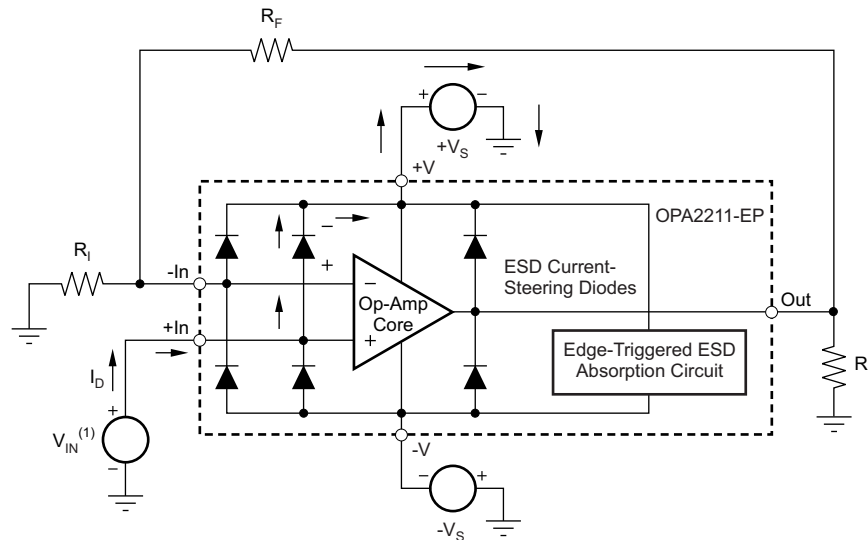
It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. [Figure 40](#) illustrates the ESD circuits contained in the OPA2211-EP (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2211-EP but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in [Figure 40](#), the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Application Information (continued)



(1) $V_{IN} = +V_S + 500 \text{ mV}$

Figure 40. Equivalent Internal ESD Circuitry and its Relation to a Typical Circuit Application

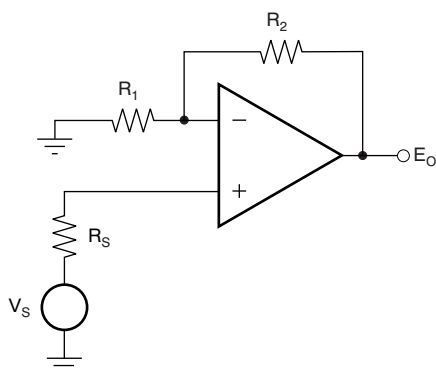
Figure 40 depicts a specific example where the input voltage, V_{IN} , exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $-V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $-V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

8.2 Typical Application

Noise in Noninverting Gain Configuration



Noise at the output:

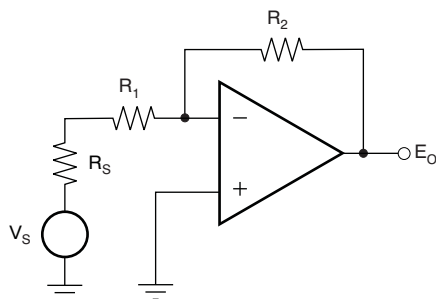
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

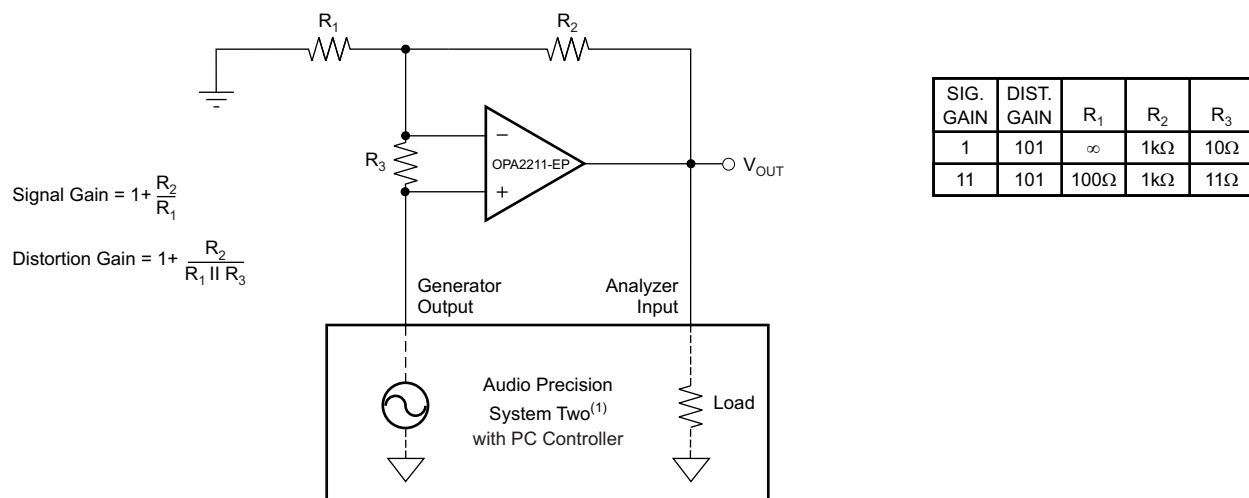
Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA211 series op amps at 1kHz, $e_n = 1.1\text{nV}/\sqrt{\text{Hz}}$ and $i_n = 1.7\text{pA}/\sqrt{\text{Hz}}$.

Figure 41. Noise Calculation in Gain Configurations



(1) For measurement bandwidth, see [Figure 43](#), [Figure 44](#), and [Figure 45](#).

Figure 42. Distortion Test Circuit

Typical Application (continued)

8.2.1 Design Requirements

The design requirements for Signal Gain = 11 are:

$$\text{Signal Gain} = 1 + \frac{R_2}{R_1}$$

where

- Supply voltage: 30 V (± 15 V)
- $R_1 = 100 \, \Omega$
- $R_2 = 1 \, \text{k}\Omega$
- $R_3 = 11 \, \Omega$

(1)

8.2.2 Detailed Design Procedure

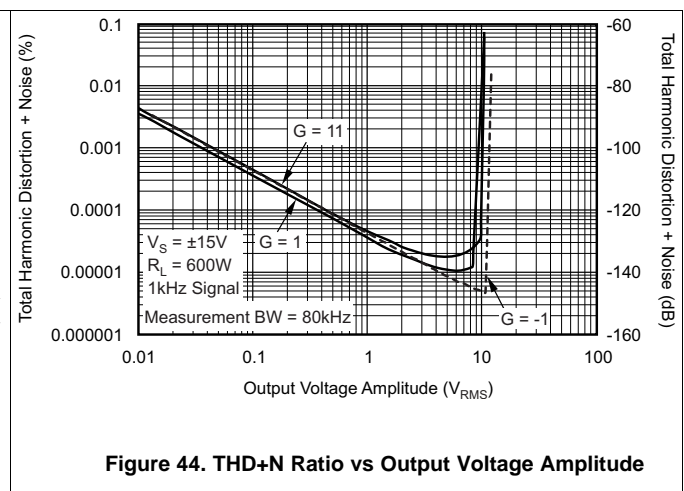
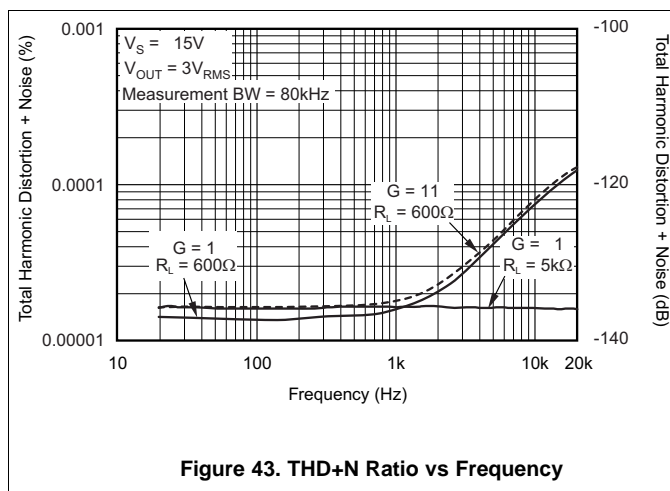
8.2.2.1 Total Harmonic Distortion Measurements

OPA2211-EP series operational amplifiers have excellent distortion characteristics. THD + Noise is below 0.0002% ($G = +1$, $V_{OUT} = 3V_{RMS}$) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600- Ω load. The distortion produced by OPA2211-EP series operational amplifiers is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in Figure 47 can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. Figure 47 shows a circuit that causes the operational amplifier distortion to be 101 times greater than that normally produced by the operational amplifier. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3 . The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

8.2.3 Application Curves



Typical Application (continued)

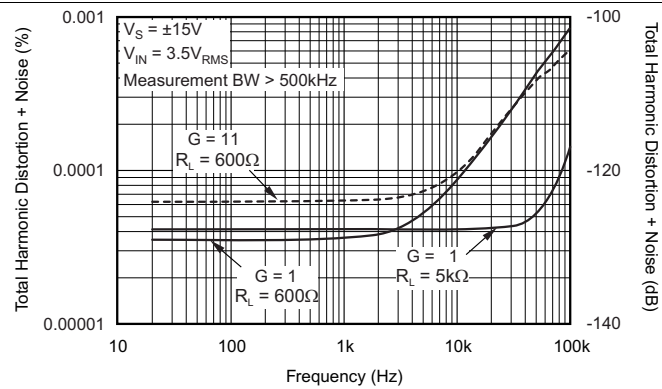


Figure 45. THD+N Ratio vs Frequency

9 Power Supply Recommendations

9.1 Operating Voltage

OPA2211-EP series operational amplifiers operate from ± 2.25 -V to ± 18 -V supplies while maintaining excellent performance. The OPA2211-EP series can operate with as little as +4.5 V between the supplies and with up to +36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA2211-EP series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25 V with the negative supply at –5 V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, $T_A = -55^{\circ}\text{C}$ to 125°C . Parameters that vary significantly with operating voltage or temperature are shown in [Typical Characteristics](#).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, [SLOA089](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 46](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

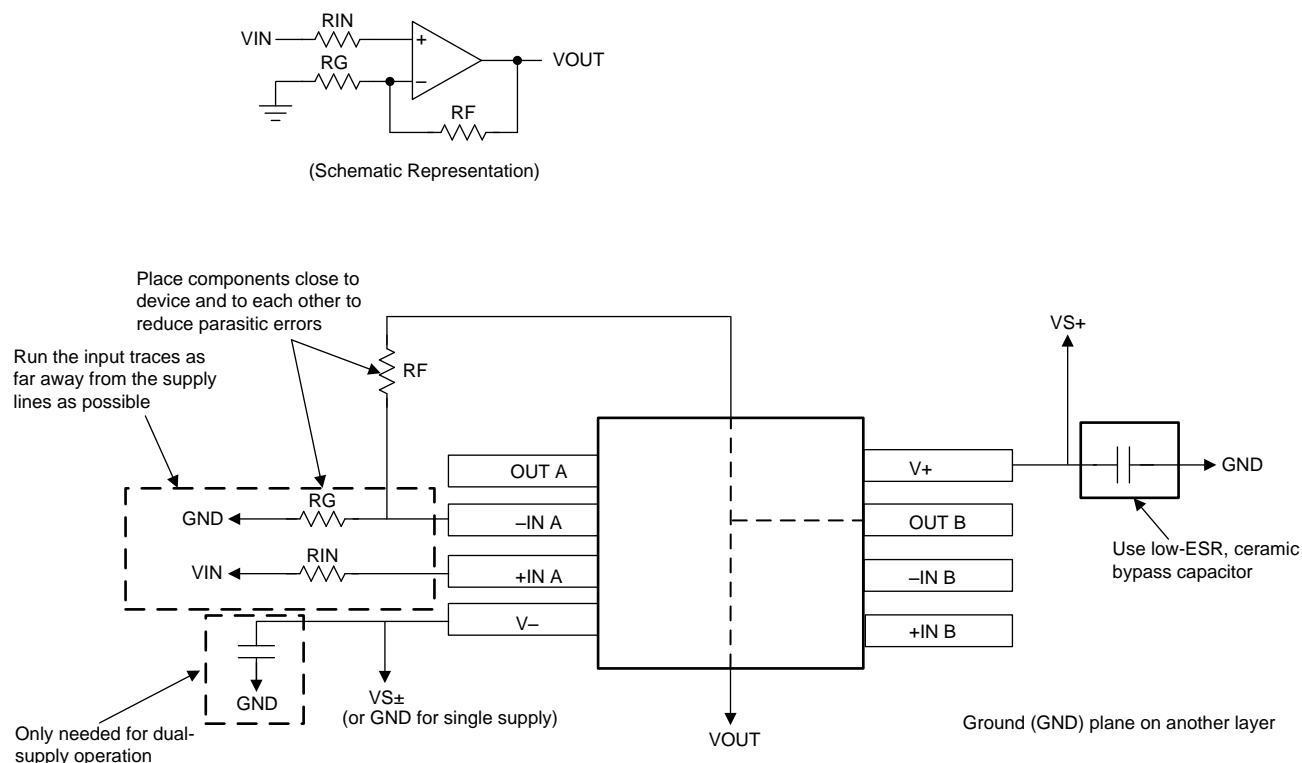


Figure 46. Operational Amplifier Board Layout for Noninverting Configuration

10.3 Thermal Considerations

The primary issue with all semiconductor devices is junction temperature (T_J). The most obvious consideration is assuring that T_J never exceeds the absolute maximum rating specified for the device. However, addressing device thermal dissipation has benefits beyond protecting the device from damage. Even modest increases in junction temperature can decrease operational amplifier performance, and temperature-related errors can accumulate. Understanding the power generated by the device within the specific application and assessing the thermal effects on the error tolerance lead to a better understanding of system performance and thermal dissipation needs.

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2211MDRGTEP	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OCQM	Samples
V62/15606-01XE	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OCQM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

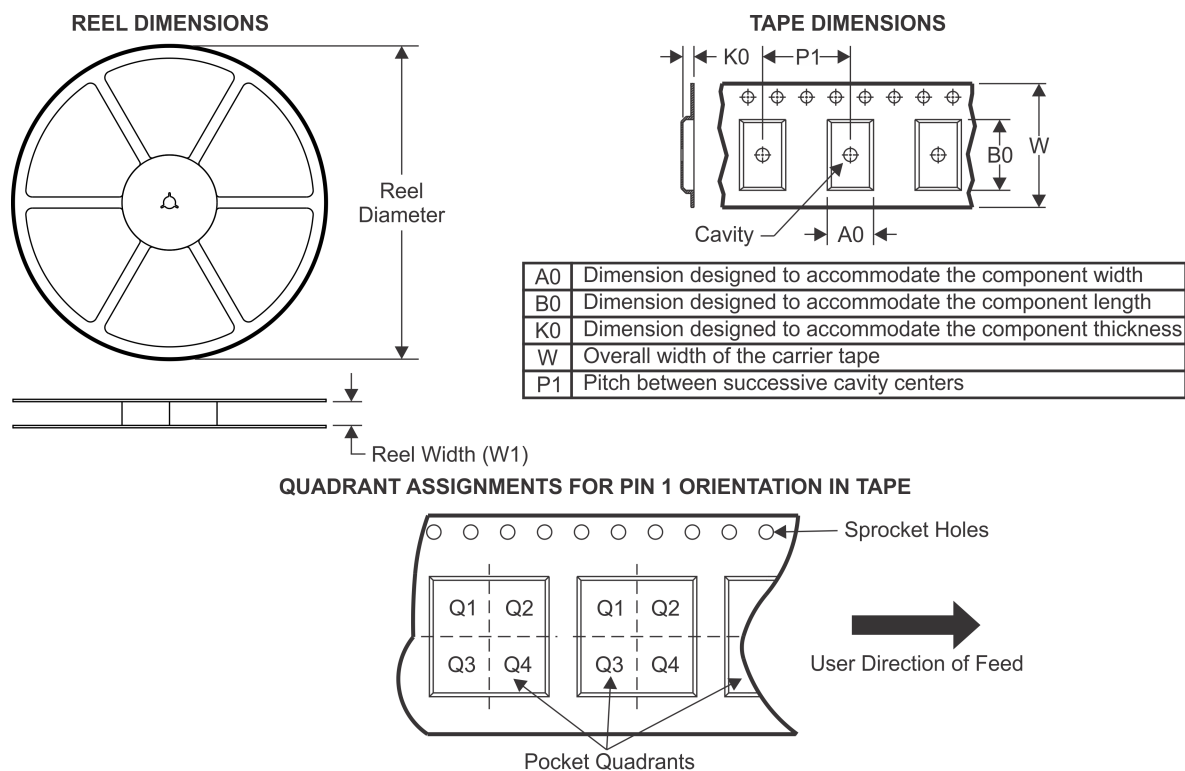
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2211-EP :

NOTE: Qualified Version Definitions:

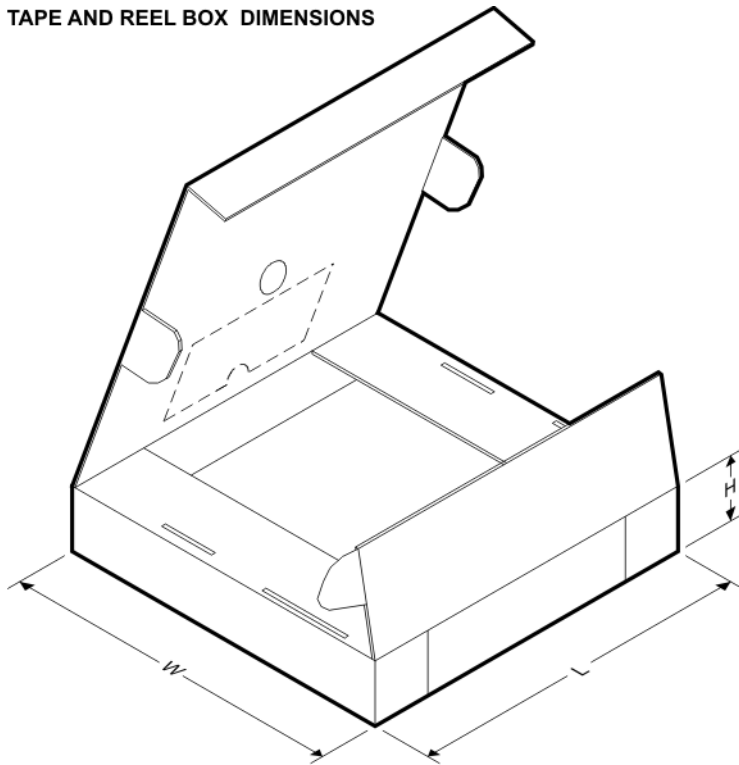
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2211MDRGTEP	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

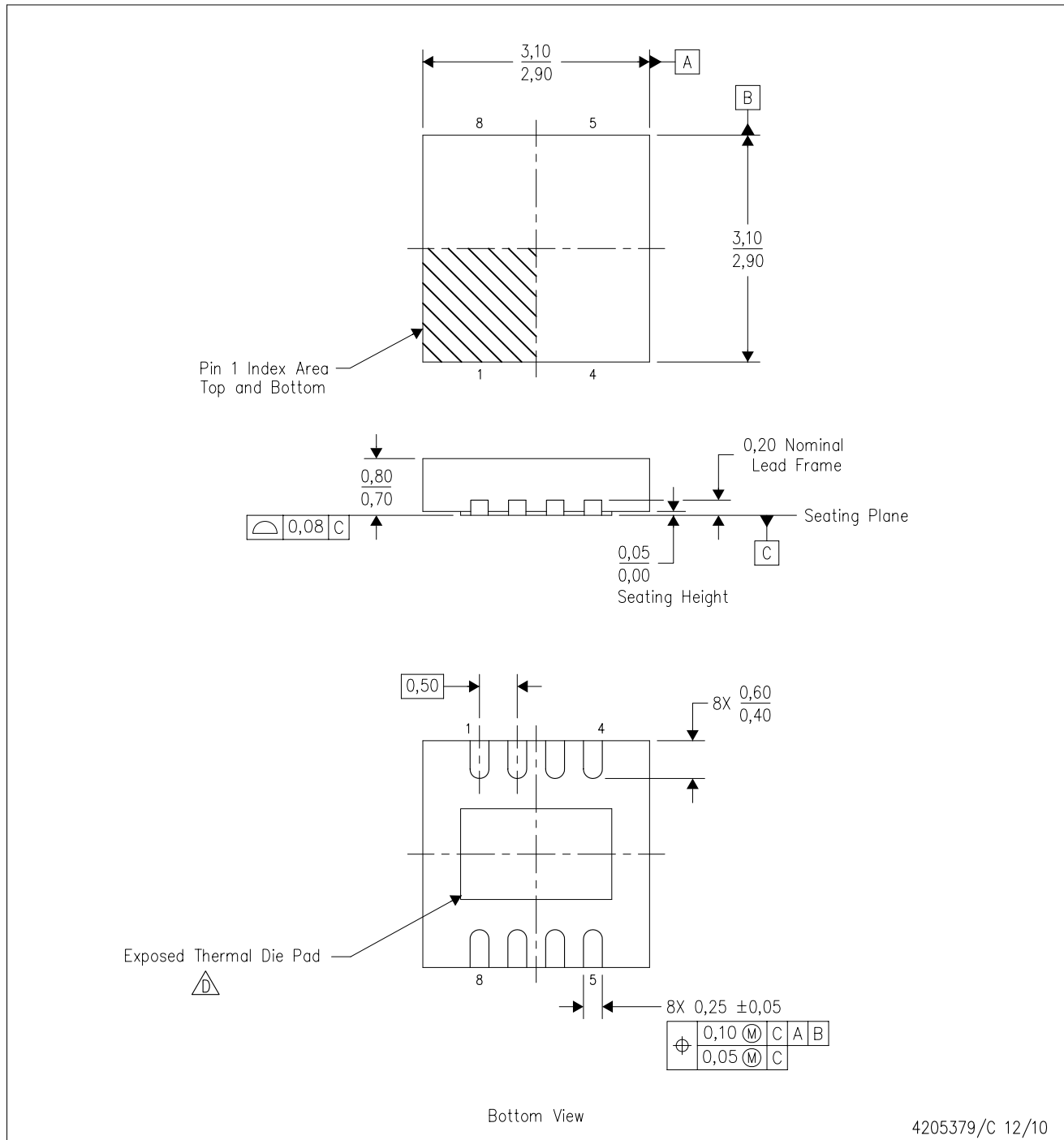


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2211MDRGTEP	SON	DRG	8	250	210.0	185.0	35.0

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. JEDEC MO-229 package registration pending.

DRG (S-PWSON-N8)

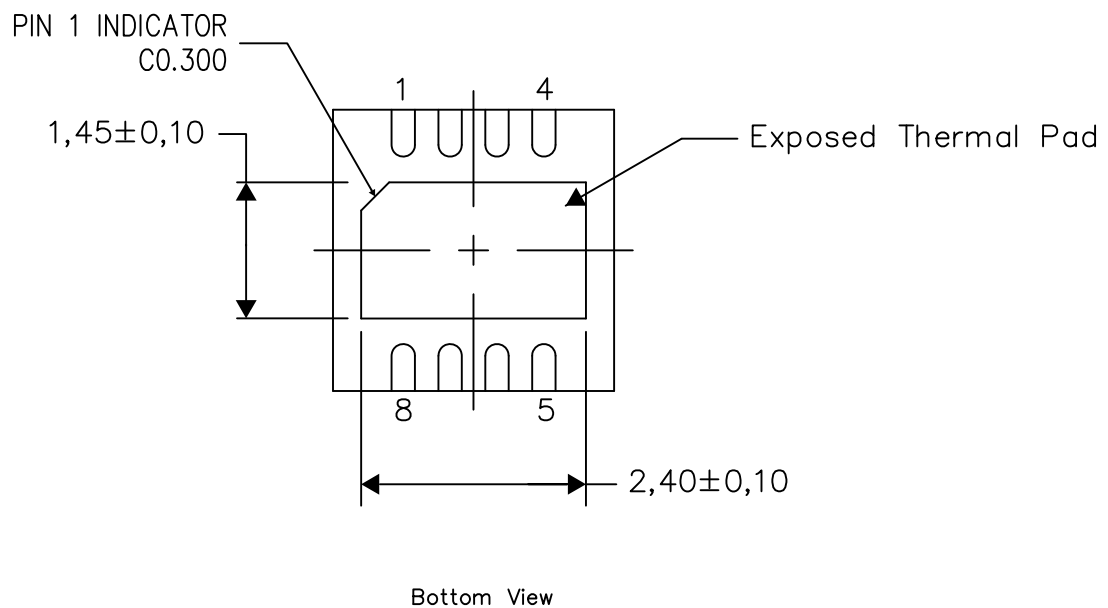
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



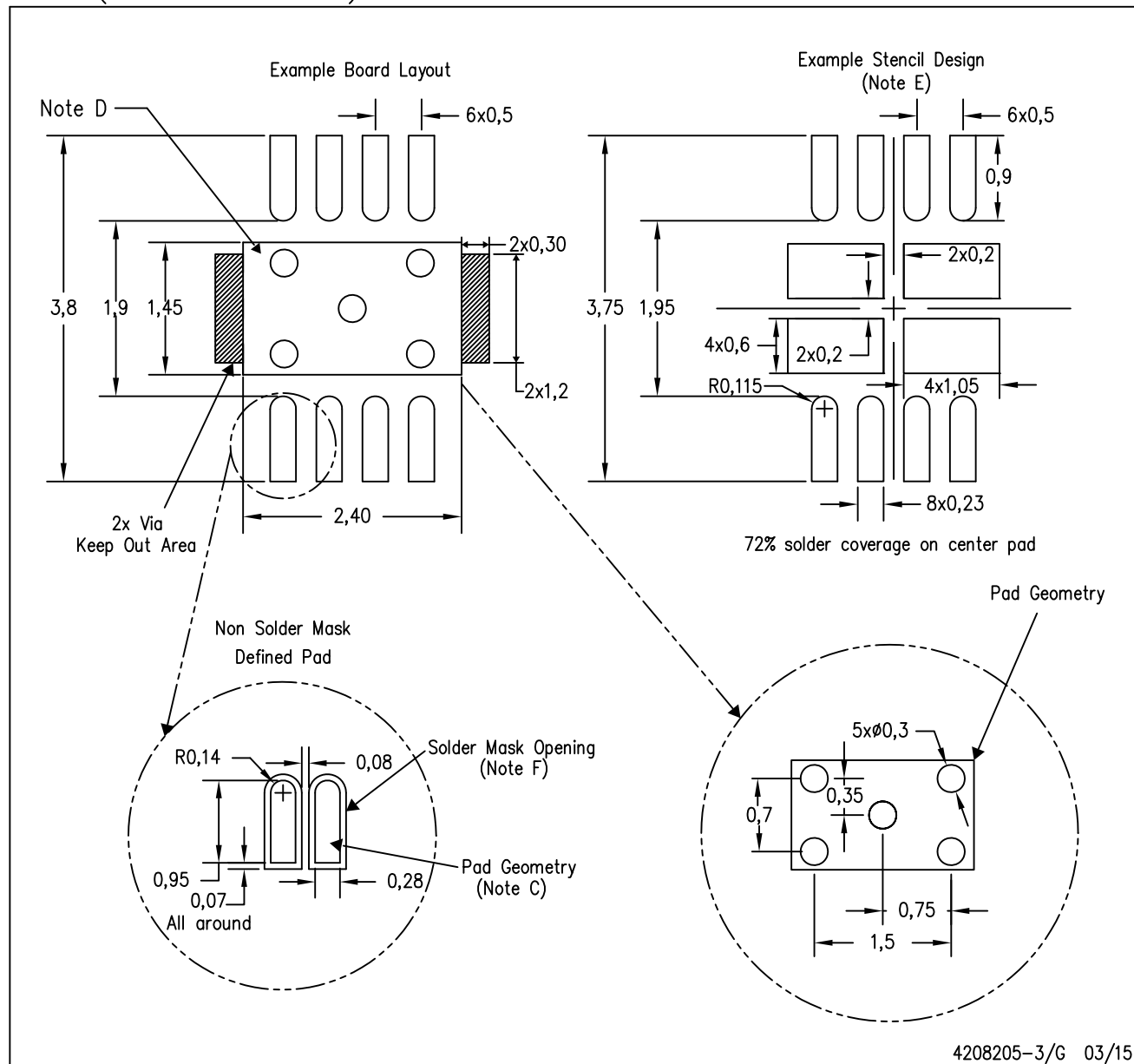
Exposed Thermal Pad Dimensions

4206881-3/1 03/15

NOTE: All linear dimensions are in millimeters

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated