I3C Slave IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02083-1.2

June 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LUT	Lookup-Table
I^2C	Inter-Integrated Circuit
LMMI	Lattice Memory Mapped Interface
SDA	Serial Data
SCL	Serial Clock
DA	Dynamic Address
SA	Static Address
DAA	Dynamic Address Assignment
NVM	Non Volatile Memory

1. Introduction

I3C is a two-wire bi-directional serial bus, optimized for multiple sensor Slave Devices and controlled by only one I3C Master Device at a time. I3C is backward compatible with many Legacy I^2C Devices, but I3C Devices also support significantly higher speeds, new communication Modes, and new Device roles, including an ability to change Device Roles over time (that is, the initial Master can cooperatively pass the Mastership to another I3C Device on the Bus, if the requesting I3C Device supports Secondary Master feature).

Lattice I3C IP is intended to improve upon the features of the I^2C interface, preserving backward compatibility.

Implementing the I3C Specification greatly increases the implementation flexibility for an ever-expanding sensor subsystem as efficiently and at as low cost as possible. Implementation follows the MIPI I3C specification to provide a single scalable, cost effective, power efficient protocol to solve issues with the high protocol overhead, increased power consumption, nonstandard protocol, separate lines for interrupt and the rest requirement. The MIPI I3C interface has been developed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.

Two main concerns are paramount for the I3C IP:

- use of as little energy as possible in transporting data and control
- reducing the number of physical pins used by the interface

The I3C interface provides major efficiencies in Bus power while providing greater than 10x speed improvements over I^2C.

This design is implemented in Verilog. Lattice Radiant® software Place and Route tool integrated with Synplify Pro® synthesis tool is used for design implementation. The design can be targeted to all CrossLink™-NX and Certus™-NX family devices. When used on a different device, density, speed or grade, performance and utilization may vary.

1.1. Quick Facts

Table 1.1 presents a summary of the I3C Slave IP Core.

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Family	CrossLink-NX, Certus-NX
Resource Utilization	Targeted Devices	LIFCL-40, LIFCL-17, LFD2NX-40
	Supported User Interfaces	LMMI (Lattice Memory Mapped Interface), APB, AHB-L
Design Tool Support	Lattice Implementation	IP Core v1.0.x – Lattice Radiant Software 2.1
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software 2.1 User Guide.

1.2. Features

An I3C Bus supports up to 11 I3C Slave Device, though the maximum number of Devices will depend on trace length, capacitive load per Controller, and the types of Devices (I^2C vs I3C) present on the Bus, because these factors affect clock frequency requirements.

The MIPI I3C Slave Controller supports the following features:

- Two wire serial interface up to 12.5 MHz using Push-Pull
- Legacy I^2C Device co-existence on the same Bus (with some limitations)
- I^2C -like Single Data Rate messaging (SDR)
- HDR-DDR messaging Mode
- In-Band Interrupt support
- Hot-Join support
- Timing Control Asynchronous mode 0 time stamping
- Synchronous Timing Support (not in this release)

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _*n* are active low (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

2. Functional Description

2.1. Overview

I3C Slave IP supports several communication formats, all sharing a two-wire interface: SDA bidirectional data line and SCL input.

The I3C communication protocol supports the following modes:

- SDR mode
- HDR-DDR mode

I3C bus is always initialized and configured in SDR Mode. Current implementation supports SDR and HDR-DDR modes.

The I3C Slave Controller accepts commands from LMMI interface. These commands are decoded into I3C Slave Device Read/Write transactions. Furthermore, the I3C Slave Controller can operate in interrupt or polling mode. This means that the LMMI interface can choose to poll the I3C Slave for a change in status at periodic intervals or wait to be interrupted by the I3C Slave Controller when data needs to be read or written.

An I3C Slave Controller listens to I3C Bus for relevant I3C Commands sent by the Current Master and responds accordingly. This includes all Broadcast Commands, and any Directed Commands addressed specifically to the I3C Slave Controller and supported by that I3C Slave Controller.

I3C Slave Controller can optionally:

- Request In-Band Interrupts
- Generate Hot-Join events
- Support I3C's defined HDR-DDR Mode

I3C Slave IP functional diagram is shown in Figure 2.1.

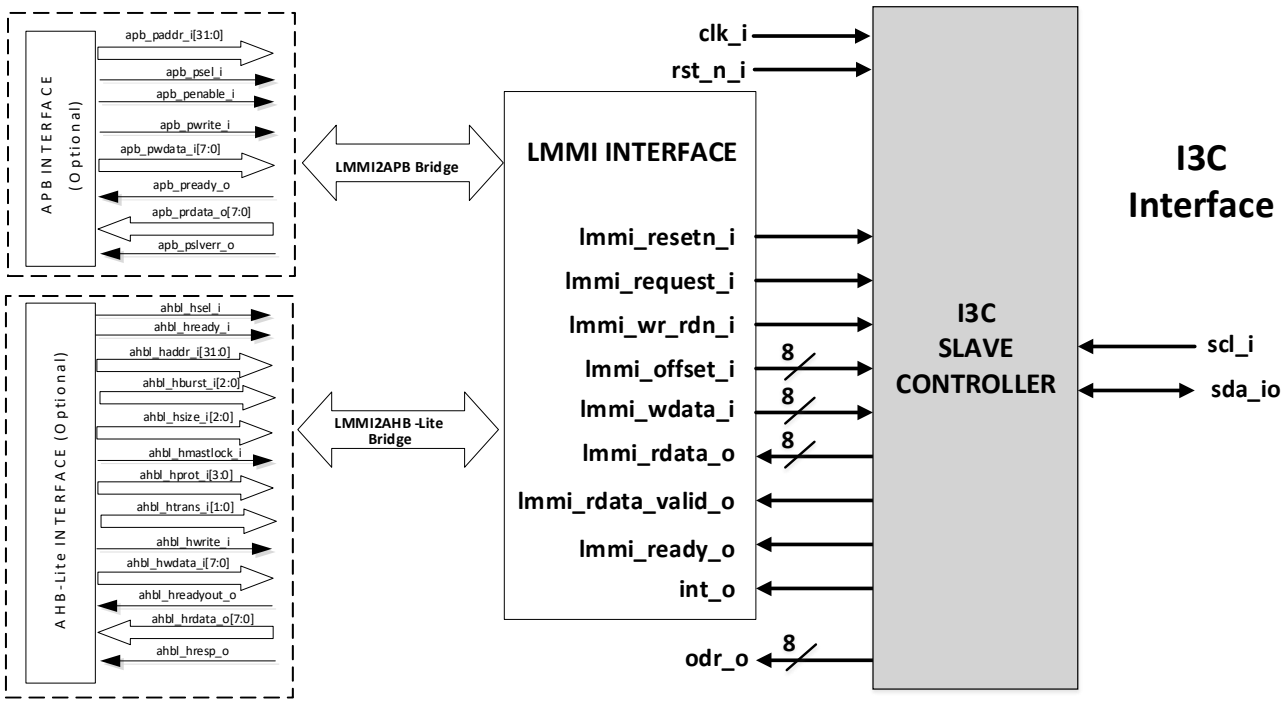

Figure 2.1. I3C Slave IP Core Functional Diagram

2.1.1. Modules

I3C Slave Controller design module contains the following functional blocks:

- LMMI interface
- I3C Slave Controller Top
  - Bus Management Block
    - Configuration Registers
    - Dynamic Address Capture
    - In-Band Interrupt and Hot-Join Management, Slave level
    - Data Packet Generator HDR-DDR and/or I^2C

A top-level block diagram of the I3C Slave Controller is shown in Figure 2.2.

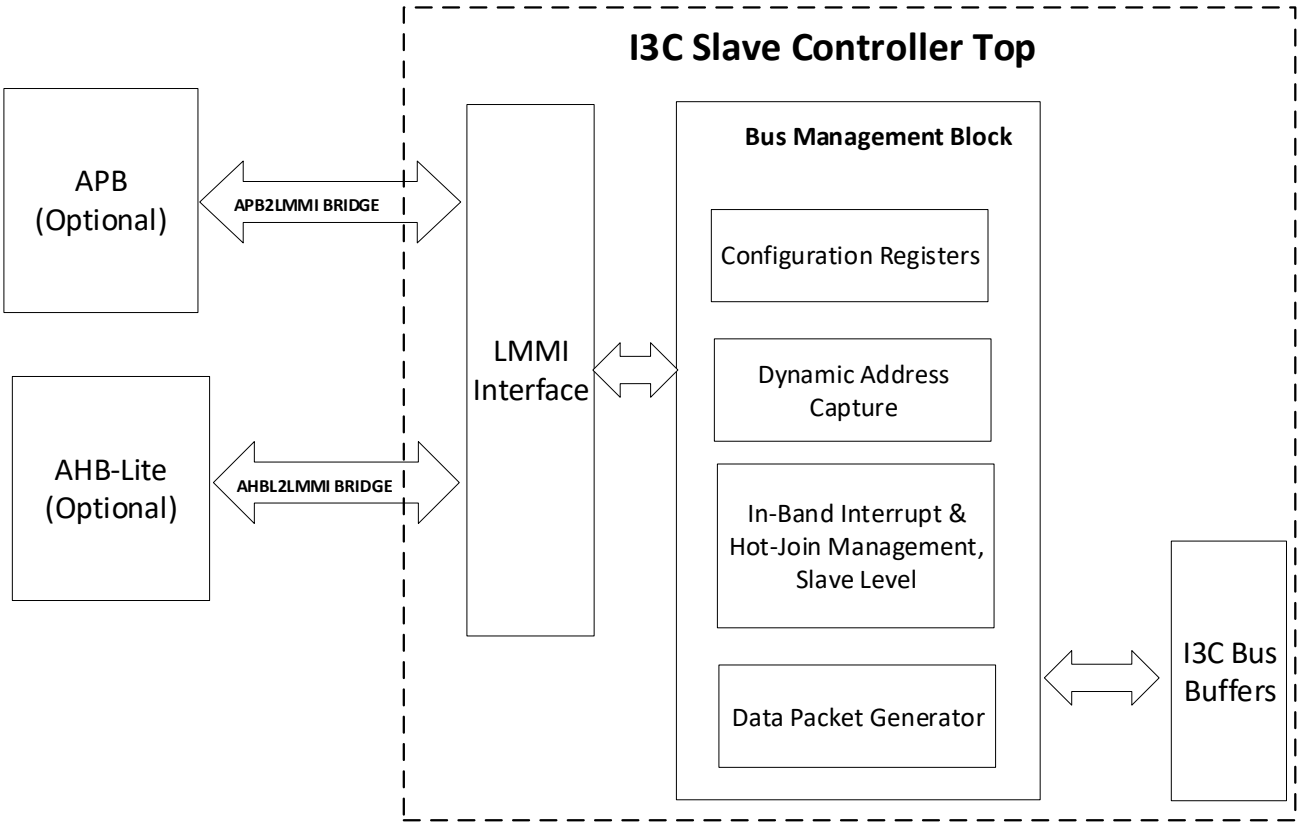

Figure 2.2. Top Level Block Diagram

2.1.2. I3C Slave Controller Top Logic

This is the top-level HDL block of the I3C Slave Controller design module. This block is created to instantiate all modules of the design and control of tri-state driver of the SDA line. I3C Slave Controller supports one of the two I3C Slave Device Roles:

- I3C Slave: An ordinary I3C Slave Device without Master capability. Supports both SDR Mode and HDR-DDR Mode.
- SDR-Only I3C Slave: An I3C Slave without Master capability that only supports I3C's SDR Mode (that is, does not support any of the HDR Modes).

Note: An additional Slave Device Role is defined for I^2C Slave. However, this is not relevant for an I3C Slave Device.

2.1.3. LMMI Interface

The LMMI, Lattice Memory Mapped Interface module implements memory mapped registers. LMMI is a memory-mapped address/data interface, which supports both single and burst transactions with a maximum throughput of one transaction per clock cycle.

LMMI module is a fully synchronous module that runs off the LMMI clock. A number of registers are initialized via the LMMI interface to ensure that the I3C Slave IP core functions as intended. LMMI defines a standard set of interface signals for register/memory access. The basic requirement is that any additional interface signals must not duplicate functionality described in this spec, that is, there should be only one interface (LMMI) for register/memory access.

This block also generates an interrupt signal when any of the Transmit Buffer Full, Receive Buffer Not Empty, IBI Acknowledge or Hot-Join Acknowledge interrupts are active.

The LINTR, Lattice Interrupt Interface module consists of an interrupt signal and a set of interrupt registers which are accessed through LMMI. These interrupt registers follow a standard functional definition, allowing you to implement common hardware/software to handle interrupts from a variety of Hard IP blocks.

For more information on LMMI, see the Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

2.1.4. AHB-Lite/APB to LMMI Bridge

When AHBL Mode is selected, AHBL2LMMI Bridge is instantiated inside the I3C Slave IP and the native LMMI interface is translated to AHB-Lite interface.

When APB Mode is selected, APB2LMMI is instantiated inside the I3C Slave IP and the native LMMI interface is translated to APB interface.

These optional bridges are implemented to easily interface the I3C Slave IP in APB and AHB-Lite systems while preserving the native LMMI interface for writing and reading to internal registers and FIFO

2.1.5. Bus Management Block

I3C bus is configured as the link among several clients, in a flexible and efficient manner. At the system architecture level, eight roles are defined for I3C-compatible Devices. An example block diagram of I3C interconnections is shown in Figure 2.3. In this diagram there is a device with Main Master role, Devices with I3C Slave role and Devices with I^2C Slave role. Note that I3C Secondary Master Devices are gradient shaded, illustrating their ability to function in both Master and Slave roles (at different times). I3C Slave IP implements I3C Slave as labelled in Figure 2.3.

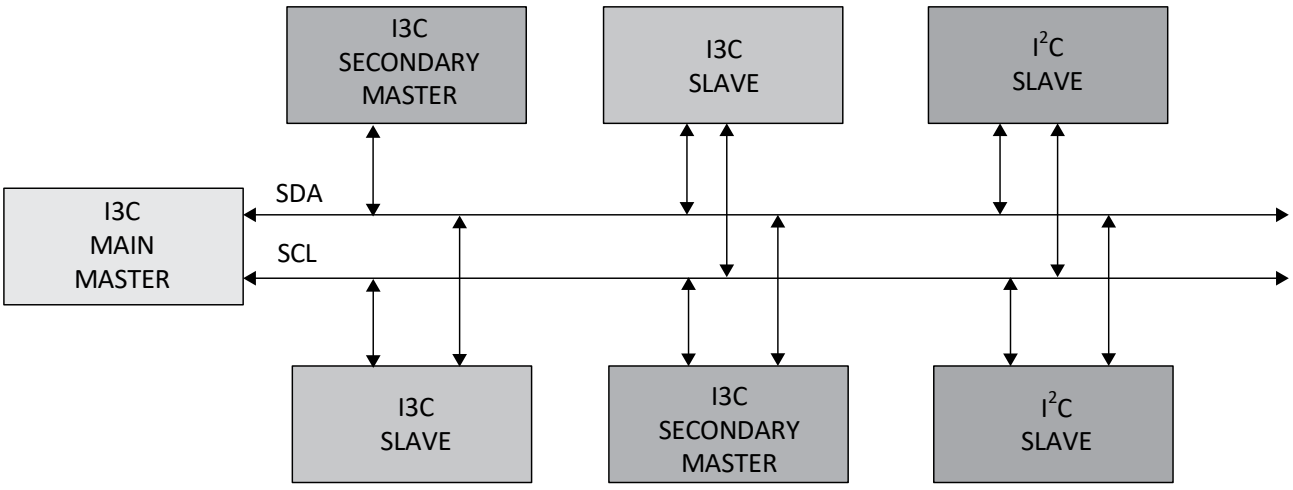

Figure 2.3. Bus Interconnect

2.1.5.1. I3C Configuration Registers

I3C Characteristics Registers describe and define an I3C compatible Device's capabilities and functions on I3C bus, as the Device services a given system. Devices without I3C Characteristics Registers should not be connected to a common I3C Bus.

There are three Characteristics Register types:

- Bus Characteristics Register (BCR)
- Device Characteristics Register (DCR)
- Legacy Virtual Register (LVR)

Every I3C compatible Device has associated Characteristics Registers, depending on the Device types described below:

- Every I3C compliant Device has one Bus Characteristics Register, and one Device Characteristics Register.
- Every Legacy I^2C Device to be connected to an I3C Bus has one associated Legacy Virtual Register. Since these are Legacy Devices, it is understood that this register will exist virtually, for example as part of the Device's driver.

2.1.5.2. Dynamic Address Capture

This block helps to capture Dynamic Address assignment performed by Main Master.

2.1.5.3. In-Band Interrupt and Hot-Join Management Block

To request an interrupt, an I3C Slave Controller emits its Address into the arbitrated Address header following a START (but not following a Repeated START). If no START is forthcoming within the Bus Available Condition, the I3C Slave Controller may issue a START Request by pulling the SDA line Low. In response, the Main Master sets the SCL clock line Low, completing the START Condition.

The I3C protocol supports a Hot-Join mechanism, to allow Slaves to join I3C Bus after it is already configured.

Note: Hot-Join does not allow Slaves to join I3C Bus before I3C Bus has been configured.

Hot-Joining Slaves may be any valid Slave type, including Secondary Master. After a Hot-Join, the Current Master uses the DEFSLVS CCC. To ensure that any Secondary Masters are aware of all of the available Slaves, the Master immediately notifies I3C bus if it discovers that any previously joined Slaves are no longer present on the Bus (e.g. due either to non-response, or to mechanisms outside of the Bus).

2.1.5.4. Data Packet Generator HDR-DDR

This block generates an I3C HDR-DDR mode data signals. The HDR-DDR Protocol uses the same signaling as SDR, but operates with SDA changing after each SCL edge. Each Command Word and each Data Word is 20 bits in length (20 clock edges) including a two-bit Preamble. HDR-DDR Command Words indicate the direction of data movement: either Write (Master to Slave), or Read (Slave to Master). After the Command Word, zero or more Data Words are sent by the Master or by the Slave (unless NACK-ed) until done, followed by the CRC Word (unless NACK-ed).

In HDR-DDR Mode, just as in SDR Mode, only I3C bus Master drives the SCL line. For Commands, the SDA line is driven by the Master. For Data, the SDA line is driven either by the Slave or by the Master, depending on the Command direction (Bus Turnaround).

There are three points of Bus Turnaround (between Master and Slave) with HDR-DDR Mode:

- After a Read Command from the Master, the Slave drives SDA to indicate that the Slave plans to return Data.
- After the end of Data from the Slave for a Read Command, the Master drives SDA again.
- There is an optional Bus Turnaround before Data Words are returned by the Slave, allowing the Master to prematurely terminate a Read.

2.1.6. Bus Characteristics Register (BCR)

Each I3C Device that is connected to I3C bus has an associated read-only Bus Characteristics Register (BCR). This read-only register describes the I3C compliant Device's role and capabilities for use in Dynamic Address assignment and Common Command Codes.

Table 2.1. Bus Characteristics Register

Bit	Name	Description
7	Device Role [1]	2'b00 – I3C Slave 2'b01 – I3C Master 2'b10 – Reserved for future definition 2'b11 – Reserved for future definition
6	Device Role [0]	
5	SDR Only / SDR and HDR-DDR Capable	0 – SDR only 1 – HDR-DDR Capable
4	Bridge Identifier	0 – Not a Bridge Device 1 – Is a Bridge Device
3	Offline Capable	0 – Device will always respond to I3C Bus commands 1 – Device will not always respond to I3C Bus commands
2	IBI Payload	0 – No data byte follows the accepted IBI 1 – Mandatory one or more data bytes follow the accepted IBI. Data byte continuation is indicated by T-Bit.
1	IBI Request Capable	0 – Not Capable 1 – Capable
0	Max Data Speed Limitation	0 – No Limitation 1 – Limitation

2.1.7. Device Characteristics Register (DCR)

Each I3C Device that is connected to I3C bus has an associated read-only Device Characteristics Register (DCR). This read-only register describes the I3C compliant Device type (e.g. accelerometer, gyroscope, etc.) for use in Dynamic Address assignment and Common Command Codes.

Table 2.2. Device Characteristics Register

Bit	Name	Description
7	Device ID [7]	255 available codes for describing the type of sensor, or Device. Examples: Accelerometer, gyroscope, composite Devices. Default value is 8'b0: Generic Device
6	Device ID [6]	
5	Device ID [5]	
4	Device ID [4]	
3	Device ID [3]	
2	Device ID [2]	
1	Device ID [1]	
0	Device ID [0]	

2.2. Signal Description

Table 2.3 lists the input and output signals for I3C Slave IP Core along with their descriptions.

Table 2.3. Ports Description

Signal	Direction	Description
System Clock and Reset		
rst_n_i	Input	System reset from the Host
clk_i	Input	System/Core clock
I3C Interface		
scl_i	Input	I3C clock input to Slave from Master
sda_io	In/Out	Bidirectional SDA data bus
LMMI Interface[1]		
lmmi_resetn_i	Input	LMMI reset (active low) Resets the LMM interface and sets registers to their default values. Does not reset the internals of the Hard IP block.
lmmi_request_i	Input	Start transaction
lmmi_wr_rdn_i	Input	Write = HIGH, Read = LOW
lmmi_offset_i[7:0]	Input	Register offset within Slave, starting at offset 0.
lmmi_wdata_i[7:0]	Input	Write data
lmmi_rdata_o[7:0]	Output	Read data
lmmi_rdata_valid_o	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	Output	Slave is ready to start a new transaction.
LINTR Interface		
int_o	Output	Interrupt to the Host. Stays high while an enabled interrupt is active.
AHB-Lite Interface[2]		
ahbl_hsel_i	Input	AHB-Lite Select signal.
ahbl_hready_i	Input	AHB-Lite Ready Input signal.
ahbl_haddr_i[31:0]	Input	AHB-Lite Address signal. ([9:2] used)
ahbl_hburst_i[2:0]	Input	AHB-Lite Burst Type signal.
ahbl_hsize_i[2:0]	Input	AHB-Lite Transfer Size signal.
ahbl_hmastlock_i	Input	AHB-Lite Lock signal.
ahbl_hprot_i[3:0]	Input	AHB-Lite Protection Control signal.
ahbl_htrans_i[1:0]	Input	AHB-Lite Transfer Type signal.
ahbl_hwrite_i	Input	AHB-Lite Direction signal. Write = High, Read = Low.
ahbl_hwdata_i[31:0]	Input	AHB-Lite Write Data signal ([7:0] used).
ahbl_hreadyout_o	Output	AHB-Lite Ready Output signal.
ahbl_hrdata_o[31:0]	Output	AHB-Lite Read Data signal ([7:0] used).
ahbl_hresp_o	Output	AHB-Lite Transfer Response signal.
APB Interface[3]		
apb_paddr_i[31:0]	Input	APB Address signal. ([9:2] used)
apb_psel_i	Input	APB Select signal.
apb_penable_i	Input	APB Enable signal.
apb_pwrite_i	Input	APB Direction signal.
apb_pwdata_i[31:0]	Input	APB Write Data signal ([7:0] used).
apb_pready_o	Output	APB Ready signal.
apb_prdata_o[31:0]	Output	APB Read Data signal ([7:0] used).
apb_pslverr_o	Output	APB Slave Error signal.
Direct Sensor Interface		
odr_o[7:0]	Output	ODR to the sensor received from I3C bus (SETXTIME feature)

Notes:

1. LMMI Interface is only available when selected from the user interface.
2. AHB-Lite Interface is only available when selected from the user interface. Refer to AMBA 3 AHB-Lite Protocol Specification for details of the protocol.
3. APB Interface is only available when selected from the user interface. Refer to AMBA 3 APB Protocol v1.0 Specification for details of the protocol.

2.3. Attributes Summary

Table 2.4 provides the list of user-selectable and compile time configurable parameters for the I3C Slave IP Core. Attributes are described in Table 2.5. The parameter settings are specified using I3C Slave IP Core Configuration user interface in Lattice Radiant.

Table 2.4. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
CPU Interface			
Interface	LMMI, APB, AHBL	LMMI	None
Bus Characteristics			
Bus Type	SDR-only, HDR-capable	HDR-capable	None
HDR Type	DDR only	DDR	Bus Type = HDR capable
Offline Capable	Not Checked	Not Checked	None
IBI Capable	Checked, Not Checked	Not Checked	None
IBI Number of bytes in a single sample [0–128]	0–128	2	IBI Capable = True
Hot-Join Capable	Checked, Not Checked	Checked	None
Max Data Speed Limitation	Checked	Checked	None
Device Characteristics: Run-Time Configurable			
DCR Value (hex) [0–FF]	0–FF	0	None
Static Address Enable	Checked, Not Checked	Checked	None
Static Address (hex) [4–7D]	4–7D	35	Static Address Enable = True
Manufacturer ID [0–32767]	0–32767	414	—
Part ID [0–65535]	0–65535	1	—
Instance ID [0–15]	0–15	1	—
Additional ID [0–4095]	0–4095	0	—
Output Data Rate in KSMPS [0–250]	0–250	50	—
Device Characteristics			
FIFO Address Width	10	10	—
Timing Characteristics			
System Clock Frequency (MHz) [80–100]	80–100	100	—
Max Write Data Speed	Max, 8 MHz, 6 MHz, 4 MHz, 2 MHz	Max	—
Max Read Data Speed	Max, 8 MHz, 6 MHz, 4 MHz, 2 MHz	Max	—
Max Clock to Data Turnaround Time	8 ns, 9 ns, 10 ns, 11 ns, 12 ns	>12 ns	—
Max Write Data Length	1024	1024	—
Max Read Data Length	1024	1024	—

Table 2.5. Attributes Descriptions

Attribute	Description
General	
CPU Interface	
Interface	Selects memory-mapped interface from the list for register access by the host Available values: LMMI (default), APB, AHBL
Bus Characteristics	
Bus Type	HDR capability. Always capable (common state machine for all modes). Grayed out.
HDR Type	HDR supported modes. Only DDR is supported. Grayed out
Offline Capable	Offline capability support. Currently grayed out, not supported, since the related data must be stored in NVM.
IBI Capable	IBI capability selector
IBI Number of bytes in a single sample	IBI payload size selector
Hot-Join Capable	HJ capability selector
Max Data Speed Limitation	Checked for not supported TSL/TSP modes. Grayed out.
Bus Type	HDR capability. Always capable (common state machine for all modes). Grayed out.
Max Data Speed Limitation	Secondary master feature. Checked for not supported TSL/TSP modes. Grayed out.
Settings	
Device Characteristics: Run-Time Configurable	
DCR Value (hex)	Device Characteristics register. It is recommended to assign a value to this register according to the list of the devices, which can be found at https://www.mipi.org/MIPI_I3C_device_characteristics_register.
Static Address Enable	SA may be assigned to device, which will be accessible to the host. Main Master may assign DA to this device using the SA bypassing the DAA procedure, if knows its SA (designer must pass the SA to the Main Master host application).
Static Address (hex)	Defines device's SA
Manufacturer ID	Defines Provisional ID[47:33] bits
Part ID	Defines Provisional ID[31:16] bits
Instance ID	Defines Provisional ID[15:12] bits
Additional ID	Defines Provisional ID[11:0] bits
Output Data Rate in KSMPS	Sensor ODR
Device Characteristics	
FIFO Address Width	Defines depth of FIFOs. Set to 10, since EBR is used for a FIFO in any case. Greyed out
Timing Characteristics	
System Clock Frequency (MHz)	Interface/sampling clock frequency. Recommended value is 100MHz.
Max Write Data Speed	Maximum I3C bus data write speed for device. Device is capable of max speed.
Max Read Data Speed	Maximum I3C bus data read speed for device. Device is capable of max speed.
Max Clock to Data Turnaround Time	The time duration between reception of an SCL edge and the start of driving an SDA change. Set to maximum for safety.
Max Write Data Length	Max write data capability. Equals to $2^{(\text{FIFO Address width})}$. Set to 1024 for this release, greyed out.
Max Read Data Length	Max read data capability. Equals to $2^{(\text{FIFO Address width})}$. Set to 1024 for this release, greyed out

2.4. Register Description

2.4.1. I3C Slave Commands

Direct access with Dynamic Address without active CCC gives access to both, Tx and Rx FIFOs. The following I3C Slave IP commands are supported in this release.

Table 2.6. Supported I3C Slave IP Commands

Command Code	Command Name (MIPI Standard v1.0)	Type*	Comment
0x00	ENEC	B	Enable Slave event driven interrupts
0x01	DISEC	B	Disable Slave event driven interrupts
0x06	RSTDAA	B	Forget current Dynamic Address and wait for new assignment
0x07	ENTDAA	B	Entering Master initiation of Slave Dynamic Address Assignment. Do not participate if the Slave already has an Address assigned.
0x09	SETMWL	B	Set maximum write length in a single command
0x0A	SETMRL	B	Set maximum read length in a single command
0x20	ENTHDR0	B	Enter HDR Mode 0
0x28	SETXTIME	B	Only Async 0 mode is supported
0x80	ENEC	D	Enable Slave event driven interrupts
0x81	DISEC	D	Disable Slave event driven interrupts
0x86	RSTDAA	D	Forget current Dynamic Address and wait for new assignment
0x87	SETDASA	D	Set Dynamic Address from Static Address
0x88	SETNEWDA	D	Set New Dynamic Address
0x89	SETMWL	D	Set maximum write length in a single command
0x8A	SETMRL	D	Set maximum read length in a single command
0x8B	GETMWL	D	Get Slave's maximum possible write length
0x8C	GETMRL	D	Get Slave's maximum possible read length
0x8D	GETPID	D	Get Provisional ID
0x8E	GETBCR	D	Get Bus Characteristics Register
0x8F	GETDCR	D	Get Device Characteristics Register
0x90	GETSTATUS	D	Get a Device's operating status
0x95	GETHDRCAP	D	Master asks Slave what HDR Modes it supports
0x98	SETXTIME	D	Only Async 0 mode is supported
0x99	GETXTIME	D	Only Async 0 mode is supported
DA	Read	D	Read from FIFO (granularity: 8-bit SDR, 16-bit HDR)
DA	Write	D	Write to FIFO (granularity: 8-bit SDR, 16-bit HDR)

*__Note:__ B - Broadcast, D - Direct, DA – device's dynamic address

2.4.2. Register Address Map

I3C Slave Controller configuration and status registers are located at the addresses shown in Table 2.7. Detailed description of the register bits is in the Registers Bits Description section. Table 2.8 lists the 48-bit Provisional ID bit mapping.

Table 2.7. Register Address Map

LMMI Offset HEX	APB/AHB Offset HEX	LMMI APB/ AHB RW	Register	Used Bits	Description
0	0000	RW	BCR	[7:0]	Write is for debugging only. Parameter BCR
1	0004	RW	DCR	[7:0]	Write is for debugging only. Parameter DCR
2	0008	RW	DA	[6:0]	Dynamic Address assigned by Master
3	000C	RW	HjMrIbi	[5:0]	LMMI / I3C bus controllable HJ and IBI enables
7	001C	RO	mwl_msb	[7:0]	mwl[15:8]. Max value is 1024 (EBR)
8	0020	RO	mwl_lsb	[7:0]	mwl[7:0]
9	0024	RO	mrl_msb	[7:0]	mrl[15:8]. Max value is 1024 (EBR)
A	0028	RO	mrl_lsb	[7:0]	mrl[7:0]
B	002C	RW	mxds2_msb	[7:0]	two bytes of max data speed (GETMXDS). Write is for debugging only
C	0030	RW	mxds2_lsb	[7:0]	parameter MAX_D_SPEED
D	0034	RW	mtrt0	[7:0]	max turnaround time byte 0
E	0038	RW	mtrt1	[7:0]	max turnaround time byte 1
F	003C	RW	mtrt2	[7:0]	max turnaround time byte 2
10	0040	RW	pid5	[7:0]	PID_MANUF[14:7].
11	0044	RW	pid4	[7:0]	{PID_MANUF[6:0], 1'b0}
12	0048	RW	pid3	[7:0]	PID_PART[15:8]
13	004C	RW	pid2	[7:0]	PID_PART[7:0]
14	0050	RW	pid1	[7:0]	{PID_INST, PID_ADD[11:8]}
15	0054	RW	pid0	[7:0]	PID_ADD[7:0]
16	0058	RW	SA	[6:0]	Static Address (hardwired in core but may be modified by LMMI) parameter STAT_ADDR
17	005C	RW	inaccuracy	[7:0]	Internal frequency oscillator inaccuracy in 0.1% increments
18	0060	RO	odr	[7:0]	LMMI - read, Core - write. ODR (set by SETXTIME)
19	0064	RO	max_ibi_pl		LMMI - read, Core - write
20	0080	LMMI-R I3C-W	Read FIFO	[7:0]	I3C bus write to device. In HDR mode first LMMI read returns MSB, next - LSB
21	0084	LMMI-R I3C-W	num_slaves	[3:0]	Number of Slaves captured from latest DEFSLVS (not used if not Secondary Master)
22	0088	LMMI-W I3C-R	Write FIFO	[7:0]	Device read by I3C bus. In HDR mode first LMMI write is for MSB, next - LSB
24	0090	RW	hdr_wrcmd_code	[7:0]	HDR Write Command Code
25	0094	RW	hdr_rdcmd_code	[7:0]	HDR Read Command Code
26	0098	LMMI-RO	block_ibi	[0]	P2P SETDASA Configuration Indication
38	00E0	LMMI-RO	i3c_sts_sdr_msb	[7:0]	I3C status SDR [15:8]
39	00E4	LMMI-RO	i3c_sts_sdr_lsb	[7:0]	I3C status SDR [7:0]
3A	00E8	LMMI-RO	i3c_sts_hdr_msb	[7:0]	I3C status HDR [15:8]
3B	00EC	LMMI-RO	i3c_sts_hdr_lsb	[7:0]	I3C status HDR [7:0]
3C	00F0	LMMI-WO	rst_errors	NA	SDR/HDR status reset
3D	00F4	LMMI-WO	rst_errors	NA	IBI ACK flag reset

LMMI Offset HEX	APB/AHB Offset HEX	LMMI APB/ AHB RW	Register	Used Bits	Description
F0	03C0	RW	intr_status	[7:0]	Interrupt status register
F1	03C4	RW	intr_enable	[7:0]	Interrupt enable register
F2	03C8	W	intr_set	[7:0]	Interrupt set register
F3	03CC	R	FIFO status	[3:0]	FIFO Current State

Table 2.8. Register Address Map

I3C Command Code	Description	Note
[47:33]	MIPI Manufacturer ID [MIPI01]	15 bits. The Most Significant Bit of the MIPI Manufacturer ID is discarded, that is only the 15 Least Significant Bits are used.
[32]	Provisional ID Type Selector	One bit, 1'b1: Random Value, 1'b0: Vendor Fixed Value.*
[31:16]	Part ID	The meaning of this 16-bit field is left to the Device vendor to define.
[15:12]	Instance ID	The value in this 4-bit field should identify the individual Device, using a method selected by the system designer. For example, straps, fuses, non-volatile memory, or another appropriate method.
[11:0]	Additional ID	The meaning of this 12-bit field is left for definition with additional meaning. For example, deeper Device Characteristics, which could optionally include Device Characteristic Register values.

***Note:** (Not implemented in this release) If the value of Bit [32] is 1'b1 (Random Value), Bits [31:0] - value randomly generated by the Device. This value can be queried via General Test Mode, using the Command Code Enter Test Mode (ENTTM). Under Vendor Test Mode, the Device may provide a fully random or pseudo-random 48-bit Provisional ID.

2.4.3. In Band Interrupt and Hot Join request results

IBI generation is controllable from both I3C bus and LMMI side (LMMI offset). After IBI or HJ interrupt enable from LMMI side and if it is also enabled by I3C Master, the Slave waits for 1 µs (Requirement in the MIPI standard is 5 µs. Working group is proposed 1 µs, what is out of standard but matches the implementation) for IBI request sending or 1 ms for HJ then drives the SDA line low. Delays have about 0.3 µs and 1 µs accuracy. If master ACKs the request (pulls SCL low), Slave sends its address to the bus. If the Slave won arbitration and received ACK from the master, payload bytes are sent to the master depending on BCR[2] value.

2.4.4. LMMI Interrupts

LMMI Interrupt mechanism is served by three registers: Status, Mask and Set. Status register bits are described in SDR Status Register MSB, SDR Status Register LSB, HDR Status Register MSB, HDR Status Register LSB, and SDR and HDR Status Register Reset section. Writing 1 to the corresponding bit of this register clears the bit. Enable register controls whether interrupts in the Status register assert the int_o signal or not. It does not affect the contents of the Status register. If one of the interrupt sources in the IP Block generates an interrupt event (edge triggered), it sets the corresponding bit in the Status register regardless of whether the interrupt is enabled or disabled in the Enable register. Interrupt is generated by bitwise ANDing Status and Enable and then doing a reduction OR of the result.

In Verilog, this looks like:

int_o = |(Status & Enable)

The interrupt Set register allows you to set bits in the Status register. Writing this register sets pending interrupts for each bit set to '1'.

Table 2.9. LMMI Interrupt Status Map

Bit	RW	Default	Description
[7]	RW	0	HJ interrupt has been generated
[6]	RW	0	SMR interrupt has been generated
[5]	RW	0	IBI interrupt has been generated
[4]	RW	0	HJ interrupt has been acknowledged
[3]	RW	0	SMR has been acknowledged
[2]	RW	0	IBI interrupt has been acknowledged
[1]	RW	0	Receive FIFO data ready (FIFO is not empty)
[0]	RW	0	Transmit FIFO is full

2.4.5. Registers Bits Description

Each table below represents a register bit from Table 2.7.

Table 2.10. Bus Characteristics Register

Bits	Mode	Description
[7:6]	R	Device role: 2'b00 - I3C Slave 2'b01 - I3C Master/Secondary Master 2'b10, 2'b11 - Reserved for future definition by MIPI Sensor WG
[5]	R	HDR capability: 0 - SDR only, 1 - HDR-DDR Capable
[4]	R	Bridge identifier: 0 - Not a Bridge Device, 1 - Is a Bridge Device
[3]	R	Offline capable: 0 - Device will always respond to I3C Bus commands 1 - Device will not always respond to I3C Bus commands
[2]	R	IBI payload: 0 – No data byte follows the accepted IBI 1 – Mandatory one or more data bytes follow the accepted IBI. Data byte continuation is indicated by T-Bit.
[1]	R	IBI request capable: 0 - Not Capable, 1 - Capable
[0]	R	Max data speed limitation: 0 - No Limitation, 1 - Limitation

Table 2.11. Device Characteristics Register

Bits	Mode	Description
[7:0]	R	255 available codes for describing the type of sensor, or Device. Examples: Accelerometer, gyroscope, composite Devices. Default value is 8'b0: Generic Device

Table 2.12. Dynamic Address

Bits	Mode	Description
[6:0]	R	Dynamic address assigned by the Master

Table 2.13. IBI, HJ Control

Bits	Mode	Default	Access	Description
[7:6]	R	0		Reserved
[5]	RW	0	LMMI	HJ request enable
[4]	R	0	LMMI	Reserved
[3]	RW	0	LMMI	IBI request enable
[2]	W	1	I3C	HJ request enable by ENEC/DISEC
[1]	W	0	I3C	Reserved
[0]	W	0	I3C	IBI request enable ENEC/DISEC

Table 2.14. Maximum Write Length MSB

Bits	Mode	Description
[7:0]	R	Maximum Write Length [15:0]

Default value is 1024 bytes. For data storing an EBR based FIFO is used.

Table 2.15. Maximum Write Length LSB

Bits	Mode	Description
[7:0]	R	Maximum Write Length [7:0]

Table 2.16. Maximum Read Length MSB

Bits	Mode	Description
[7:0]	R	Maximum Read Length [15:0]

Default value is 1024 bytes. For data storing an EBR based FIFO is used.

Table 2.17. Maximum Read Length LSB

Bits	Mode	Description
[7:0]	R	Maximum Read Length [7:0]

Table 2.18. Maximum Write Data Speed

Bits	Mode	Description
[7:3]	RW	RESERVED
[2:0]	RW	Maximum Sustained Data Rate for non-CCC messages sent by Master Device to Slave Device. 0: fSCL Max (default value) 1: 8 MHz 2: 6 MHz 3: 4 MHz 4: 2 MHz 5-7: Reserved for future use by the MIPI Alliance

Table 2.19. Maximum Read Data Speed

Bits	Mode	Description
[7:3]	RW	RESERVED
[5:3]	RW	Clock to Data Turnaround Time (TSCO). 0: <= 8 ns (default value) 1: <= 9 ns 2: <= 10 ns 3: <= 11 ns 4: <= 12 ns 5-7: Reserved for future use by the MIPI Alliance
[2:0]	RW	Maximum Sustained Data Rate for non-CCC messages sent by Master Device to Slave Device. 0: fSCL Max (default value) 1: 8 MHz 2: 6 MHz 3: 4 MHz 4: 2 MHz 5-7: Reserved for future use by the MIPI Alliance

Table 2.20. Maximum Turnaround Time LSB

Bits	Mode	Description
[7:0]	RW	Maximum Turnaround Time in us. Least Significant Byte (byte 0)

Table 2.21. Maximum Turnaround Time MB

Bits	Mode	Description
[7:0]	RW	Maximum Turnaround Time in us. Middle Byte (byte 1)

Table 2.22. Maximum Turnaround Time MSB

Bits	Mode	Description
[7:0]	RW	Maximum Turnaround Time in us. Most Significant Byte (byte 2)

Table 2.23. Provisional ID Byte 5

Bits	Mode	Description
[7:0]	RW	Manufacturer ID [14:7]

Table 2.24. Provisional ID Byte 4

Bits	Mode	Description
[7:1]	RW	Manufacturer ID [6:0]
[0]	RW	0

Table 2.25. Provisional ID Byte 3

Bits	Mode	Description
[7:0]	RW	Part ID [15:8]

Table 2.26. Provisional ID Byte 2

Bits	Mode	Description
[7:0]	RW	Part ID [7:0]

Table 2.27. Provisional ID Byte 1

Bits	Mode	Description
[7:4]	RW	Instance ID [3:0]
[3:0]	RW	Additional ID [11:8]

Table 2.28. Provisional ID Byte 0

Bits	Mode	Description
[7:0]	RW	Additional ID [7:0]

Table 2.29. Static Address

Bits	Mode	Description
[7]	RW	DC
[6:0]	RW	7-bit static address

Table 2.30. Frequency Inaccuracy

Bits	Mode	Description
[7:0]	RW	Inaccuracy of the internal clock for Timing Control functionality. In 0.1% increments

Table 2.31. Output Data Rate

Bits	Mode	Description
[7:0]	R	ODR of the sensor connected to I3C slave controller, if supported. In KSPS. Default is 50 KSPS. Command: SETXTIME+8F+ODR

Table 2.32. Maximum IBI Payload Size

Bits	Mode	Description
[7:0]	R	In bytes. Third byte of SETMRL command. Ignored if the Slave is configured with no IBI support

Table 2.33. Read FIFO

Bits	Mode	Description
[7:0]	RW	Data bytes received from I3C bus are stored in this FIFO. In HDR mode MSB is stored first.

Table 2.34. Number of Slaves Captured from DEFSLVS

Bits	Mode	Description
[7:0]	RW	Number of slave devices on I3C bus returned by latest DEFSLVS command issued by Master

Table 2.35. Write FIFO

Bits	Mode	Description
[7:0]	RW	Data to be sent to I3C bus are stored in this FIFO. In HDR mode MSB must be stored first.

Table 2.36. HDR Write Command Code

Bits	Mode	Description
[7:0]	R/W	HDR Write Command Code of the Secondary Master in Slave mode. Defaults to 0x20

Table 2.37. HDR Read Command Code

Bits	Mode	Description
[7:0]	R/W	HDR Read Command Code of the Secondary Master in Slave mode. Defaults to 0xA0

Table 2.38. P2P SETDASA Configuration Indication

Bits	Mode	Description
[7:1]	R	RESERVED
[0]	R/W	Indicates IBI Blocking

Table 2.39. SDR Status Register MSB

Bits	Mode	Description
[7:0]	RW	SDR operation status [15:0]

Table 2.40. SDR Status Register LSB

Bits	Mode	Description
[7:0]	RW	SDR operation status [7:0]

Table 2.41. Error Status for SDR Mode

Value	Description
0x0001	T-bit error
0x0002	DA parity error
0x0004	abnormal command termination with stop
0x0008	IBI read data master abort
0x0010	early data devastation (IBI)
0x0020	directed read master abort

Table 2.42. HDR Status Register MSB

Bits	Mode	Description
[7:0]	RW	HDR operation status [15:0]

Table 2.43. HDR Status Register LSB

Bits	Mode	Description
[7:0]	RW	HDR operation status [7:0]

Table 2.44. Error Status for HDR Mode:

Value	Description
0x0001	wrong preamble in cmd phase
0x0002	unsupported cmd
0x0004	cmd+DA parity error
0x0008	preamble bit1 is not 1
0x0010	master abort HDR during read
0x0020	data transfer limit is hit
0x0040	first write preamble error (must be 10)
0x0080	wrong preamble during write (00 or 10)
0x0100	write FIFO is full
0x0200	CRC_W error

Table 2.45. SDR and HDR Status Register Reset

Bits	Mode	Description
[7:0]	W	Writing to this address resets both status registers

Table 2.46. IBI ACK Flag Reset

Bits	Mode	Description
[7:0]	W	Writing to this address resets IBI acknowledge flag

Table 2.47. LMMI Interrupt Status

Bits	Mode	Description
[7]	RW	Latched generated HJ request event
[6]	RW	Latched generated SMR event (not used). Reserved
[5]	RW	Latched generated IBI event
[4]	RW	Latched HJ ACK
[3]	RW	Latched SMR ACK (not used). Reserved
[2]	RW	Latched IBI ACK
[1]	RW	Read FIFO is not empty
[0]	RW	Write FIFO is full

Writing 1 to the corresponding bit of this register clears it.

Table 2.48. LMMI Interrupt Enable

Bits	Mode	Description
[7:0]	RW	Enable bits for the interrupts described in Interrupt Status Register (0xF0)

Table 2.49. LMMI Interrupt Set

Bits	Mode	Description
[7:0]	W	Set bits for the interrupts described in Interrupt Status Register (0xF0)

Table 2.50. FIFO Current State

Bits	Mode	Description
[7:4]	R	RESERVED
[3]	R	Read FIFO is almost empty
[2]	R	Read FIFO is empty
[1]	R	Write FIFO is almost full
[0]	R	Write FIFO is full

2.5. Programming Flow

Figure 2.4 illustrates I3C Slave key transmission modes.

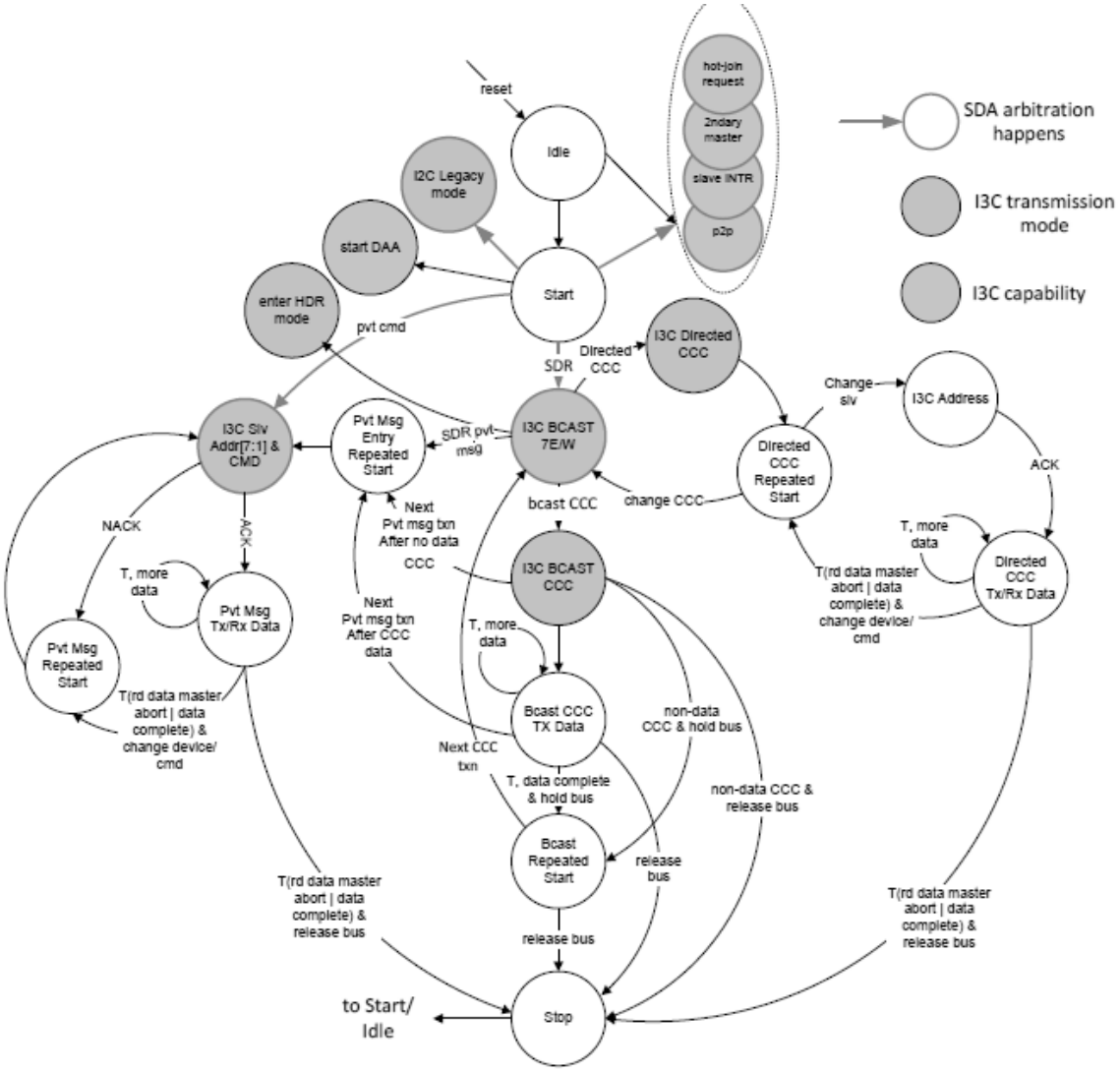

Figure 2.4. I3C Main Master Key Transmission Modes

2.5.1. Data Transfer

Slave device has two FIFOs for data transmission and receiving. Both FIFOs can accommodate up to 1024 bytes of data. In SDR direct addressing mode the Tx FIFO (LMMI to I3C) is the target, if the read access is requested by I3C master. The Rx FIFO (I3C to LMMI) is the target upon write request. LMMI reads the Rx FIFO at the address 0x20. LMMI writes to 0x22 are directed to Tx FIFO.

In HDR-DDR mode the Slave controller accesses the FIFOs by word assuming the data is written with MSB first. The only acceptable commands in HDR_DDR mode are read (0xA0 by default, register 0x25) and write (0x20 by default, register 0x24).

2.5.2. Initialization

Before using I3C Slave core, host may need to modify the default values of the Run-time Registers listed below:

- 0x00: BCR
- 0x16: SA
- 0x24: HDR Write Command Code
- 0x25: HDR Read Command Code

The host may also need to set the interrupt enable bits (see Table 2.48.)

After bus initialization by I3C Master, Slave is ready for I3C transactions. In order to send data to the I3C bus, host (or sensor) must write data into Write FIFO (0x22). Read data is stored in Read FIFO (0x20). In case the Slave interface is used in sensor, I3C Master can control its 8-bit ODR (in KSPS).

The Hot Join feature is enabled by default; however, it still needs to be activated by host (address 0x03, bit [5]). I3C Master may disable this feature according to protocol.

2.5.3. FIFO Interrupt Mode Operation

When *Read FIFO Is Not Empty* interrupt is enabled (address 0xF1, bit [1]), received data are available in the FIFO (0x20). Note that the number of bytes written into Write FIFO must be within the limits set in the Maximum IBI Payload Size Register (see Table 2.32). Otherwise, all extra bytes are read during the next IBI procedure. IBI is controllable by Master according to protocol.

When *Write FIFO Is Ful*" interrupt is enabled (address 0xF1, bit [0]), host must stop writing into Write FIFO, otherwise extra data is not sent.

For detailed error status in SDR and HDR operation modes, see SDR Status Register MSB in Table 2.39 and HDR Status Register MSB in Table 2.42.

2.6. Data Format

Data is in big endian format.

SDR data consume a byte in FIFO.

HDR data consume two bytes in FIFO and must be written or read MSB first.

2.7. Timing Diagrams

I3C bus timing and timing diagrams are described in *mipi_I3C_specification_v1-0*.

3. IP Core Generation, Simulation, and Validation

This section provides information on how to generate the I3C Slave IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software 2.1 User Guide.

3.1. Licensing the IP

An IP core-specific license string is required enable full use of the I3C Slave IP Core in a complete, top-level design.

When the IP Core used in LIFCL and LFD2NX devices, you can fully evaluate the IP core through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, which operate in hardware for a limited time (approximately four hours) without requiring an IP license string. See Hardware Evaluation section for further details. However, a license string is required to enable timing simulation and to generate bitstream file that does not include the hardware evaluation timeout limitation.

3.2. Generation and Synthesis

Lattice Radiant software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate the I3C Slave IP Core:

1. In the **Module/IP Block Wizard** create a new Lattice Radiant software project for I3C Slave module.
2. In the dialog box, configure the I3C Slave module according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 3.1. For configuration options, see Table 2.4

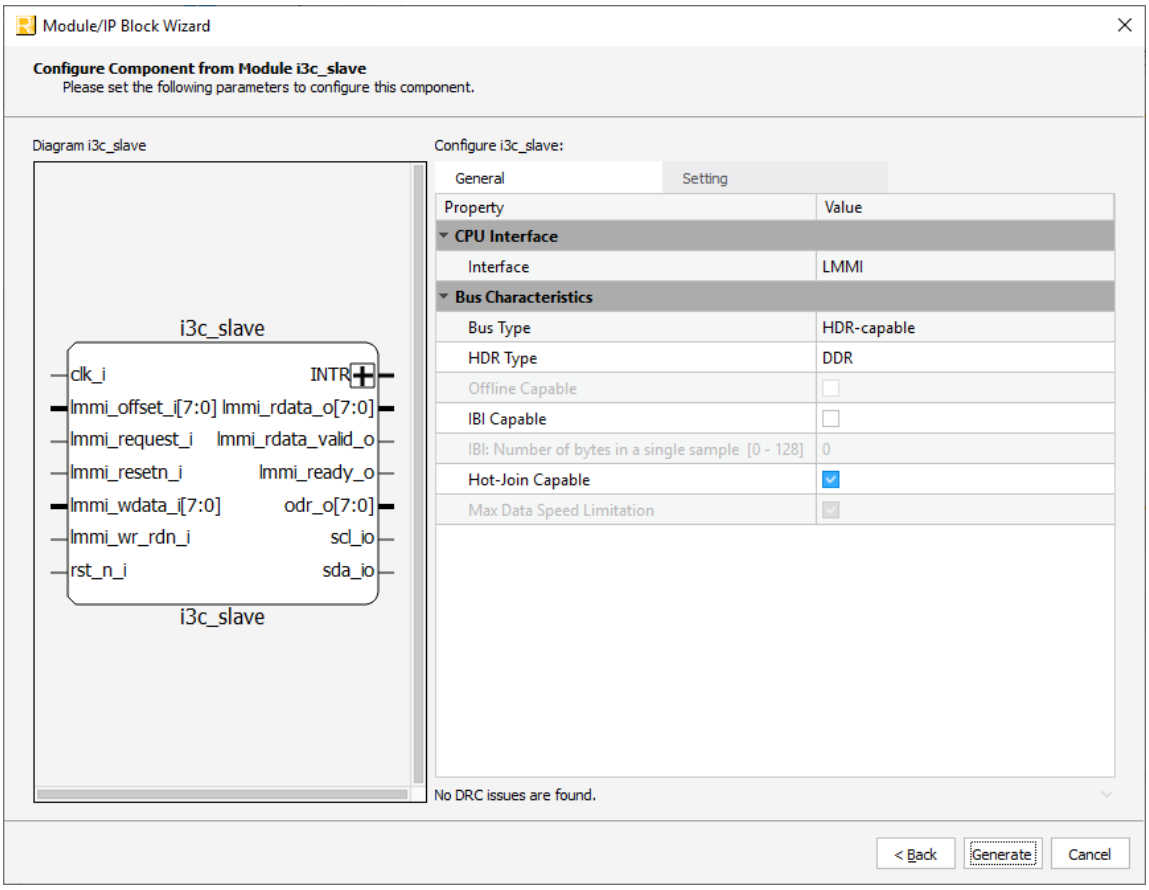

Figure 3.1. Configure Block of I3C Slave Module

3. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results
4. Click the **Finish** button to generate the Verilog file.

The generated I3C Slave IP Core package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.

5. Upon generating desired design, you can synthesize it by clicking **Synthesize Design** located in the top left corner of the screen, as shown in Figure 3.2.

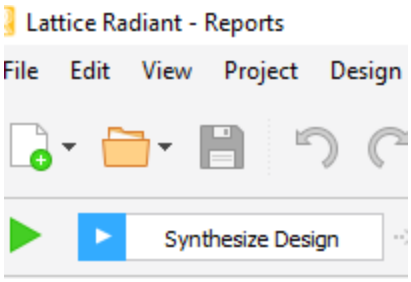

Figure 3.2. Synthesizing Design

3.3. Running Functional Simulation

To run Verilog simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.3.

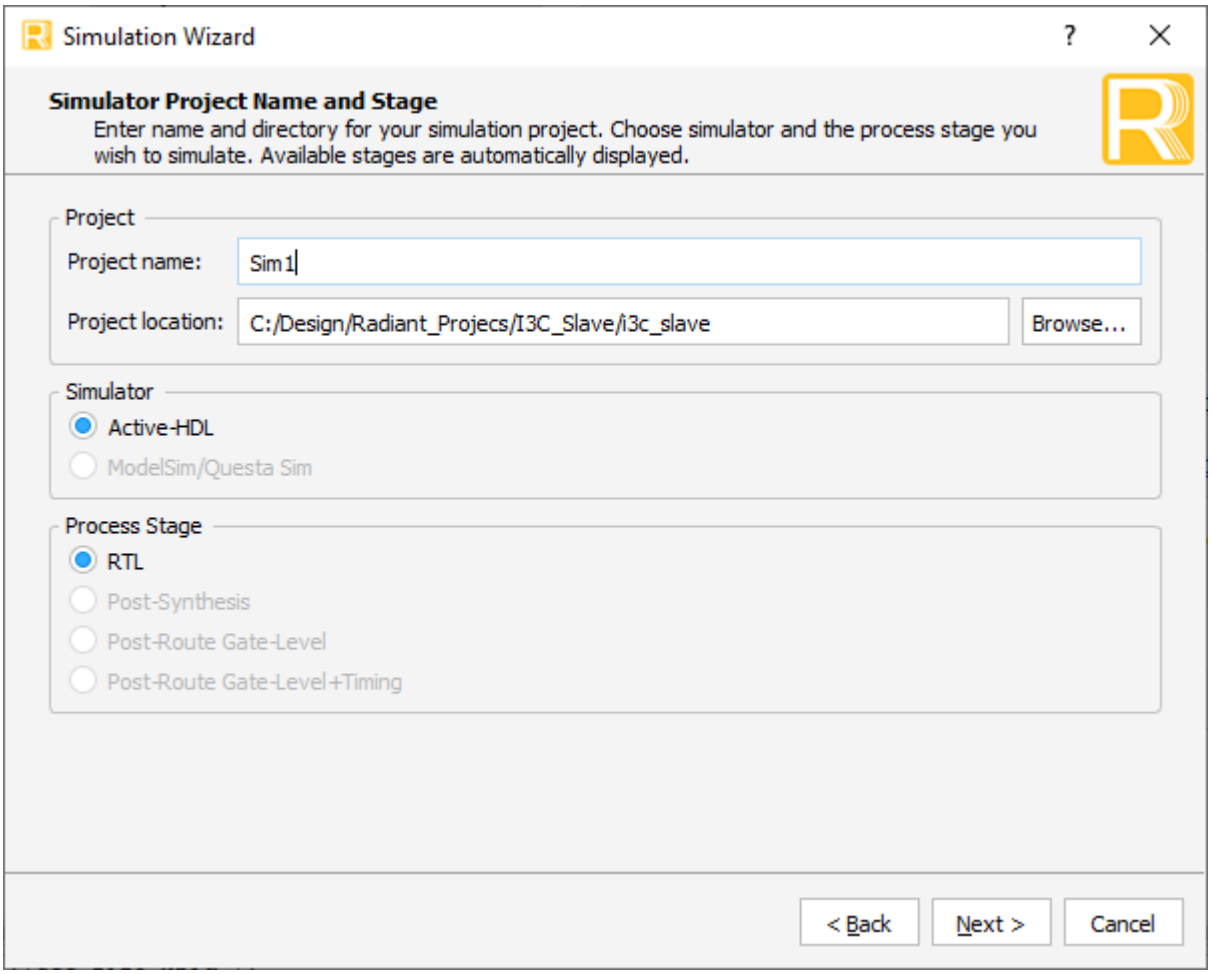

Figure 3.3. Simulation Wizard

2. Double-click **Next** to open the Add and Reorder Source window as shown in Figure 3.4.

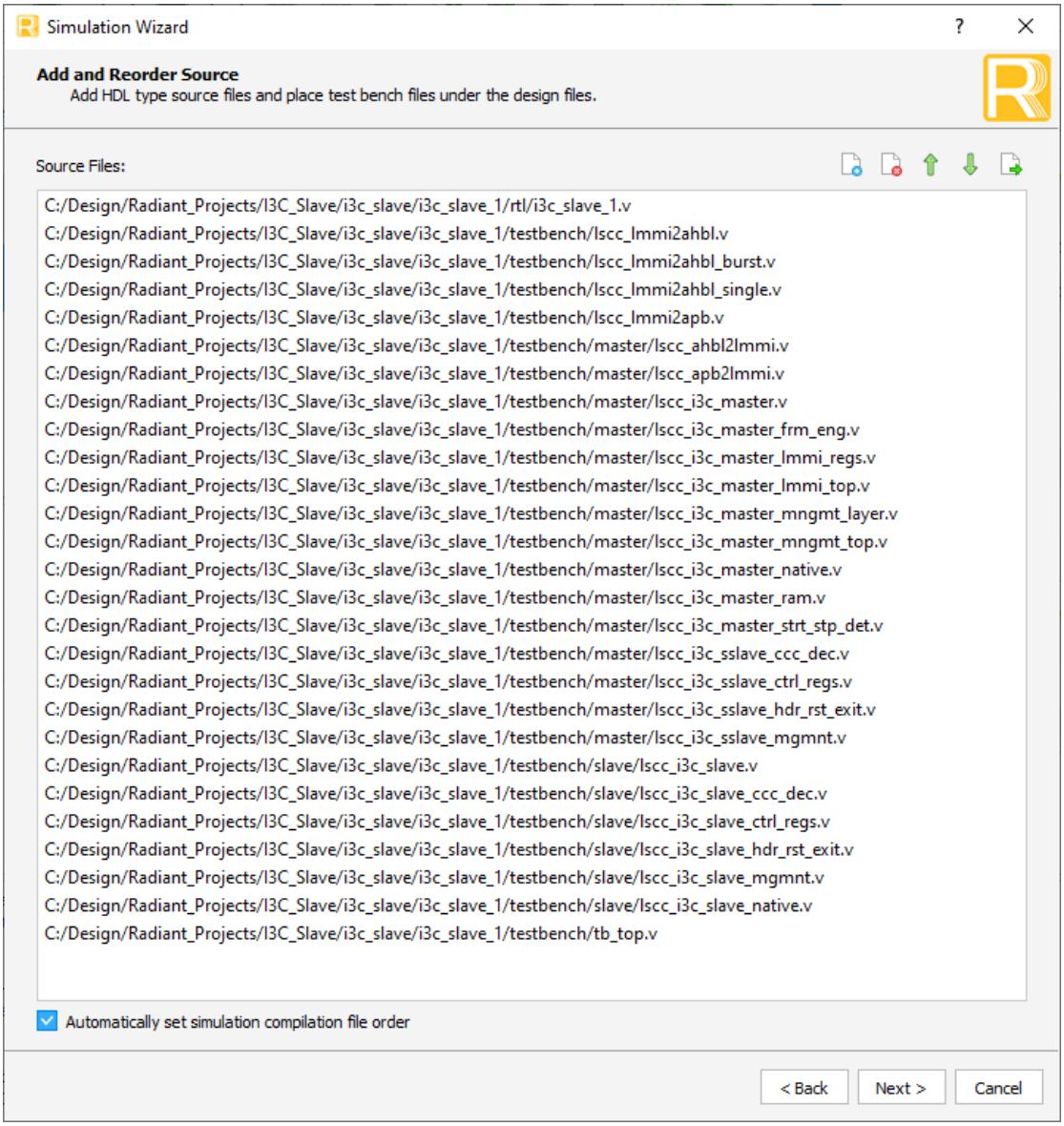

Figure 3.4. Adding and Reordering Source

3. Delete all files except tb_top.v and generated core file (i3c_slave.v in our example.)
4. Click **Next** and **Finish** to run simulation.

3.4. Hardware Evaluation

The I3C Slave IP Core supports Lattice's IP hardware evaluation capability when used with LIFCL and LFD2NX devices. This makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default. To change this setting, go to Project > Active Strategy > LSE/Synplify Pro Settings.

4. Ordering Part Number

The Ordering Part Number (OPN) for this IP Core are the following:

- I3C-S-CNX-U – I3C Slave for CrossLink-NX – Single Design License
- I3C-S-CNX-UT – I3C Slave for CrossLink-NX – Site License
- I3C-S-CTNX-U – I3C Slave for Certus-NX – Single Design License
- I3C-S-CTNX-UT – I3C Slave for Certus-NX – Site License

Appendix A. Resource Utilization

Table A.1 show configuration and resource utilization for LIFCL-40-9BG400I using Synplify Pro of Lattice Radiant Software 2.1.

Table A.1. Resource Utilization

Configuration	Clk Fmax (MHz)*	Slice Registers	LUTs	EBRs
Default	143.596	958	1828	2
Interface = APB, Others = Default	139.353	987	1826	2
Interface = AHBL, Bus Type = SDR only, Others = Default	149.231	870	1465	2

***Note:** Fmax is generated when the FPGA design only contains I^3C Slave IP Core and the target Frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software 2.1 User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, June 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add Certus-NX as supported FPGA family and LFD2NX-40 as targeted device.
Functional Description	Updated Table 2.4.
IP Core Generation, Simulation, and Validation	Updated section content.
Ordering Part Number	Updated this section.
References	Updated this section.

Revision 1.1, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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