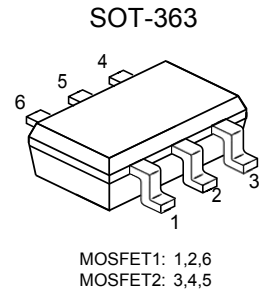
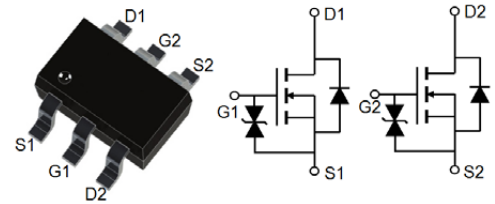


**Dual N-Channel Enhancement Mode Field Effect Transistor**
**FEATURES**

- Low on-resistance:  $V_{DS}=60V, I_D=300mA, R_{DS(ON)} \leq 1.9 \Omega @ V_{GS}=10V$
- High density cell design for low  $R_{DS(ON)}$
- Voltage controlled small signal switch
- High saturation current capability
- Rugged and reliable
- ESD Protection


**MECHANICAL DATA**

- Case: SOT-363
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: 0.3 grams (approximate)


**MAXIMUM RATINGS  $T_A = 25^\circ\text{C}$  unless otherwise noted**

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter	Rating	Unit	
<b>Common Ratings (<math>T_A=25^\circ\text{C}</math> Unless Otherwise Noted)</b>				
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V	
$T_J$	Maximum Junction Temperature	150	$^\circ\text{C}$	
$T_{STG}$	Storage Temperature Range	-50 to 150	$^\circ\text{C}$	
<b>Mounted on Large Heat Sink</b>				
$I_{DM}$	Pulse Drain Current Tested①	$T_A = 25^\circ\text{C}$	0.8	A
$I_D$	Continuous Drain Current	$T_A = 25^\circ\text{C}$	0.3	A
		$T_A = 70^\circ\text{C}$	0.24	
$P_D$	Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	0.3	W
		$T_A = 70^\circ\text{C}$	0.2	
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	400	$^\circ\text{C/W}$	

**Dual N-Channel Enhancement Mode Field Effect Transistor**
**MOSFET ELECTRICAL CHARACTERISTICS  $T_a=25^\circ\text{C}$  unless otherwise specified**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Electrical Characteristics @ <math>T_J = 25^\circ\text{C}</math> (unless otherwise stated)</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current( $T_A=25^\circ\text{C}$ )	$V_{DS}=60V, V_{GS}=0V$	--	--	1	$\mu A$
	Zero Gate Voltage Drain Current( $T_A=125^\circ\text{C}$ )	$V_{DS}=48V, V_{GS}=0V$	--	--	100	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	--	--	$\pm 100$	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance <sup>②</sup>	$V_{GS}=10V, I_D=0.3A$	--	1.9	3	$\Omega$
$R_{DS(ON)}$	Drain-Source On-State Resistance <sup>②</sup>	$V_{GS}=4.5V, I_D=0.2A$	--	2.5	4	$\Omega$
<b>Dynamic Electrical Characteristics @ <math>T_J = 25^\circ\text{C}</math> (unless otherwise stated)</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=30V, V_{GS}=0V,$ $f=1\text{MHz}$	--	12	--	pF
$C_{oss}$	Output Capacitance		--	3.2	--	pF
$C_{rss}$	Reverse Transfer Capacitance		--	0.8	--	pF
$Q_g$	Total Gate Charge	$V_{DS}=30V$ $I_D=0.3A,$ $V_{GS}=10V$	--	0.65	--	nC
$Q_{gs}$	Gate Source Charge		--	0.12	--	nC
$Q_{gd}$	Gate Drain Charge		--	0.21	--	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn on Delay Time	$V_{DD}=30V,$ $I_D=0.3A,$ $R_G=3.3\Omega,$ $V_{GS}=10V$	--	4.5	--	ns
$t_r$	Turn on Rise Time		--	3.1	--	ns
$t_{d(off)}$	Turn Off Delay Time		-	15	--	ns
$t_f$	Turn Off Fall Time		--	3.3	--	ns
<b>Source Drain Diode Characteristics</b>						
$I_{SD}$	Source drain current(Body Diode)	$T_A=25^\circ\text{C}$	--	--	0.2	A
$V_{SD}$	Forward on voltage <sup>②</sup>	$T_J=25^\circ\text{C}, I_{SD}=0.2A,$ $V_{GS}=0V$	--	0.8	1.2	V

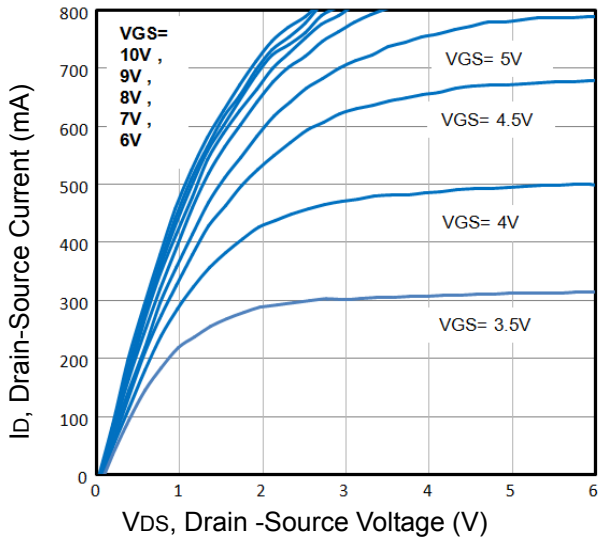
Notes:

① Pulse width limited by maximum allowable junction temperature

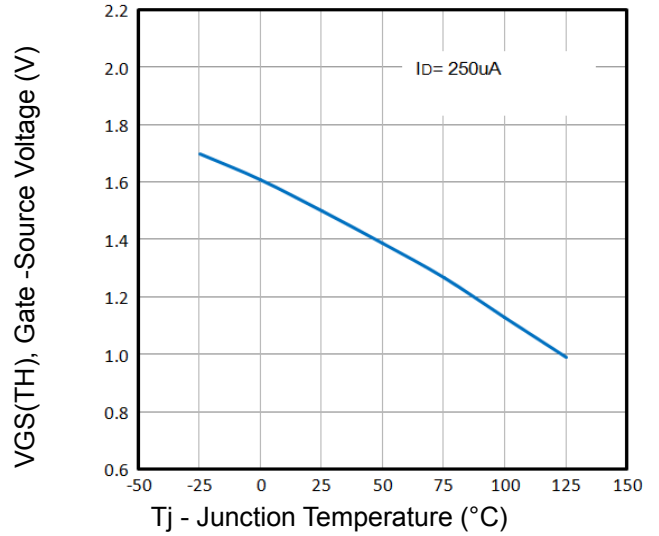
 ② Pulse test ; Pulse width $\leq 300\mu s$ , duty cycle $\leq 2\%$ .

**Dual N-Channel Enhancement Mode Field Effect Transistor**

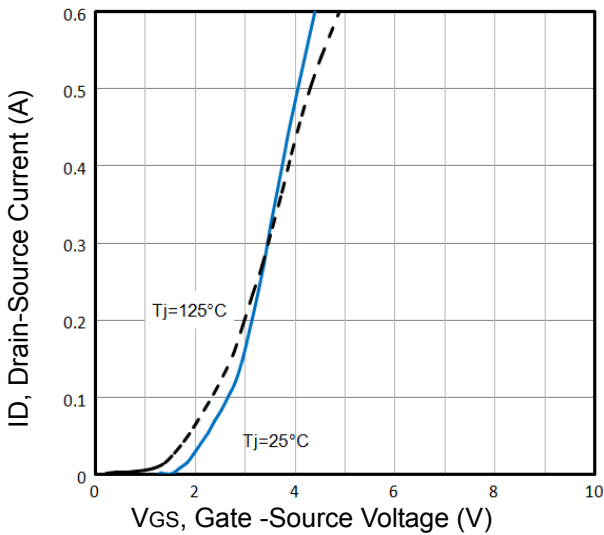
**Typical Characteristics**



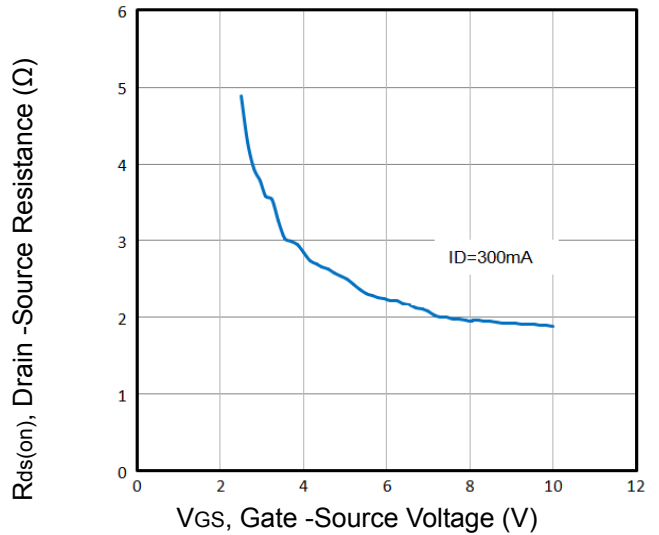
**Fig1.** Typical Output Characteristics



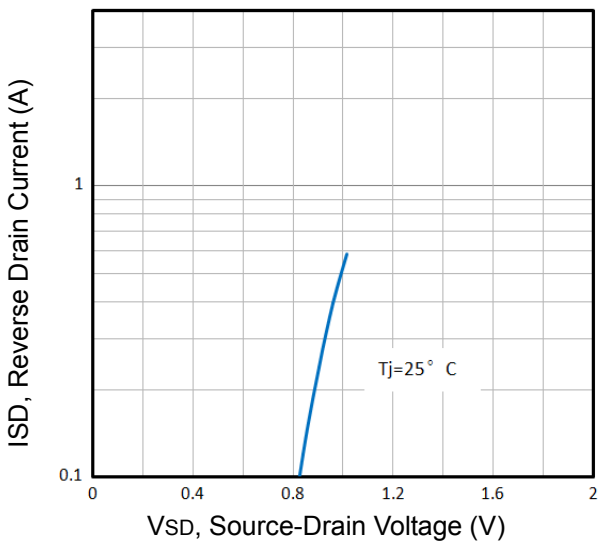
**Fig2.** Normalized Threshold Voltage Vs. Temperature



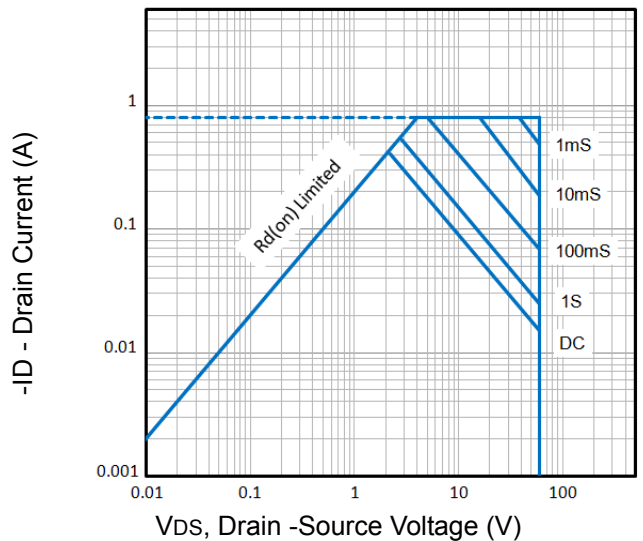
**Fig3.** Typical Transfer Characteristics



**Fig4.** Rds(on) vs Gate-Source Voltage



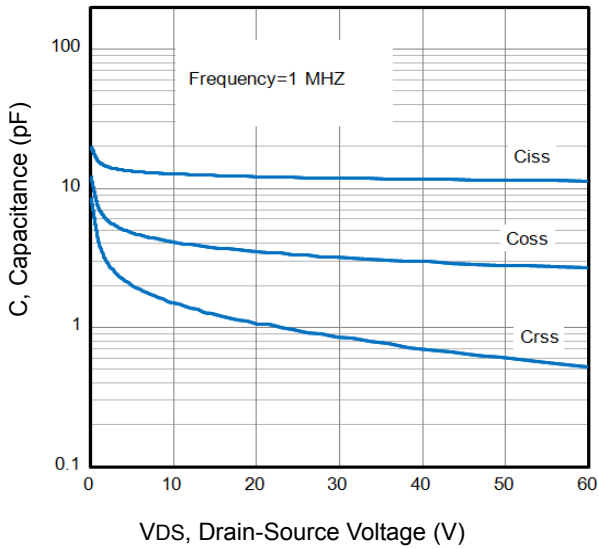
**Fig5.** Typical Source-Drain Diode Forward Voltage



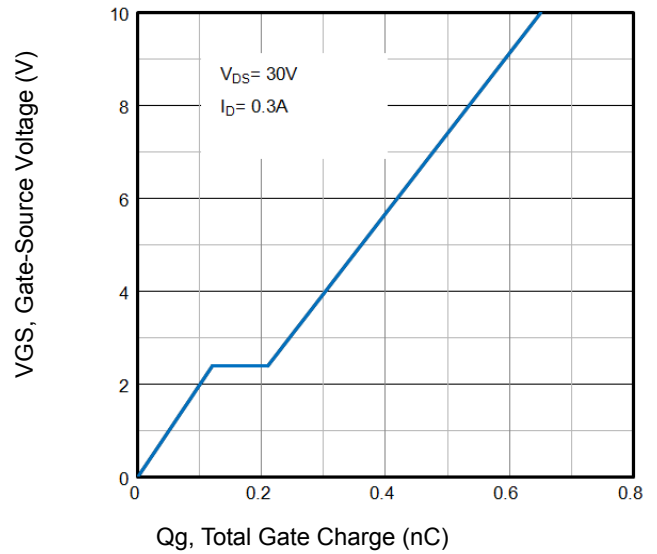
**Fig6.** Maximum Safe Operating Area

**Dual N-Channel Enhancement Mode Field Effect Transistor**

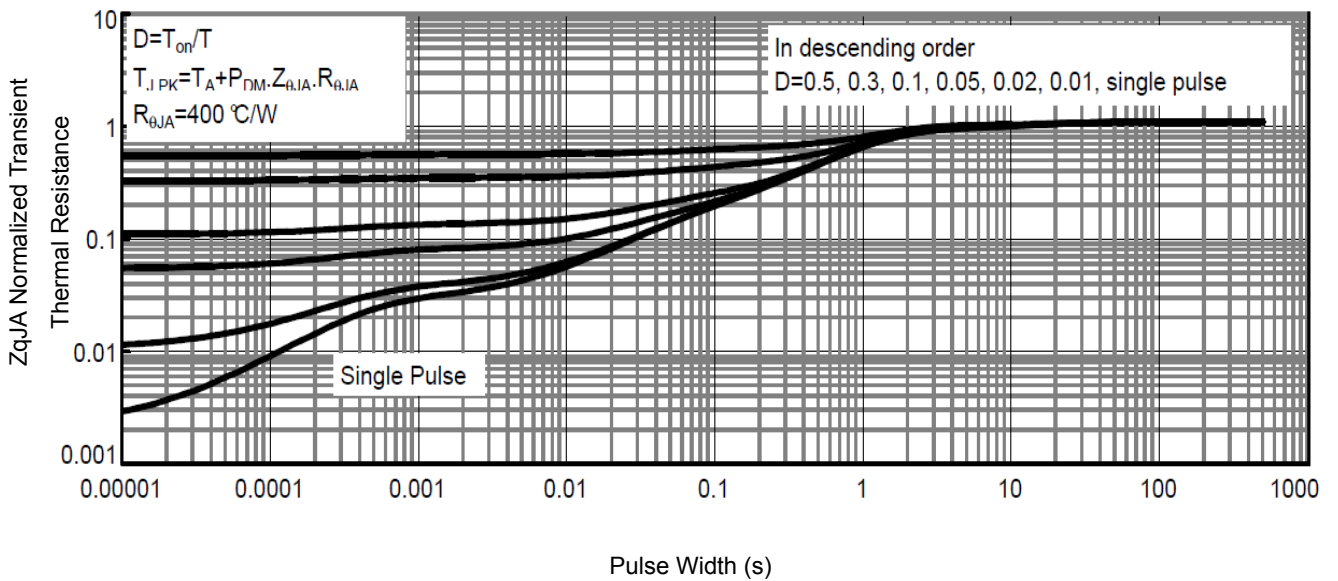
**Typical Characteristics**



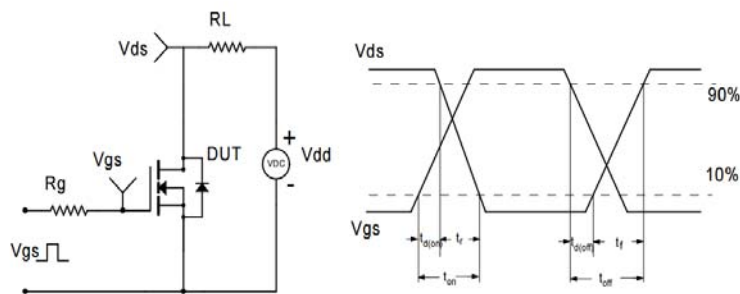
**Fig7.** Typical Capacitance Vs. Drain-Source Voltage



**Fig8.** Typical Gate Charge Vs. Gate-Source Voltage



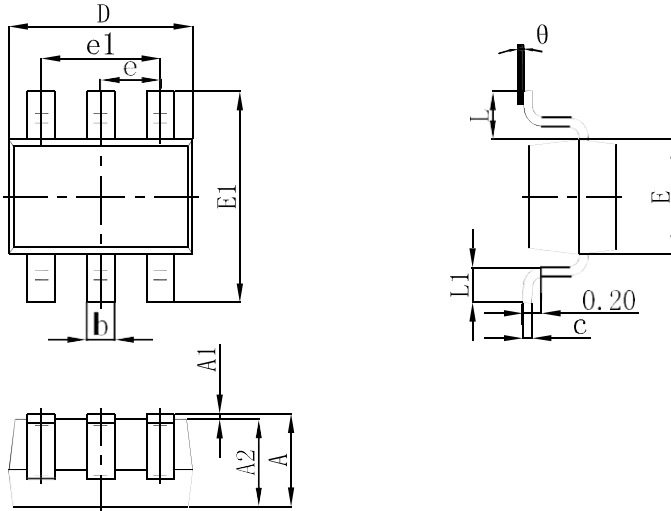
**Fig9.** Normalized Maximum Transient Thermal Impedance



**Fig10.** Switching Time Test Circuit and waveforms

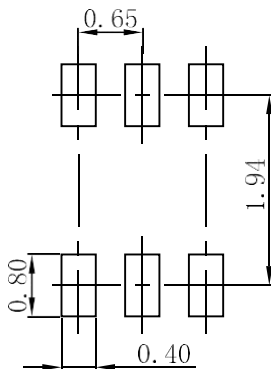
**Dual N-Channel Enhancement Mode Field Effect Transistor**

**SOT-363 Package Outline Dimensions**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.100	0.150	0.004	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.400	0.085	0.094
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

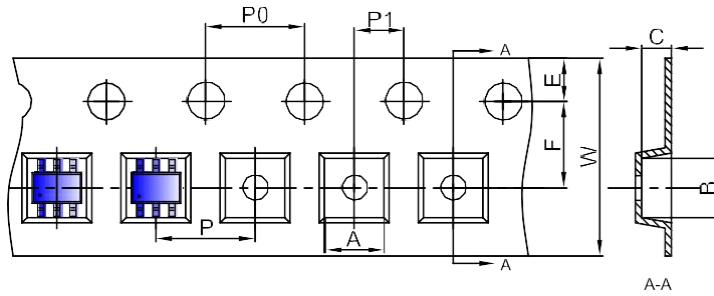
**SOT-363 Suggested Pad Layout**



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ± 0.05mm.  
 3. The pad layout is for reference purposes only.

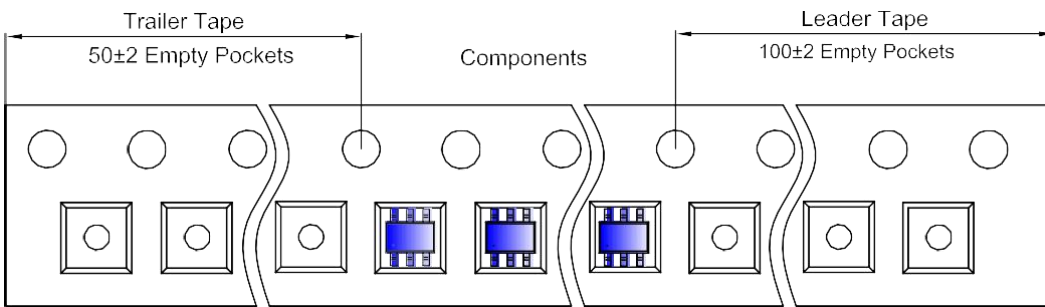
**Dual N-Channel Enhancement Mode Field Effect Transistor**

SOT-363 Embossed Carrier Tape

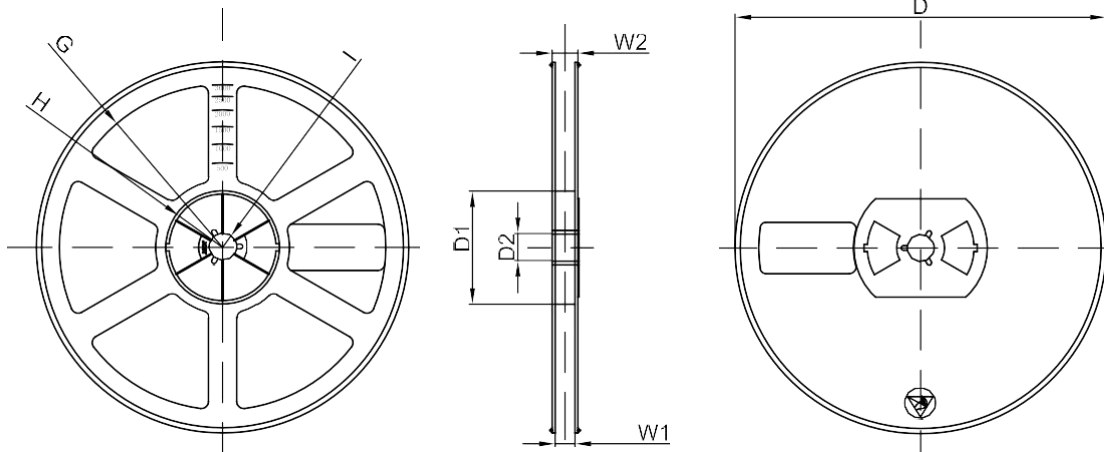


Dimensions are in millimeter										
Pkg type	A	B	C	d	E	F	P0	P	P1	W
SOT-363	2.25	2.55	1.20	Ø1.50	1.75	3.50	4.00	4.00	2.00	8.00

**SOT-363 Tape Leader and Trailer**



**SOT-363 Reel**



Dimensions are in millimeter								
Reel Option	D	D1	D2	G	H	I	W1	W2
7" Dia	Ø178.00	54.40	13.00	R78.00	R25.60	R6.50	9.50	12.30