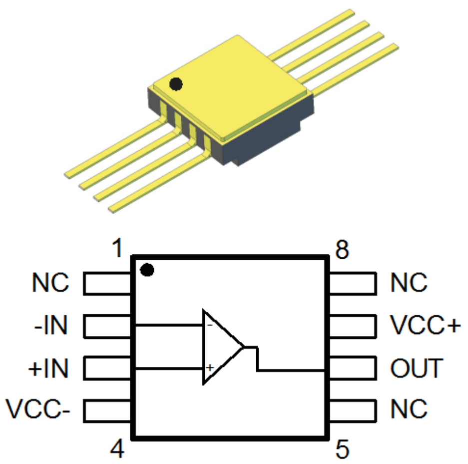
Rad-hard very high-speed comparator

Datasheet - production data

Ceramic Flat-8



The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package

Features

- Propagation time of 7 ns
- Rise/fall time: 1.1 ns on 10 pF
- Low consumption: 1.4 mA
- Single supply: 3 V to 5 V
- 100 krad high-dose rate
- SEL-free up to 120 MeV.cm²/mg
- SET characterized

Applications

- High-speed timing
- High-speed sampling
- Clock recovery
- Clock distribution
- Phase detectors

Description

The RHR801 is a very high-speed single comparator. It is designed to allow very high rise and fall times while drawing a high noise supply rejection. It uses a high-speed complementary BiCMOS process to achieve its very good speed/power ratio and its high tolerance to radiation. The RHR801 is mounted in a hermetic Flat-8 package.

Table 1: Device summary

Parameter	RHR801K1	RHR801K01V
SMD [(1)]	—	5962-10215
Quality level	Engineering model	QML-V flight
Package Mass	Flat-8 0.45 g	
EPPL [(2)]	—	Yes
Temp. range	-55 °C to 125 °C	

Notes:

[(1)]SMD: standard microcircuit drawing

[(2)]EPPL = ESA preferred part list

This is information on a product in full production. www.st.com

Contents

1 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{id}	Differential input voltage (2)	±2	
V_{in} (3)	Input voltage	(V_{cc}^-) - 0.3 V to (V_{cc}^+) + 0.3 V	
T_{stg}	Storage temperature range	-65 to 150	°C
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction-to-ambient (4)	125	°C/W
R_{thjc}	Thermal resistance junction-to-case (4)	40	
ESD	HBM: human body model (5)	3.5	kV
	MM: machine model (6)	0.35	
	CDM: charged device model (7)	0.9	
tlead	Lead temperature (soldering, 10 s)	260	°C

Notes:

(1)V_{CC} is defined as the voltage between the Vcc+ and Vcc- pins. The comparator can be used in single supply (for example, Vcc+ = 5 V, Vcc- = 0 V) or dual supply (for example, Vcc+ = 2.5 V, Vcc- = -2.5 V).

(2)Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. Vid should not exceed ±2 V. Diodes should be placed externally between the inputs should this voltage be beyond this range

(3)If the input voltage goes beyond the rails (above Vcc+ or below Vcc-), the ESD diodes may be activated. It is required in that case to limit the input current to 10 mA with a serial resistor connected on the input.

(4)Short-circuits can cause excessive heating and destructive dissipation. Values are typical.

(5)Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

(6)Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

(7)Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 5	V
V_{ICM}	Common-mode input voltage range	(V_{CC-}) + 0.5 V to (V_{CC+}) - 1.2 V	
T_{oper}	Operating free-air temperature range	-55 to 125	°C

2 Electrical characteristics

Table 4: VCC+ = 3.3 V, VCC- = 0 V (unless otherwise specified)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
Input characteristics (see *Figure 35*)							
V_{IO}	Input offset voltage	V_{ICM} = V_{CC}/2	125°C	-8.0		8.0	mV
			25°C	-7.0	-0.2	7.0	
			-55°C	-8.0		8.0	
V_{TRIP+}	High input threshold	V_{ICM} = V_{CC}/2	125°C	-8.0		8.0	
			25°C	-7.0	1.1	7.0	
			-55°C	-8.0		8.0	
V_{TRIP-}	Low input threshold	V_{ICM} = V_{CC}/2	125°C	-8.0		8.0	
			25°C	-7.0	-1.5	7.0	
			-55°C	-8.0		8.0	
V_{HYST}	Hysteresis	V_{ICM} = V_{CC}/2	25°C	1.5	2.5	4.0	
I_{IB}	Input bias current	V_{ICM} = V_{CC}/2	125°C	-4	-2.2	0.0	µA
			25°C	-5	-2.5	0.0	
			-55°C	-7	-3.5	0.0	
C_{IN}	Input capacitance		25°C		5		pF
Dynamic performances (see *Figure 36*, *Figure 37*, and *Figure 38*)							
T_{PLH}	Logic "0" to logic "1" propagation time	150 mV step, C_L = 10 pF, 50 mV overdrive, V_{ICM} = V_{CC}/2	125°C	7.0	8.8	12.0	ns
			25°C	6.0	8.1	9.5	
			-55°C	6.0	8.1	9.5	
		200 mV step, C_L = 10 pF, 100 mV overdrive, V_{ICM} = V_{CC}/2	125°C	6.5	8.0	10.5	
			25°C	5.5	7.8	9.0	
			-55°C	5.5	7.8	9.0	
T_{PHL}	Logic "1" to logic "0" propagation time	150 mV step, C_L = 10 pF, 50 mV overdrive, V_{ICM} = V_{CC}/2	125°C	7.0	9.0	12.0	
			25°C	6.0	8.3	9.5	
			-55°C	6.0	8.3	9.5	
		200 mV step, C_L = 10 pF, 100 mV overdrive, V_{ICM} = V_{CC}/2	125°C	6.5	7.9	10.5	
			25°C	5.5	7.7	9.0	
			-55°C	5.5	7.7	9.0	
T_R	Output rise time 20 % to 80 %	200 mV step, C_L =10 pF	25°C		1.4		
T_F	Output fall time 80 % to 20 %	200 mV step, C_L = 10 pF	25°C		1.4		ns
F_{MAX}	Maximum input frequency	V_{in} = 1 V_{P-P} sine wave, C_L = 10 pF, output duty cycle between 45 % and 55 %	125°C	60	74		MHz
			25°C	55	72		
			-55°C	50	68		
0							

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
Output characteristics							
V_{OH}	Logic "1" voltage	I_{source} = 3.3 mA	125°C	3.00	3.10	3.30	V
			25°C	3.05	3.14	3.30	
			-55°C	3.10	3.18	3.30	
V_{OL}	Logic "0" voltage	I_{sink} = -3.3 mA	125°C	0	200	300	mV
			25°C	0	170	250	
			-55°C	0	150	200	
I_{sink}	Output sink current	$V_{out} = V_{CC+}$	125°C	14	17	20	mA
			25°C	18	20	22	
			-55°C	19	22	26	
I_{source}	Output source current	$V_{out} = V_{CC-}$	125°C	17	20	23	
			25°C	20	22	25	
			-55°C	22	25	29	
Power supply							
I_{CC-H}	High output supply current	No load, V_{ID} = 0.1 V	125°C	1.40	1.55	2.10	mA
			25°C	1.20	1.44	1.60	
			-55°C	0.95	1.13	1.30	
I_{CC-L}	Low output supply current	No load, V_{ID} = -0.1 V	125°C	1.60	1.75	2.3	
			25°C	1.30	1.63	1.80	
			-55°C	1.00	1.30	1.50	
SVR	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 3 to 3.6 V, V_{ICM} = 1.65 V	125°C	42	65		dB
			25°C	55	70		
			-55°C	45	65		
CMRR	Common-mode rejection ratio ($\Delta V_{ic}/\Delta V_{io}$)	V_{ICM} = 0.5 V to V_{CC} -1.2 V	125°C	50	95		
			25°C	70	80		
			-55°C	60	85		

Table 5: VCC+ = 5 V, VCC- = 0 V (unless otherwise specified)

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
Input characteristics (see *Figure 35*)							
V_{IO}	Input offset voltage	$V_{ICM} = V_{CC}/2$	125°C	-8.0		8.0	mV
			25°C	-7.0	-0.2	7.0	
			-55°C	-8.0		8.0	
V_{TRIP+}	High input threshold	$V_{ICM} = V_{CC}/2$	125°C	-8.0		8.0	
			25°C	-7.0	1.1	7.0	
			-55°C	-8.0		8.0	
V_{TRIP-}	Low input threshold	$V_{ICM} = V_{CC}/2$	125°C	-8.0		8.0	
			25°C	-7.0	-1.5	7.0	
			-55°C	-8.0		8.0	
V_{HYST}	Hysteresis	$V_{ICM} = V_{CC}/2$	25°C	1.5	2.5	4.0	

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
I_{IB}	Input bias current	$V_{ICM} = V_{CC}/2$	125°C	-4	-2.2	0.0	µA
			25°C	-5	-2.5	0.0	
			-55°C	-7	-3.5	0.0	
C_{IN}	Input capacitance		25°C		5		pF
Dynamic performances (see *Figure 36*, *Figure 37*, and *Figure 38*)							
T_{PLH}	Logic "0" to logic "1" propagation time	150 mV step, C_L = 10 pF, 50 mV overdrive, $V_{ICM} = V_{CC}/2$	125°C	6.0	7.9	10	ns
			25°C	6.0	8.1	9.5	
			-55°C	6.0	8.1	9.5	
		200 mV step, C_L = 10 pF, 100 mV overdrive, $V_{ICM} = V_{CC}/2$	125°C	6.5	8.0	10.5	
			25°C	5.5	7.8	9.0	
			-55°C	5.5	7.8	9.0	
T_{PHL}	Logic "1" to logic "0", propagation time	150 mV step, C_L = 10 pF, 50 mV overdrive, $V_{ICM} = V_{CC}/2$	125°C	7.0	9.0	12.0	
			25°C	6.0	8.3	9.5	
			-55°C	6.0	8.3	9.5	
		200 mV step, C_L = 10 pF, 100 mV overdrive, $V_{ICM} = V_{CC}/2$	125°C	6.5	7.9	10.5	
			25°C	5.5	7.7	9.0	
			-55°C	5.5	7.7	9.0	
T_R	Output rise time 20 % to 80 %	200 mV step, C_L = 10 pF	25°C		1.4		
T_F	Output fall time 80 % to 20 %	200 mV step, C_L = 10 pF	25°C		1.4		
F_{MAX}	Maximum input frequency	V_{in} = 1 V_{P-P} sine wave, C_L = 10 pF, output duty cycle between 45 % and 55 %	125°C	60	74		MHz
			25°C	55	72		
			-55°C	50	68		
0							
Output characteristics							
V_{OH}	Logic "1" voltage	I_{source} = 5 mA	125°C	4.60	4.70	5.00	V
			25°C	4.70	4.83	5.00	
			-55°C	4.80	4.87	5.00	
V_{OL}	Logic "0" voltage	I_{sink} = -5 mA	125°C	0	240	400	mV
			25°C	0	200	300	
			-55°C	0	180	200	
I_{sink}	Output sink current	$V_{out} = V_{CC+}$	125°C	25	30	35	mA
			25°C	30	35	40	
			-55°C	30	40	45	
I_{source}	Output source current	$V_{out} = V_{CC-}$	125°C	35	40	45	
			25°C	40	45	50	
			-55°C	45	50	55	

Symbol	Parameter	Test conditions	Temp.	Min.	Typ.	Max.	Unit
Power supply							
I_{CC-H}	High output supply current	No load, V_{ID} = 0.1 V	125°C	1.50	1.84	2.30	mA
			25°C	1.30	1.59	1.80	
			-55°C	1.00	1.25	1.50	
I_{CC-L}	Low output supply current	No load, V_{ID} = -0.1 V	125°C	1.80	2.10	2.50	
			25°C	1.50	1.81	2.00	
			-55°C	1.20	1.43	1.70	
SVR	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 4.5 to 5 V, V_{ICM} = 2.375 V	125°C	50	75		dB
			25°C	60	80		
			-55°C	50	75		
CMRR	Common-mode rejection ratio ($\Delta V_{ic}/\Delta V_{io}$)	V_{ICM} = 0.5 V to V_{CC} -1.2 V	125°C	60	75		
			25°C	70	80		
			-55°C	60	75		

3 Electrical characteristic curves

Figure 1: ICC drift vs. radiation dose, high-dose rate

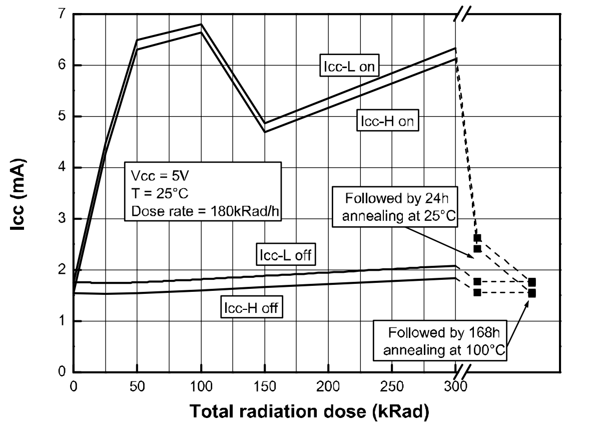


Figure 2: ICC drift vs. radiation dose, low-dose rate

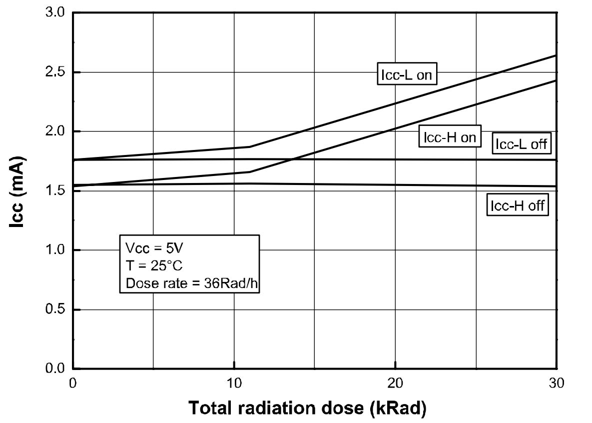


Figure 3: VIO histogram at VCC = 3.3 V

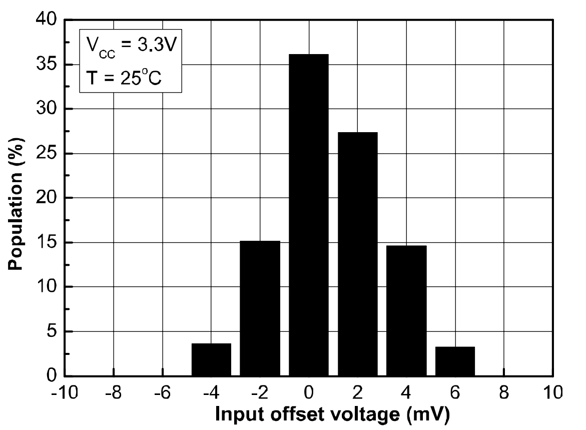


Figure 4: VHYST histogram at VCC = 3.3 V

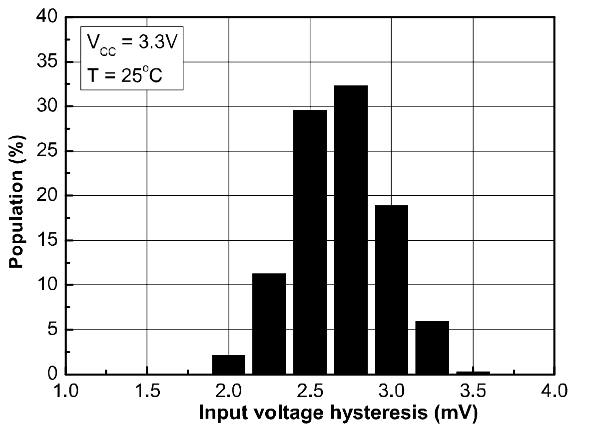


Figure 5: VIO histogram at VCC = 5 V

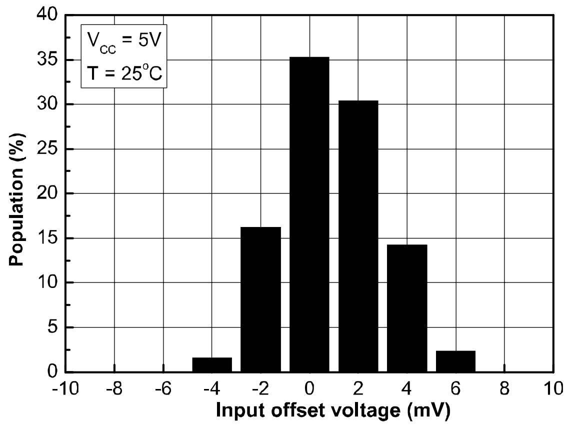


Figure 6: VHYST histogram at VCC = 5 V

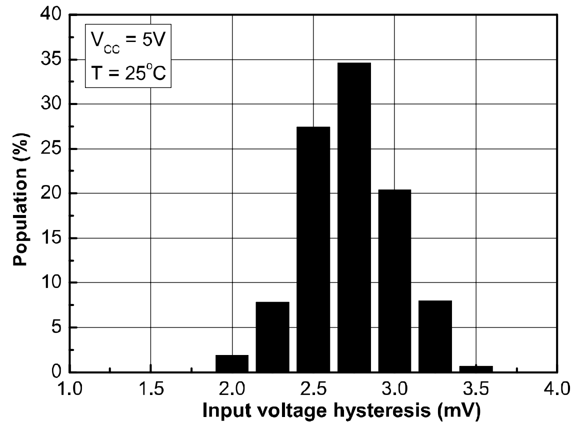


Figure 7: VIO vs. temperature

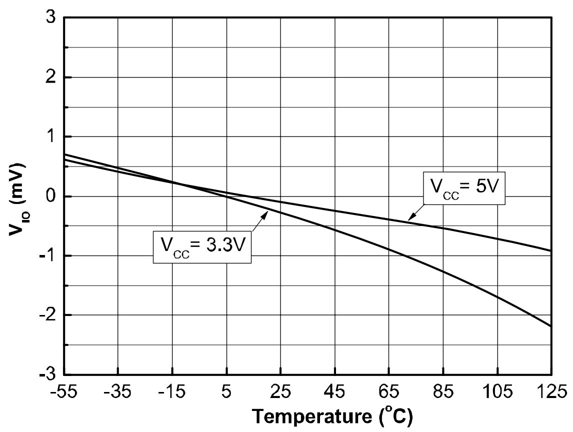


Figure 8: VHYST vs. temperature

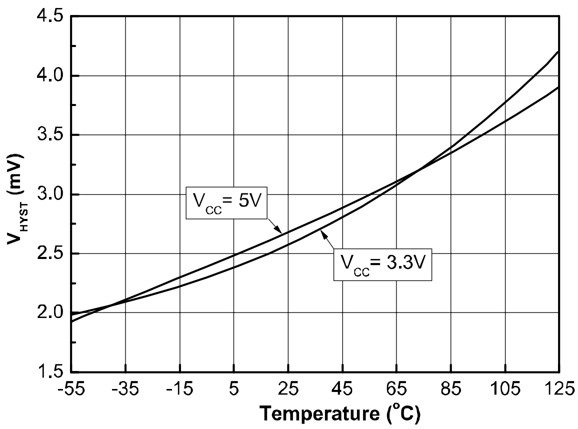


Figure 9: VIO vs. VCC

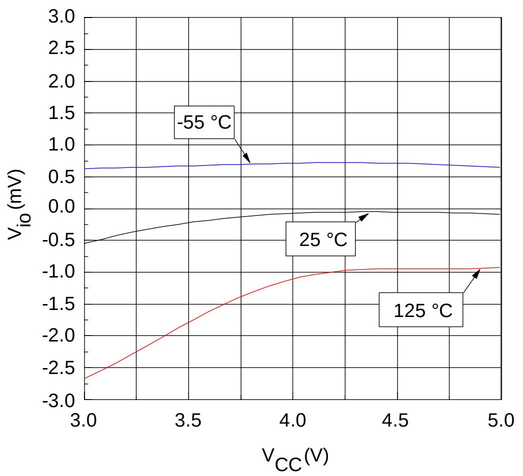


Figure 10: VHYST vs. VCC

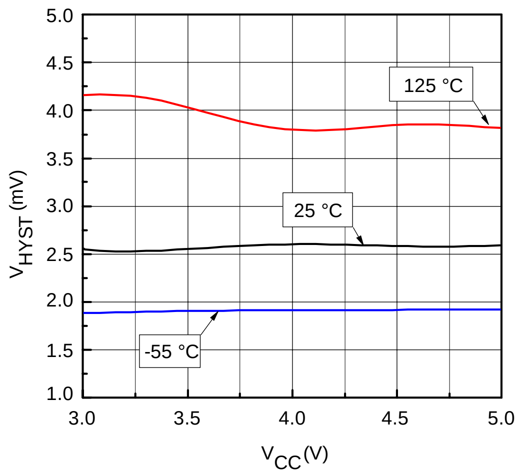


Figure 11: ICCL vs. VCC

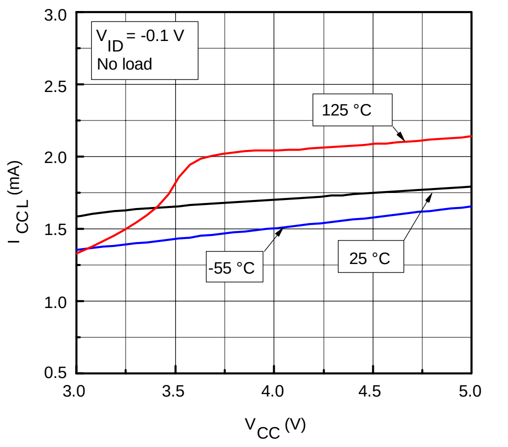


Figure 12: ICCH vs. VCC

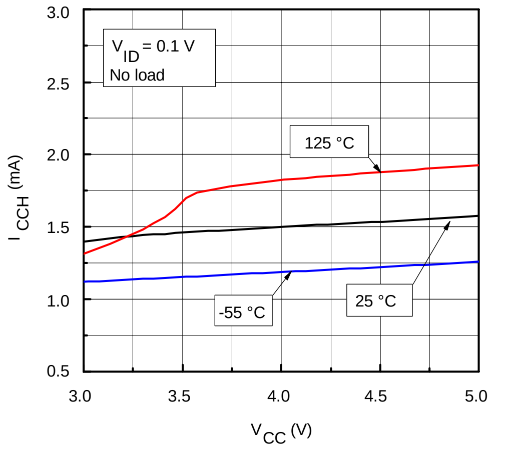


Figure 13: ICC vs. temperature

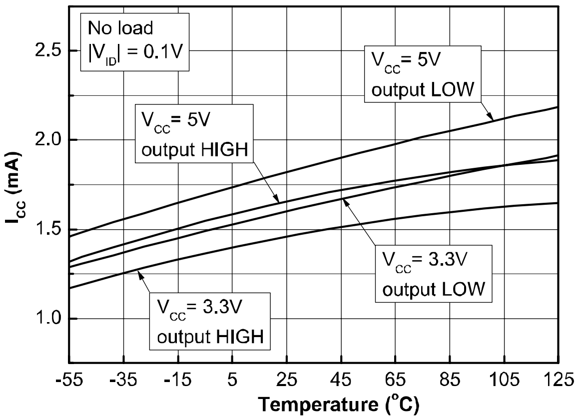


Figure 14: IIB vs. VID

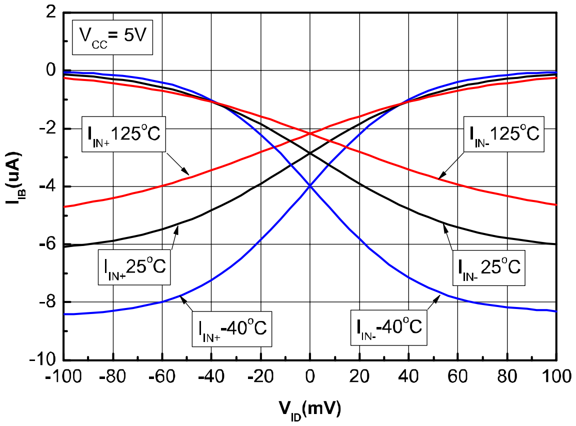


Figure 15: IIB vs. temperature

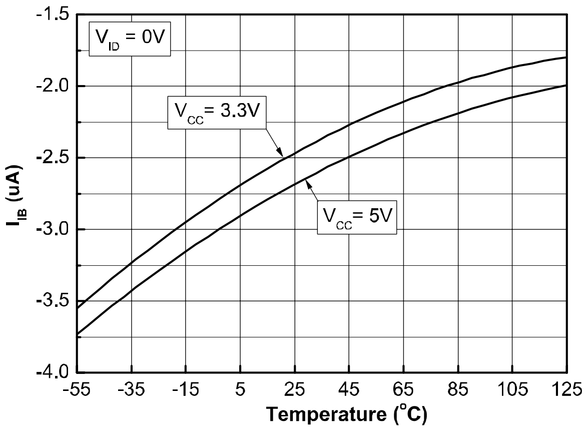


Figure 16: IOUT vs. temperature

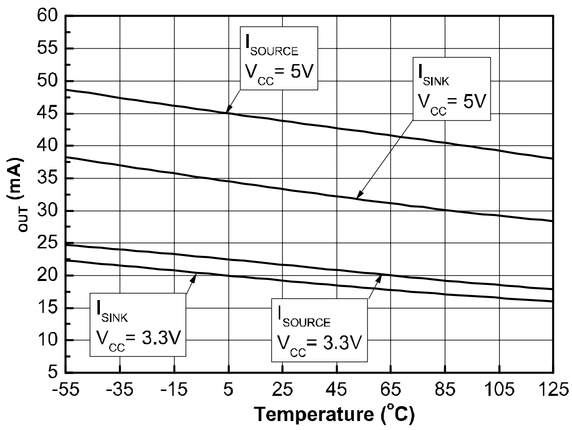


Figure 17: VOUT vs. ISINK at VCC = 3.3 V

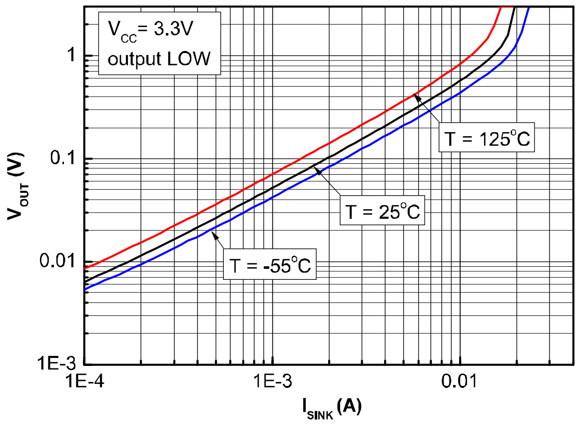


Figure 18: VDROP vs. ISOURCE at VCC = 3.3 V

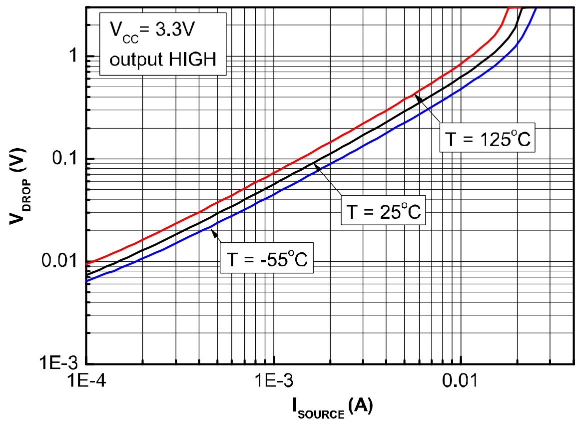


Figure 19: VOUT vs. ISINK at VCC = 5 V

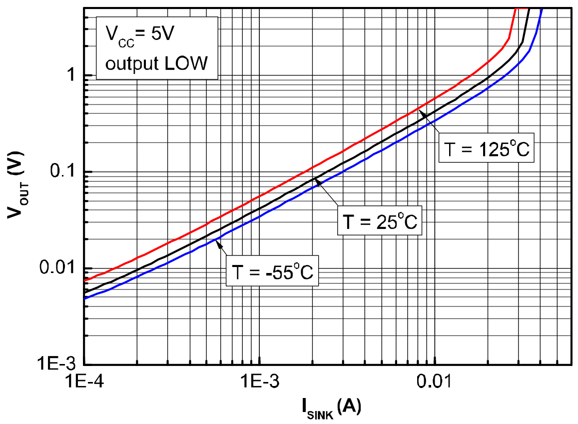


Figure 20: VDROP vs. ISOURCE at VCC = 5 V

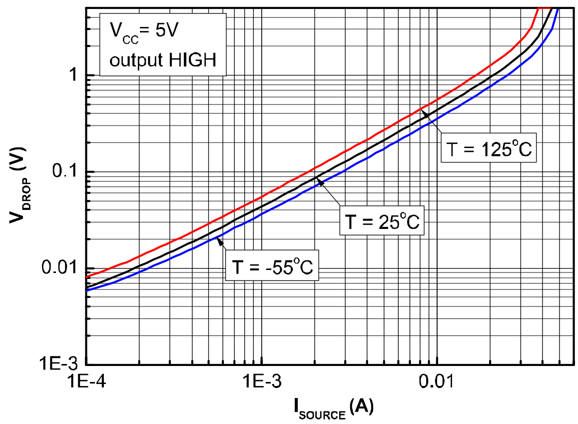


Figure 21: TPD vs. VOV at VCC = 3.3 V

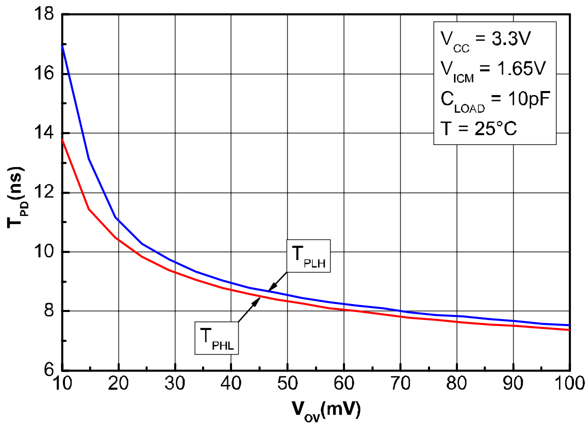


Figure 22: TPD vs. VOV at VCC = 5 V

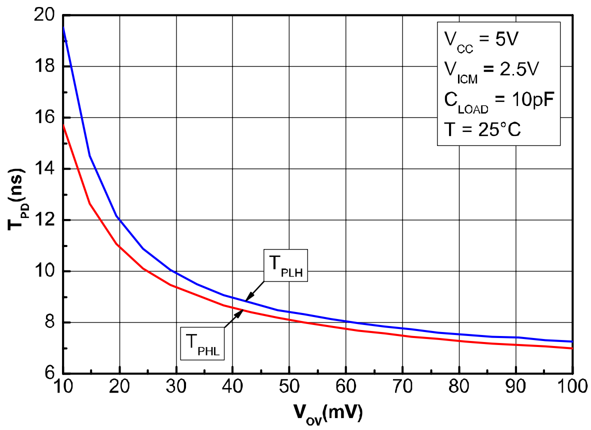


Figure 23: TPLH vs. VCC

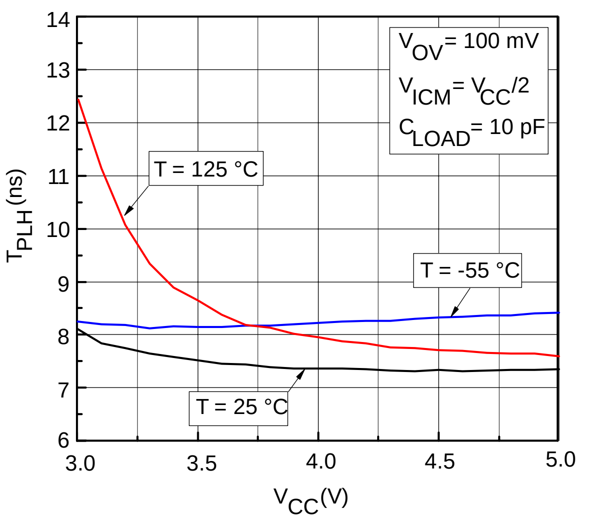


Figure 24: TPHL vs. VCC

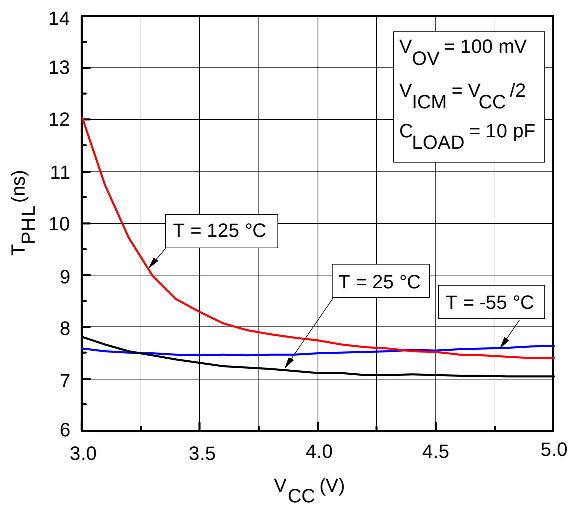


Figure 25: TPD vs. temperature, VOV = 50 mV

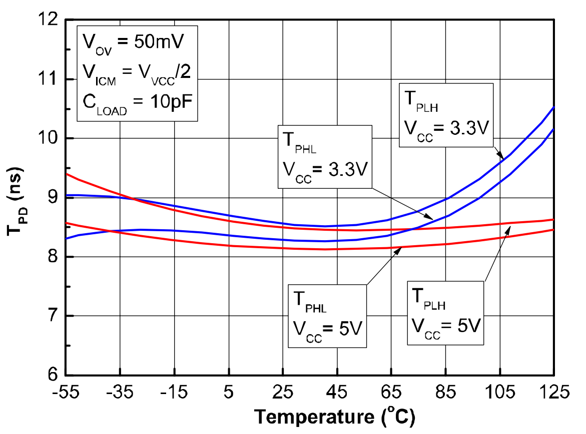


Figure 26: TPD vs. temperature, VOV = 100 mV

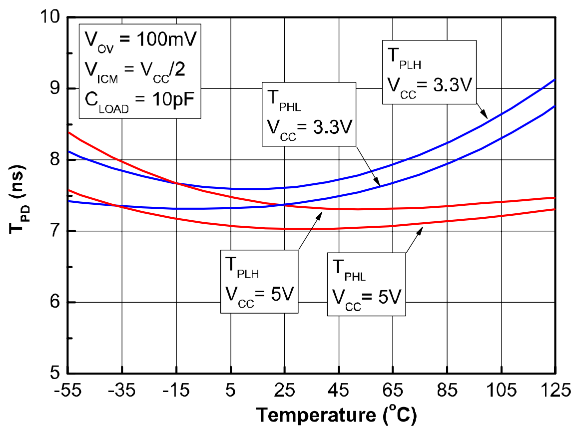


Figure 27: TPLH vs. CL at VCC = 3.3 V

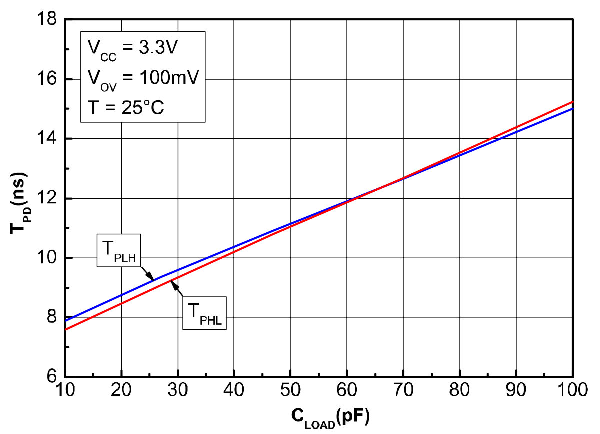


Figure 28: TPHL vs. CL at VCC = 5 V

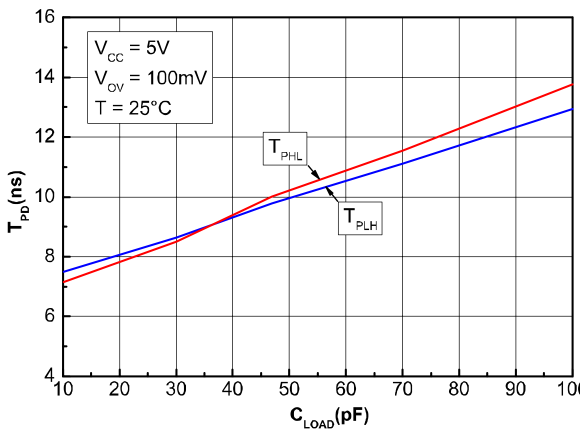


Figure 29: Rise time vs. CL

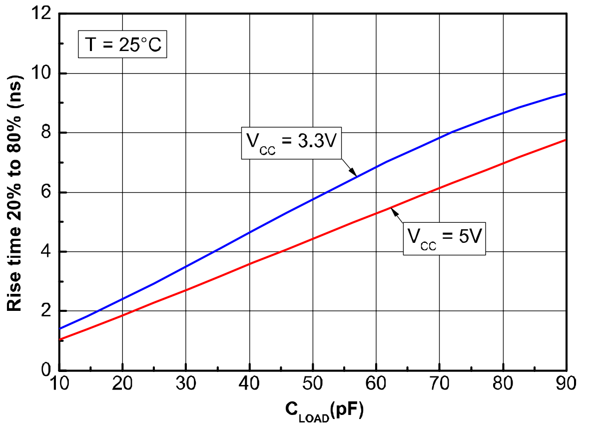


Figure 30: Fall time vs. CL

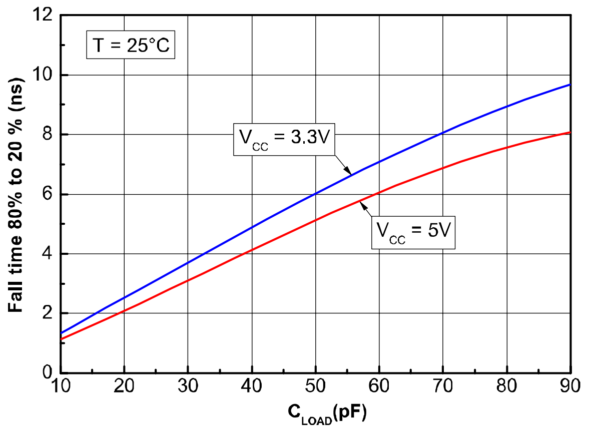


Figure 31: Eye diagram for data rate 100 Mbit/s, test pattern PRBS7, CL = 10 pF and VCC = 3.3 V

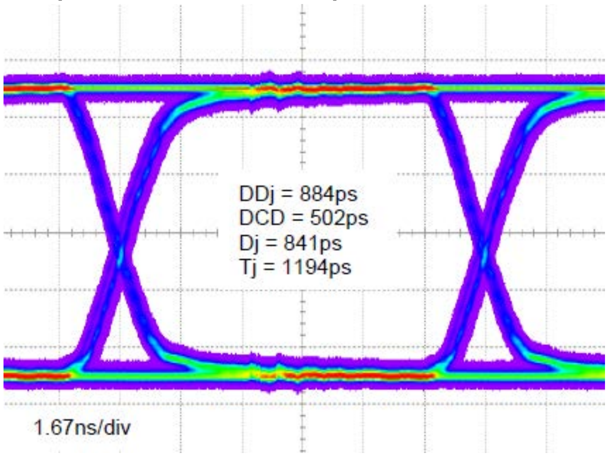


Figure 32: Eye diagram for data rate 100 Mbit/s, test pattern PRBS7, CL = 10 pF and VCC = 5 V

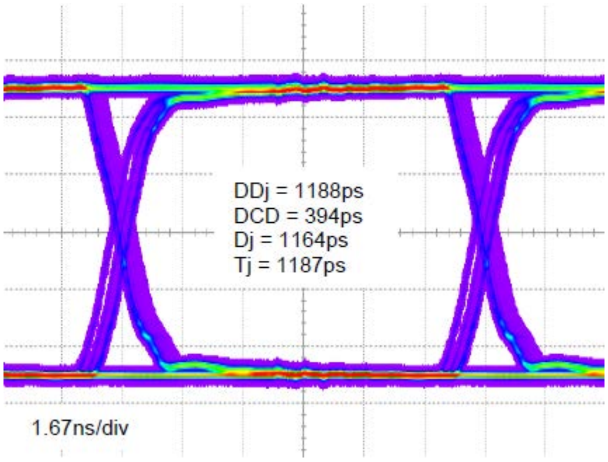


Figure 33: Eye diagram for data rate 200 Mbit/s, test pattern PRBS7, CL = 10 pF and VCC = 3.3 V

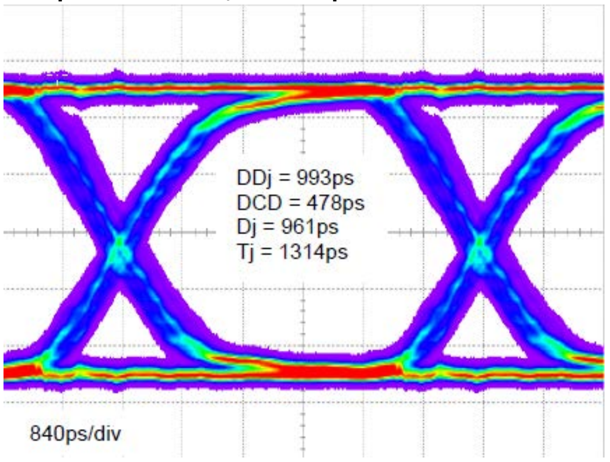
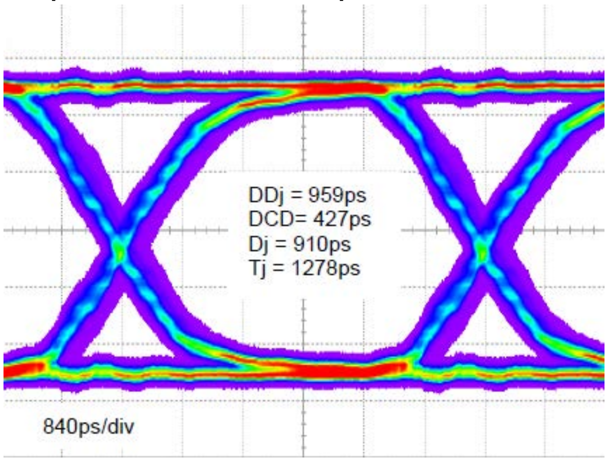


Figure 34: Eye diagram for data rate 200 Mbit/s, test pattern PRBS10, CL = 10 pF and VCC = 3.3 V



4 Radiations

4.1 Introduction

Table 6 summarizes the radiation performance of the RHF310.

Table 6: Radiations

Type	Characteristics	Value	Unit
TID	180 krad/h high-dose rate (50 rad/sec) up to:	100	krad
	36 rad/h low-dose rate (0.01 rad/sec) up to:	30 (1)	
Heavy-ions	SEL immunity up to: (at 125 °C, with a particle angle of 60 °)	120	MeV.cm²/mg
	SEL immunity up to: (at 125 °C, with a particle angle of 0 °)	60	
	SET (at 25 °C)	Characterized	

Notes:

(1) Using the comparator beyond the maximum operating voltage (5 V) may result in significant overconsumption following low-dose rate radiation at 5.5 V (30 krad at 36 rad/h) and could lead to functional interrupt above 30 krad at 36 rad/h

4.2 Total ionizing dose (TID)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHR801 is RHA QML-V tested and characterized in full compliance with the MIL-STD-883 specification, both below 10 mrad/s and between 50 and 300 rad/s.

These parameters are shown in *Table 7* and *Table 8* (high-dose rate) and *Table 9* and *Table 10* (low-dose rate), as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.
- Each wafer lot is tested at both high and low dose rates, in the worst bias case condition, based on the results obtained during the initial qualification.

Table 7: Drift after 300 krad and after annealing, during 24 h @ 25 °C and 168 h at 100 °C, 180 krad/h high-dose rate, VCC+ = 3.3 V, VCC- = 0 V, T = 25 °C, (unless otherwise specified)

Symbol	Min	Typ	Max	Unit
Delta Vio	-0.72	-0.03	0.43	mV
Delta Vtrip+	-0.72	0.01	0.52	
Delta Vtrip-	-0.88	-0.08	0.61	
Delta Iib	-0.51	-0.11	0.15	µA
Delta Tplh (150 mV step)	0.06	0.28	0.49	ns
Delta Tplh (200 mV step)	-0.01	0.22	0.53	
Delta Tphl (150 mV step)	-0.03	0.14	0.40	
Delta Tphl (200 mV step)	-0.02	0.15	0.36	
Delta Tr	0.04	0.11	0.21	
Delta Tf	-0.20	-0.07	0.12	
Delta Fmax	-16.00	-2.70	4.00	MHz
Delta ICC-H	-0.01	0.01	0.02	mA
Delta ICC-L	0.00	0.01	0.03	
Delta VOH	0.00	0.00	0.00	mV
Delta VOL	-4.68	-0.52	4.68	
Delta Isink	-0.54	-0.03	0.28	mA
Delta Isource	-0.39	-0.33	-0.28	
Delta SVR	-10.30	-1.86	7.61	dB
Delta CMRR	-3.67	-0.10	7.40	

Table 8: Drift after 300 krad and after annealing, during 24 h @ 25 °C and 168 h at 100 °C, 180 krad/h high-dose rate, VCC+ = 5 V, VCC- = 0 V, T = 25 °C, (unless otherwise specified)

Symbol	Min	Typ	Max	Unit
Delta Vio	-0.89	-0.01	0.68	mV
Delta Vtrip+	-0.92	-0.02	0.68	
Delta Vtrip-	-0.86	0.00	0.68	
Delta Iib	-0.84	-0.24	0.25	µA
Delta Tplh (150 mV step)	-0.16	0.08	0.27	ns
Delta Tplh (200 mV step)	-0.10	0.15	0.51	
Delta Tphl (150 mV step)	0.01	0.13	0.28	
Delta Tphl (200 mV step)	-0.16	0.06	0.33	
Delta Tr	0.00	0.04	0.06	
Delta Tf	-0.11	-0.01	0.09	
Delta Fmax	-5.00	-0.90	3.00	MHz
Delta ICC-H	-0.02	0.00	0.02	mA
Delta ICC-L	-0.01	0.00	0.02	
Delta VOH	0.00	0.00	0.00	mV
Delta VOL	-6.11	-1.59	3.32	
Delta Isink	-0.52	0.00	0.36	mA
Delta Isource	-0.26	-0.18	-0.13	
Delta SVR	-10.39	0.74	11.40	dB
Delta CMRR	-0.68	2.79	5.60	

Table 9: Drift after 30 krad, 36 rad/h low-dose rate, VCC+ = 3.3 V, VCC- = 0 V, T = 25 °C, (unless otherwise specified)

Symbol	Min	Typ	Max	Unit
Delta Vio	-0.36	0.07	0.57	mV
Delta Vtrip+	-0.64	0.11	0.80	
Delta Vtrip-	-0.50	0.02	0.33	
Delta Iib	-0.23	-0.02	0.23	µA
Delta Tplh (150 mV step)	-0.20	-0.01	0.20	ns
Delta Tplh (200 mV step)	-0.15	-0.01	0.15	
Delta Tphl (150 mV step)	-0.10	0.04	0.20	
Delta Tphl (200 mV step)	-0.10	0.02	0.15	
Delta Tr	-0.04	0.02	0.08	
Delta Tf	-0.14	-0.05	0.04	
Delta Fmax	-3.00	0.84	4.00	MHz
Delta ICC-H	-0.01	0.10	0.42	mA
Delta ICC-L	-0.01	0.10	0.43	
Delta VOH	-0.01	0.00	0.00	mV
Delta VOL	-5.11	-3.25	-1.45	
Delta Isink	0.14	0.23	0.32	mA
Delta Isource	-0.03	0.06	0.15	
Delta SVR	-9.54	-0.35	6.02	dB
Delta CMRR	-7.96	1.13	7.80	

Table 10: Drift after 30 krad, 36 rad/h low-dose rate, VCC+ = 5 V, VCC- = 0 V, T = 25 °C, (unless otherwise specified)

Symbol	Min	Typ	Max	Unit
Delta Vio	-0.48	0.09	0.49	mV
Delta Vtrip+	-0.76	0.13	0.80	
Delta Vtrip-	-0.40	0.06	0.49	
Delta Iib	-0.70	-0.23	0.43	µA
Delta Tplh (150 mV step)	-0.30	-0.04	0.20	ns
Delta Tplh (200 mV step)	-0.25	-0.02	0.20	
Delta Tphl (150 mV step)	-0.15	0.05	0.35	
Delta Tphl (200 mV step)	-0.10	0.02	0.20	
Delta Tr	-0.06	0.00	0.04	
Delta Tf	-0.08	-0.04	0.00	
Delta Fmax	-2.00	0.40	4.00	MHz
Delta ICC-H	-0.01	0.44	1.86	mA
Delta ICC-L	-0.01	0.44	1.86	
Delta VOH	-0.02	0.00	0.01	mV
Delta VOL	-5.91	-3.58	-1.17	
Delta Isink	0.06	0.28	0.44	mA
Delta Isource	0.00	0.14	0.31	
Delta SVR	-16.26	1.97	9.78	dB
Delta CMRR	-8.63	2.43	16.68	

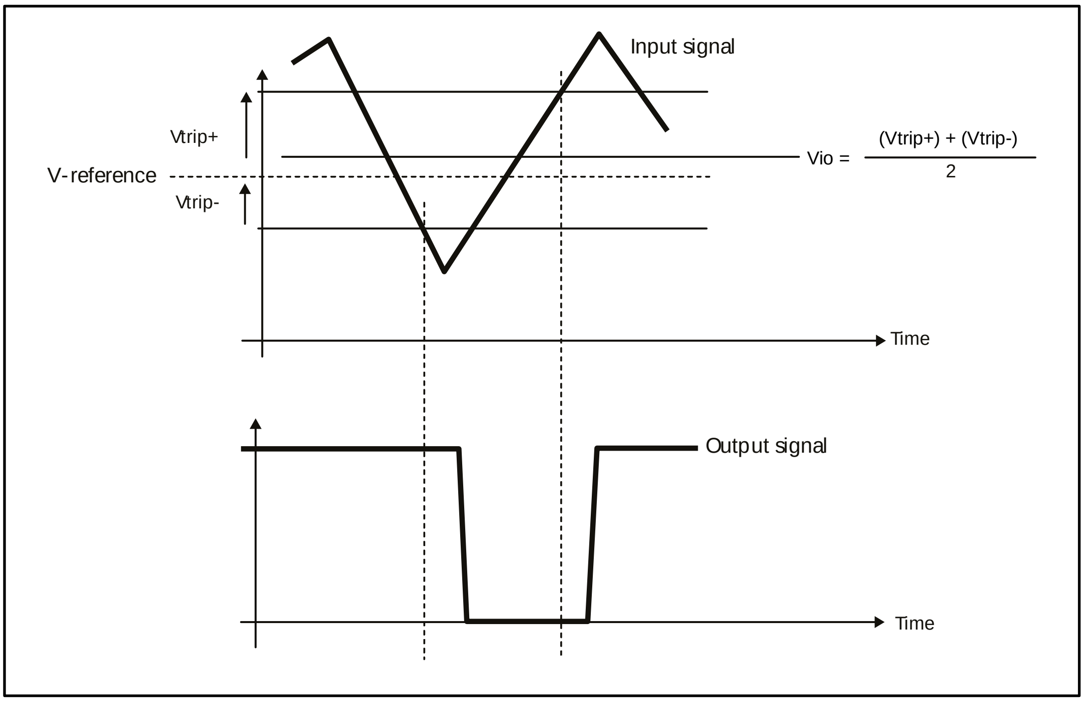
4.3 Heavy ions

The heavy ion trials are performed on qualification lots only. No additional test is performed.

5 Parameters and implementation

5.1 Static input features

Figure 35: Input threshold



5.2 Dynamic characteristics

Figure 36: Output rise and fall times

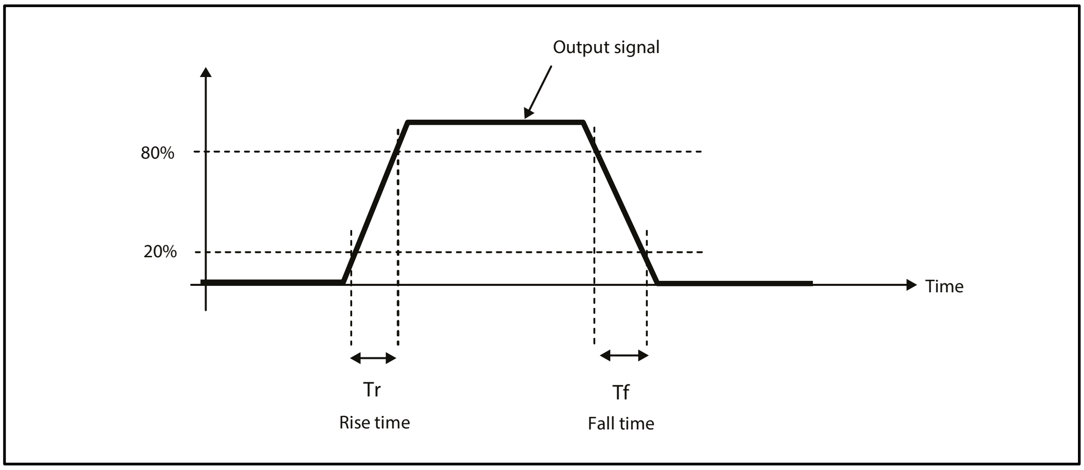


Figure 37: Input step and overdrive

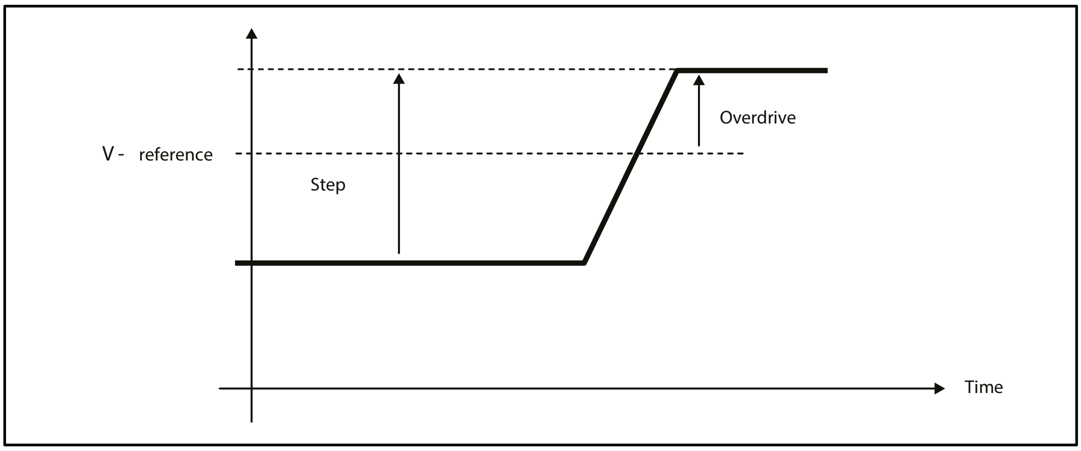
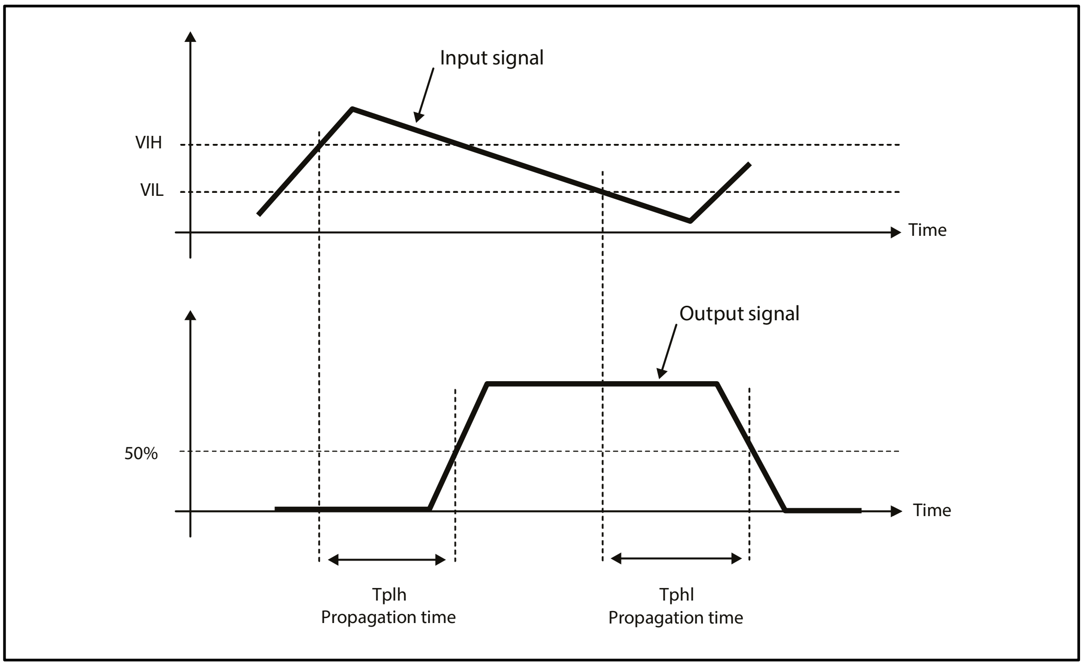


Figure 38: Propagation time



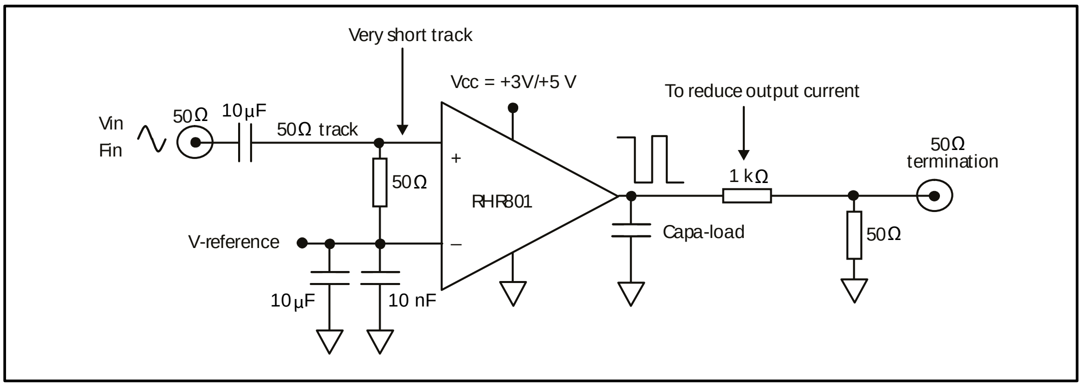
5.3 Characteristics of the output stage

The RHR801 uses a rail-to-rail MOS output. The output levels are guaranteed through testing (see the output characteristics in *Table 4* and *Table 5*). This stage is optimized for driving a load of 1 kΩ, with no stability issues. The capacitive load affects both the rise and fall times.

5.4 Impedance matching for dynamic measurements

To correctly evaluate this high-speed comparator, both the input and output must be properly matched (50 Ω). This matching is mandatory to avoid reflections on the tracks and cables, particularly at such high-speed rise and fall times. The matching of the input is relatively easy to perform with a 50 Ω input resistance placed as close as possible to the comparator input. The input track is 50 Ω matched. For the output, the comparator cannot drive a 50 Ω line directly. So, to reduce the output current while keeping a good 50 Ω termination on both sides of the cable, it is mandatory to use a series resistor much greater than 50 Ω, for example, 1 kΩ as in *Figure 39*.

Figure 39: Output impedance matching



5.5 Implementation on the board

The RHR801 is a very high-speed product that features very sharp output rise and fall times. The very high current variations must be appropriately managed and proper board layout techniques should be used to ensure best performances.

It is important to minimize the resistance from the source to the input of the comparator. High resistance values combined with the equivalent input capacitance can result in time constants below the capability of the comparator. This is the cause of a lagged response at the input, resulting in an output delay. Moreover, proper ground impedance and other layout techniques must be implemented to minimize the input stray capacitance, such as very short tracks on any high-impedance termination.

With high-speed applications, it is very important to provide bypass capacitors for the power supply. Good power supply decoupling is mandatory (pin 4 and pin 7), as well as good decoupling on the reference (pin 2). With dual supplies, a 10 µF bypass capacitor should be placed on each power supply pin. This capacitor reduces any potential voltage ripple from the power supply at lower frequencies. A 10 nF ceramic capacitor should be placed as close as possible to the power supply pins and be tracked to ground. This capacitor reduces higher frequency noise during high-frequency switching.

A proper ground plane is particularly recommended for high-speed performance. It can be created by implementing a continuous conductive plane all over the surface of the circuit board, with breaks for the necessary paths only. A proper ground plane minimizes the effects of stray capacitance on the circuit board and facilitates the layout of matched tracks.

This ground plane also provides a low inductive ground, eliminating any potential differences at various ground points.

Figure 40: Single supply layout

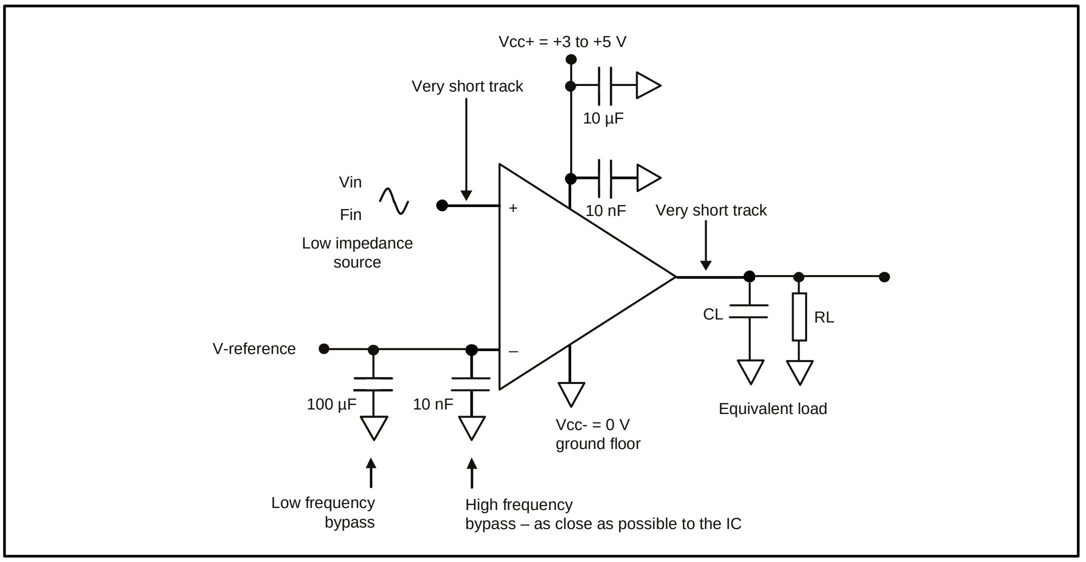


Figure 41: Dual supply layout

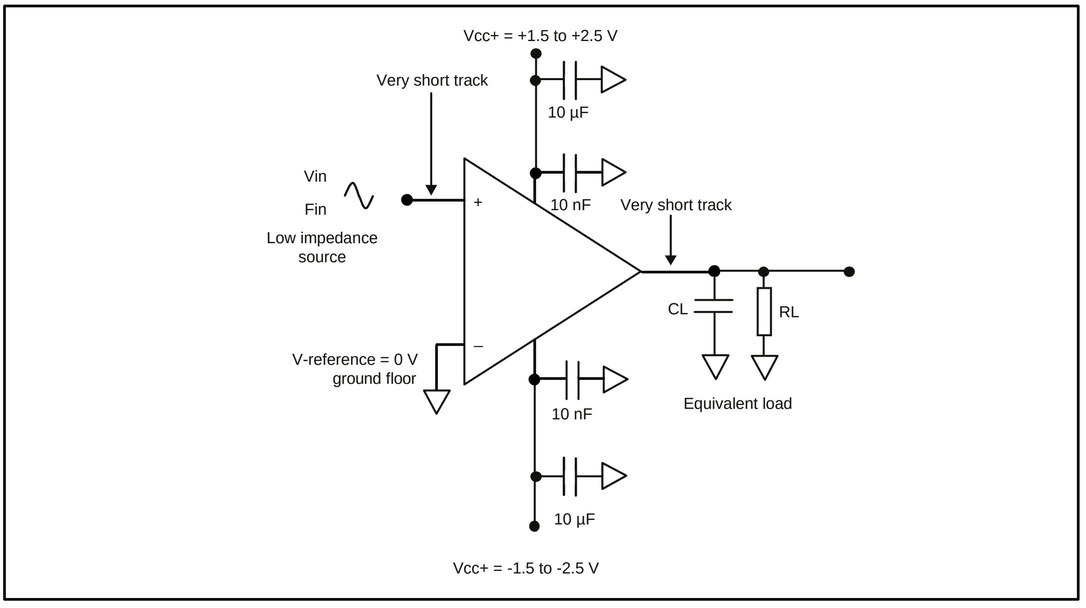
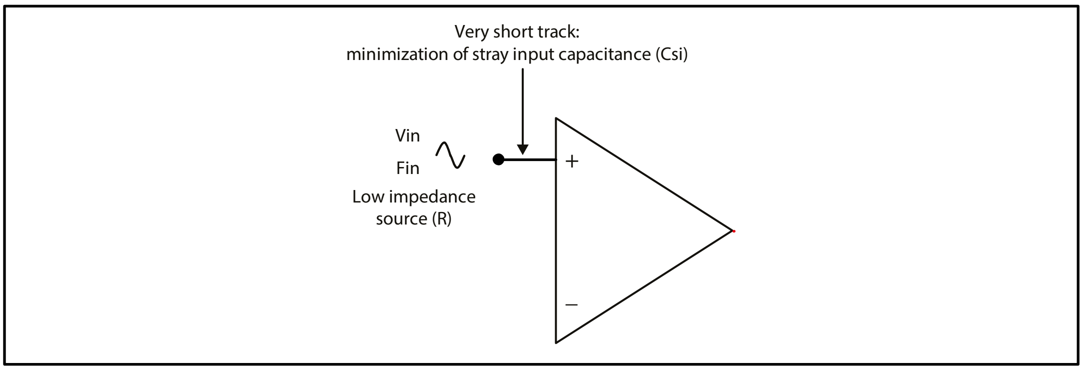
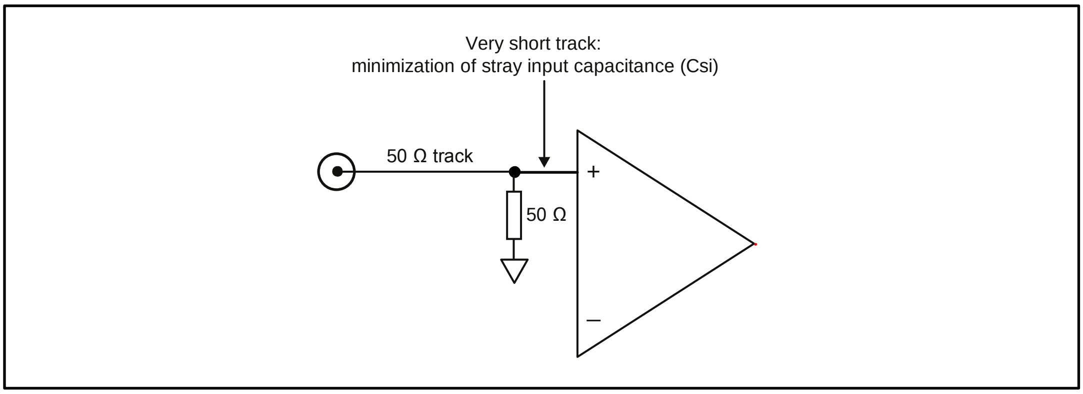


Figure 42: Input impedance matching



Time constant t = R x Csi should be as low as possible and t << Tr, Tf, Tplh, and Tphl.

Figure 43: 50 Ω matching



Time constant t = 50 Ω x Csi should be as low as possible and t << Tr, Tf, Tplh, and Tphl.

5.6 Application examples

5.6.1 Inverting comparator with hysteresis

The RHR801 comparator has a typical 2.5 mV implemented input voltage hysteresis which improves device stability and ensures a clean output response when the input signal amplude is relative small or moving slowly. However, in certain situations, like in noisy environments, it is desirable to increase the hysteresis value. This can easily be done by an external positive feedback network connected to the device.

Figure 44: External hysteresis circuit

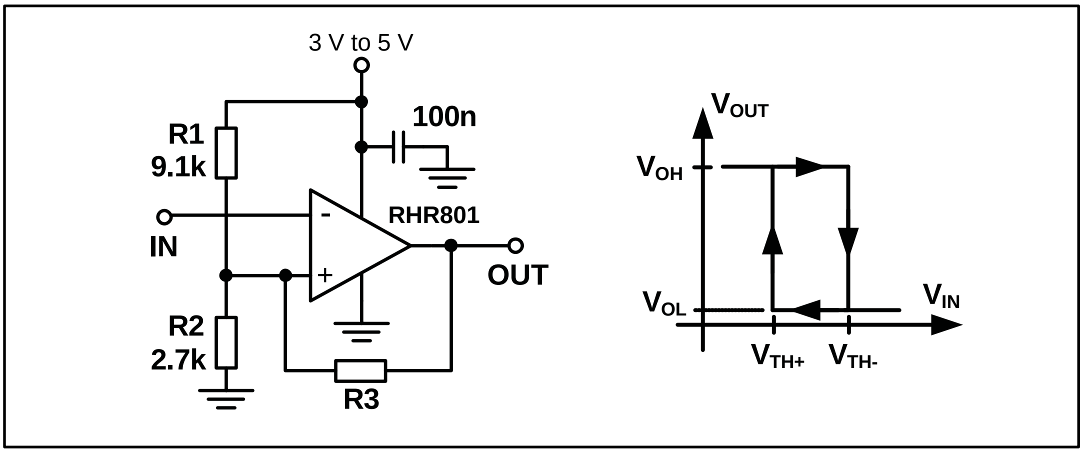


Figure 44 shows the circuit with positive feedback between the output and non-inverting input. Threshold voltages are given by the R1, R2, and R3 ratio and the V_{CC} power supply voltage. Neglecting input bias current and output voltage drop, V_{TH+}, and V_{TH-} can be calculated using *Equation 1*.

Equation 1

$$V_{TH} = V_{CC} \bullet \frac{R_2}{R_2 + R_1 | R_3}$$

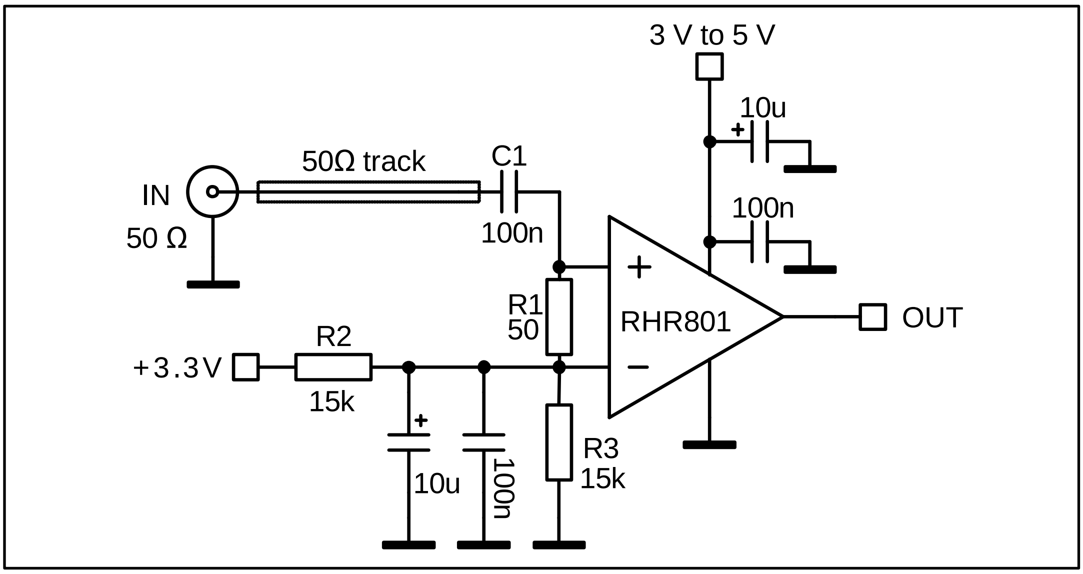
$$V_{TH} = V_{CC} \bullet \frac{R_2 | R_3}{R_1 + R_2 | R_3}$$

The symbol "|" represents a resistors parallel combination. The threshold voltages of *Figure 44* are set to V_{TH+} = 1.1 V and V_{TH-} = 1.3 V.

5.6.2 Fast signal recovery

The circuit in *Figure 45* represents an example of a simple translator input signal from a 50 Ω transmission line to a CMOS compatible output.

Figure 45: Signal recovery circuit

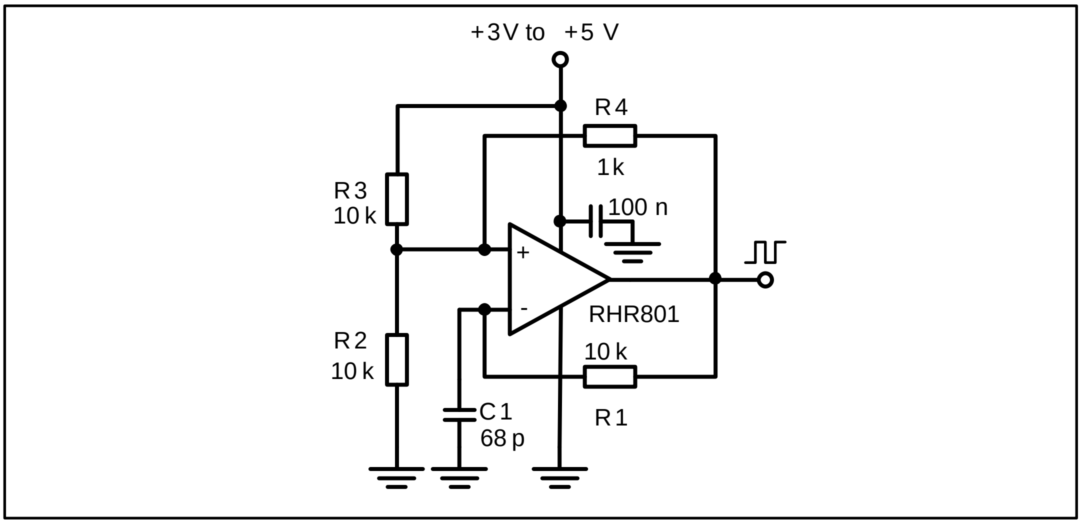


The reference voltage is set by the resistors R_2 and R_3 to 1.65 V. Capacitor (C) in parallel with R_1 ensure stable low impedance of the reference input during a transition period. A 100-nF capacitor, with low ESR, must be placed close to the device pin. C_1 removes the DC component from the input signal while R_1 terminates the 50 Ω input and avoids signal reflection. The minimum operating frequency is given by C_1 and it is about 100 kHz.

5.6.3 10 MHz RC oscillator

The circuit in *Figure 46* provides a square signal with a frequency of about 10 MHz. This circuit utilizes both positive and negative feedback. Positive feedback produces the R_2, R_3, and R_4 resistor network which implements input voltage hysteresis described in *Section 5.6.1*. Because $R_2 = R_3 = R_4$, the threshold voltages are 1/3 of the V_{CC} and 2/3 of the V_{CC}. Consequently, output duty cycle is 50 % and output frequency is independent of V_{CC}.

Figure 46: RC oscillator



The R1 feedback resistor periodically charges and discharges the C_1 capacitor. The output signal period can be calculated using *Equation 2*. Note that this equation is valid only when $R_2 = R_3 = R_4$.

Equation 2

$$T = \ln(4) \cdot \tau = 1.39 \cdot R_1 \cdot C_1$$

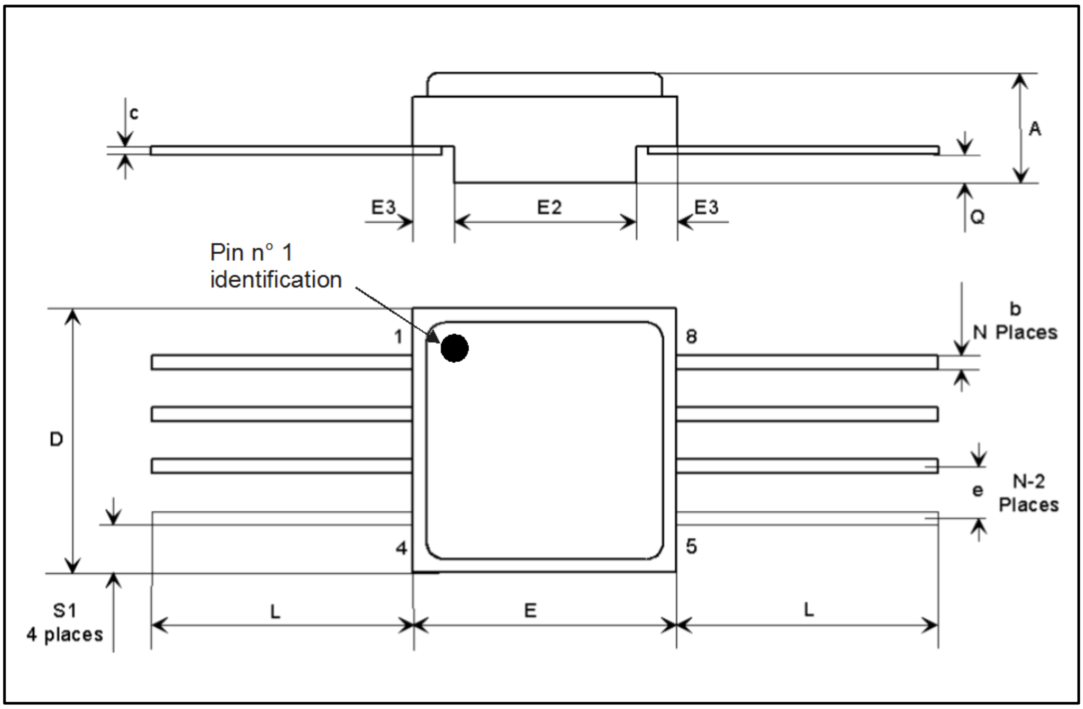
In a real application, output frequency is slightly lower than calculated due to PCB parasitic capacitances.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 Ceramic Flat-8 package information

Figure 47: Ceramic Flat-8 package outline



The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 11: Ceramic Flat-8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51		7.38	0.256		0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

7 Ordering information

Table 12: Order codes

Order code	Description	Temp. range	Package	Marking [(1)]	Packing
RHR801K1	Engineering model	-55 °C to 125 °C	Flat-8	RHR801K1	Strip pack
RHR801K01V	QML-V flight			5962R102150 1VXC	

Notes:

[(1)]Specific marking only. Complete marking includes the following: SMD pin (on QML-V flight only) ST logo Date code (date the package was sealed) in YYWWA (year, week, and lot index of week) QML logo (Q or V) Country of origin (FR = France)

Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

8 Other information

8.1 Date code

The date code is structured as shown below:

- EM xyywwz
- QML-V yywwz
  where:
  - x (EM only) = 3 and the assembly location is Rennes, France
  - yy = last two digits of the year
  - ww = week digits
  - z = lot index in the week

8.2 Documentation

Table 13: Documentation provided for each type of product

Quality level	Documentation
Engineering model	—
QML-V flight	Certificate of conformance
	QCI (groups A, B, and E) (1)
	Screening electrical data
	Precap report
	PIND test (2)
	SEM inspection report (3)
	X-ray report
	Failed component list (4)

Notes:

(1)QCI = quality conformance inspection

(2)PIND = particle impact noise detection

(3)SEM = scanning electron microscope

(4)List of components that failed during screening

9 Revision history

Table 14: Document revision history

Date	Revision	Changes
10-Jun-2014	1	Initial release
23-Mar-2015	2	Replaced package silhouette Updated Device summary table Added electrical characteristic curves into the Electrical characteristics section. Reworked Radiations section Figure 47: replaced Flat-8S package with Flat-8 package. Modified "L" values of Table 11: "Ceramic Flat-8 package mechanical data" Made small text changes to Section 7: "Other information"
16-Mar-2016	3	Updated document layout Device summary table: updated EPPL information and footnote 1 (SMD = standard microcircuit drawing).
29-Jun-2017	4	Replaced order code name RHR801K-01V with RHR801K01V.

IMPORTANT NOTICE – PLEASE READ CAREFULLY