

# Multilayer Ceramic Chip Capacitor

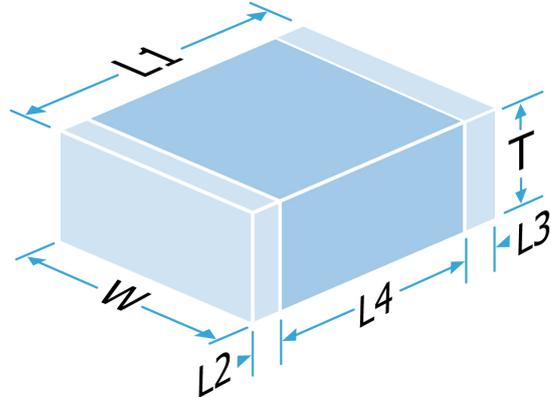
**Part Number:** 2211JA250101KATSPU

**Description:** 2211 250Vac 50/60Hz / 2500Vdc 100pF  
±10% C0G/NP0 (1B) to AEC-Q200

**Approval Specifications:** IEC/EN60384-14:2013  
UL-60950-1, 2nd Ed  
CSA 60950-1-07 2nd Ed

**Certification:** Unmarked parts are uncertified but manufactured in accordance with the above specifications.

**Classification:** These capacitors comply with the requirements of IEC/EN 60384-14:2013. For class Y2/X1.



**Component Marking and Certification Bodies:**

Not Applicable

## Mechanical Specification

Size Code	2211
Length (L1) in mm (")	5.7 ± 0.40 (0.225 ± 0.016)
Width (W) in mm (")	2.79 ± 0.30 (0.11 ± 0.012)
Thickness (T) in mm (")	2.54 Max (0.1 Max)
Minimum Termination Band (L2,L3) in mm (")	0.50 (0.020)
Maximum Termination Band (L2,L3) in mm (")	0.80 (0.030)
Minimum Band Gap (L4) in mm (")	4.0 (0.158)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 750 per reel

## General Electrical Specification

Rated Voltage	250Vac 50/60Hz / 2500Vdc 5kV impulse
Nominal Capacitance Value	100pF
Capacitance Tolerance	±10%
Tangent of Loss Angle (Tan δ)	≤0.0015
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof	3000Vdc/2000Vac
(Voltage applied for 5 secs max. @ 50mA max. charge current)	
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G/NP0 (1B) to AEC-Q200
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

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Date: Friday, January 18, 2019

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## Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	191 compliant
California Proposition 65	No exposure risk

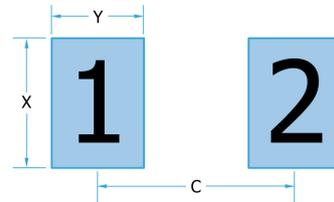
## Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

### IPC-7351 pad design

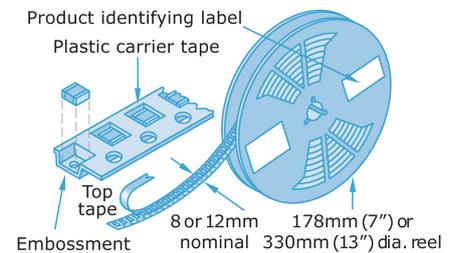
	2211	
C	5.40mm	0.213"
Y	1.35mm	0.053"
X	3.10mm	0.122"



## Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



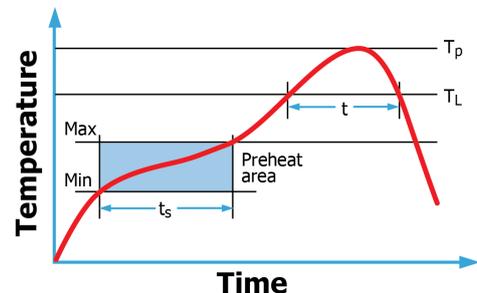
## Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

Application notes with mounting and handling guidance are available on request.



Compex

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