

# TPS56528 Buck Converter Evaluation Module User's Guide



TEXAS INSTRUMENTS

## ABSTRACT

This user's guide contains information for the TPS56528EVM-534 evaluation module as well as for the TPS56528. Included are the performance specifications, schematic, and the bill of materials of the TPS56528EVM-534.

## Table of Contents

<b>1 Introduction</b> .....	2
<b>2 Performance Specification Summary</b> .....	3
<b>3 Modifications</b> .....	4
3.1 Output Voltage Setpoint.....	4
3.2 Output Filter and Closed-Loop Response.....	4
<b>4 Test Setup and Results</b> .....	5
4.1 Input/Output Connections.....	5
4.2 Start-Up Procedure.....	5
4.3 Efficiency.....	5
4.4 Load Regulation.....	6
4.5 Line Regulation.....	8
4.6 Load Transient Response.....	8
4.7 Output Voltage Ripple.....	8
4.8 Input Voltage Ripple.....	10
4.9 Start-Up.....	10
4.10 Shut-Down.....	11
<b>5 Board Layout</b> .....	13
5.1 Layout.....	13
<b>6 Schematic, Bill of Materials, and Reference</b> .....	15
6.1 Schematic.....	15
6.2 Bill of Materials.....	16
6.3 Reference.....	16
<b>7 Revision History</b> .....	16

## Trademarks

D-CAP2™ and Eco-mode™ are trademarks of Texas Instruments.

All trademarks are the property of their respective owners.

## 1 Introduction

The TPS56528 is a single, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 650 kHz. Pulse skipping Eco-mode™ operation improves efficiency under light load conditions. The high-side and low-side switching MOSFETs are incorporated inside the TPS56528 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFETs allows the TPS56528 to achieve high efficiencies and helps keep the junction temperature low at high-output currents. The TPS56528 dc/dc synchronous converter is designed to provide up to a 5-A output from an input voltage source of 4.5 V to 18 V. The output voltage range is from 0.6 V to 7 V. Rated input voltage and output current range for the evaluation module are given in [Table 1-1](#).

The TPS56528EVM-534 evaluation module circuit is a single, synchronous buck converter providing 1.2 V at 5 A from 4.5-V to 18-V input. This user's guide describes the TPS56528EVM-534 performance.

**Table 1-1. Input Voltage and Output Current Summary**

EVM	Input Voltage Range	Output Current Range
TPS56528EVM-534	$V_{IN} = 4.5 \text{ V to } 18 \text{ V}$	0 A to 5 A

## 2 Performance Specification Summary

A summary of the TPS56528EVM-534 performance specifications is provided in [Table 2-1](#). Specifications are given for an input voltage of  $V_{IN} = 12$  V and an output voltage of 1.2 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

**Table 2-1. TPS56528EVM-534 Performance Specifications Summary**

Specifications	Test Conditions	Min	Typ	Max	Unit
Input voltage range ( $V_{IN}$ )		4.5	12	18	V
Output voltage			1.2		V
Operating frequency	$V_{IN} = 12$ V, $I_O = 2.5$ A		650		kHz
Output current range		0		5	A
Line regulation	$I_O = 2.5$ A		+0.5/-0.3		%
Load regulation	$V_{IN} = 12$ V		+0.8 /-0.11		%
Overshoot limit	$V_{IN} = 12$ V, $L_O = 1.5$ $\mu$ H	5.5	6.2	7.9	A
Output ripple voltage	$V_{IN} = 12$ V, $I_O = 5$ A		10		mV <sub>PP</sub>
Maximum efficiency	$V_{IN} = 5$ V, $I_O = 0.7$ A		89.9		%

## 3 Modifications

These evaluation modules are designed to provide access to the features of the TPS56528. Some modifications can be made to this module.

### 3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.600 V. The value of R1 for a specific output voltage can be calculated using [Equation 1](#).

For output voltage from 0.6 V to 7 V:

$$V_O = 0.6 \times \left( 1 + \frac{R_1}{R_2} \right) \quad (1)$$

[Table 3-1](#) lists the R1 values for some common output voltages. For higher output voltages of 1.8 V or above, a feed-forward capacitor (C4) may be required to improve phase margin. Pads for this component (C4) are provided on the printed-circuit board (PCB). Note that the resistor values given in [Table 3-1](#) are standard values and not the exact value calculated using [Equation 1](#).

**Table 3-1. Output Voltages**

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF) <sup>(1)</sup>			L1 (μH)			C9 + C10 + C11 (μF)	
			Min	Typ	Max	Min	Typ	Max	Min	Max
1	33.2	49.9	5	33	100	1.0	1.5	4.7	20	68
1.05	37.4	49.9	5	33	100	1.0	1.5	4.7	20	68
1.2	49.9	49.9	5	22	47	1.0	1.5	4.7	20	68
1.5	75.0	49.9	5	15	33	1.0	1.5	4.7	20	68
1.8	100	49.9	5	10	22	1.0	1.5	4.7	20	68
2.5	158	49.9	5	10	22	1.5	2.2	4.7	20	68
3.3	226	49.9	2	5	15	1.5	2.2	4.7	20	68
5	365	49.9	2	5	10	2.2	3.3	4.7	20	68
6.5	487	49.9	2	5	10	2.2	3.3	4.7	20	68

(1) Optional

### 3.2 Output Filter and Closed-Loop Response

The TPS56528 relies on the output filter characteristics to ensure stability of the control loop. The recommended output filter components for common output voltages are given in [Table 3-1](#). It may be possible for other output filter component values to provide acceptable closed-loop characteristics. R3 and TP4 are provided for convenience in breaking the control loop and measuring the closed-loop response.

## 4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56528EVM-534. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

### 4.1 Input/Output Connections

The TPS56528EVM-534 is provided with input and output connectors and test points as shown in [Table 4-1](#). A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the  $V_{IN}$  input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

**Table 4-1. Connection and Test Points**

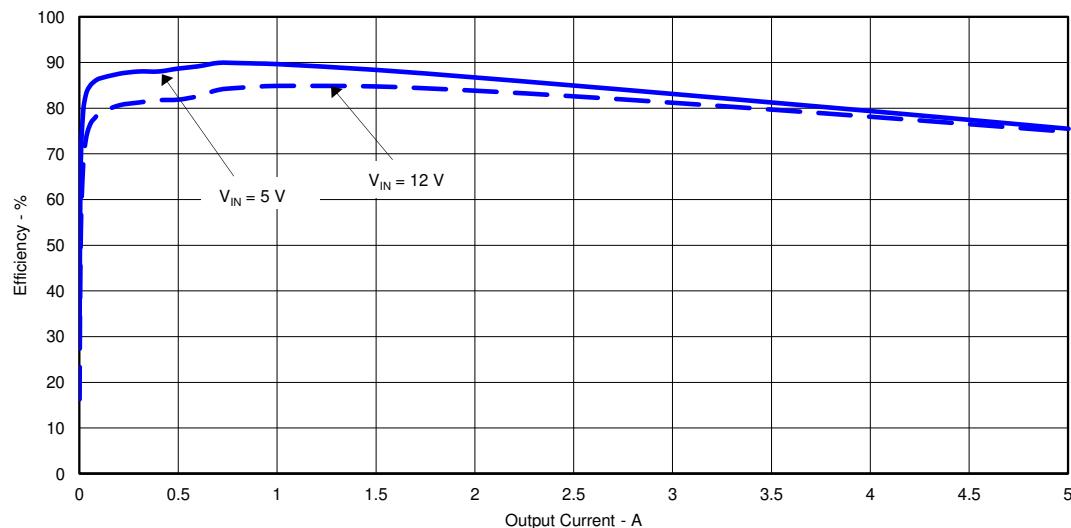
Reference Designator	Function
J1	$V_{IN}$ (see <a href="#">Table 1-1</a> for $V_{IN}$ range)
J2	$V_{OUT}$ , 1.2 V at 5-A maximum
JP1	EN control. Connect EN to OFF to disable, connect EN to ON to enable
TP1	$V_{IN}$ test point at $V_{IN}$ connector
TP2	GND test point at $V_{IN}$ connector.
TP3	EN test point
TP4	Power good (PG) test point
TP5	Switch node test point
TP6	Analog ground test point
TP7	Power ground test point
TP8	Output voltage test point at $V_{OUT}$ connector
TP9	Ground test point at $V_{OUT}$ connector

### 4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) is set from EN to OFF.
2. Apply appropriate VIN voltage to VIN and PGND terminals at J1.
3. Move the jumper at JP1 (Enable control) to cover EN and ON. The EVM enables the output voltage.

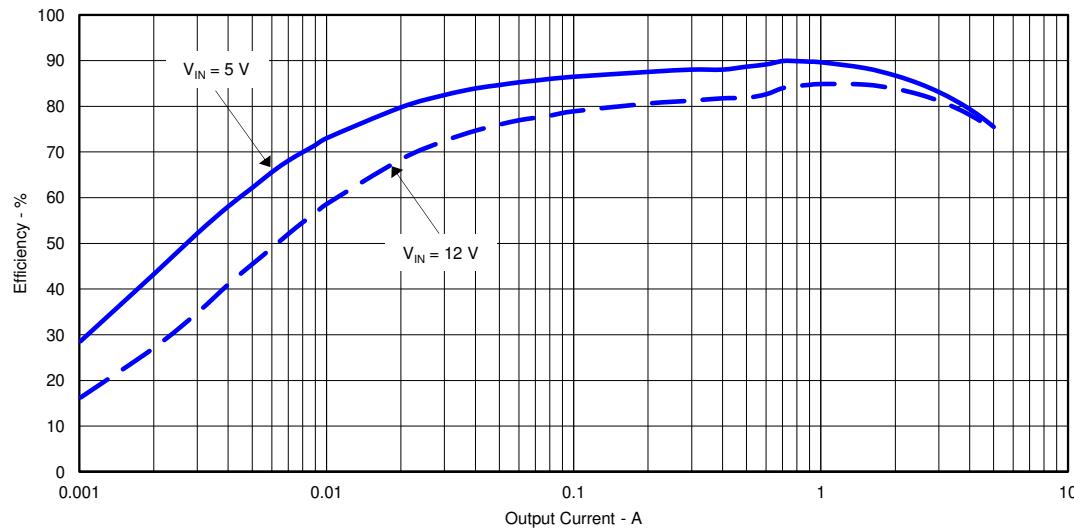
### 4.3 Efficiency

[Figure 4-1](#) shows the efficiency for the TPS56528EVM-534 at an ambient temperature of 25°C.



**Figure 4-1. TPS56528EVM-534 Efficiency**

Figure 4-2 shows the efficiency at light loads for the TPS56528EVM-534 at an ambient temperature of 25°C.



**Figure 4-2. TPS56528EVM-534 Light-Load Efficiency**

#### 4.4 Load Regulation

The load regulation for the TPS56528EVM-534 is shown in Figure 4-3.

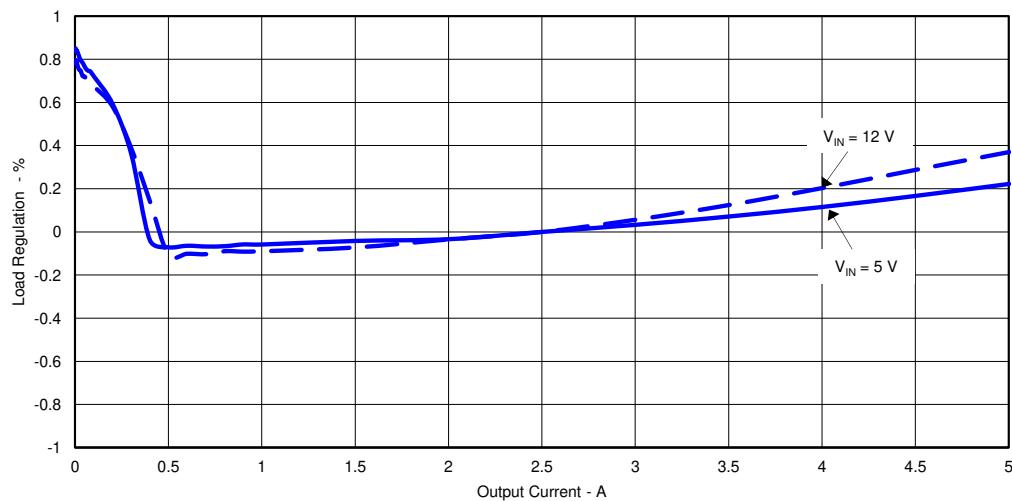
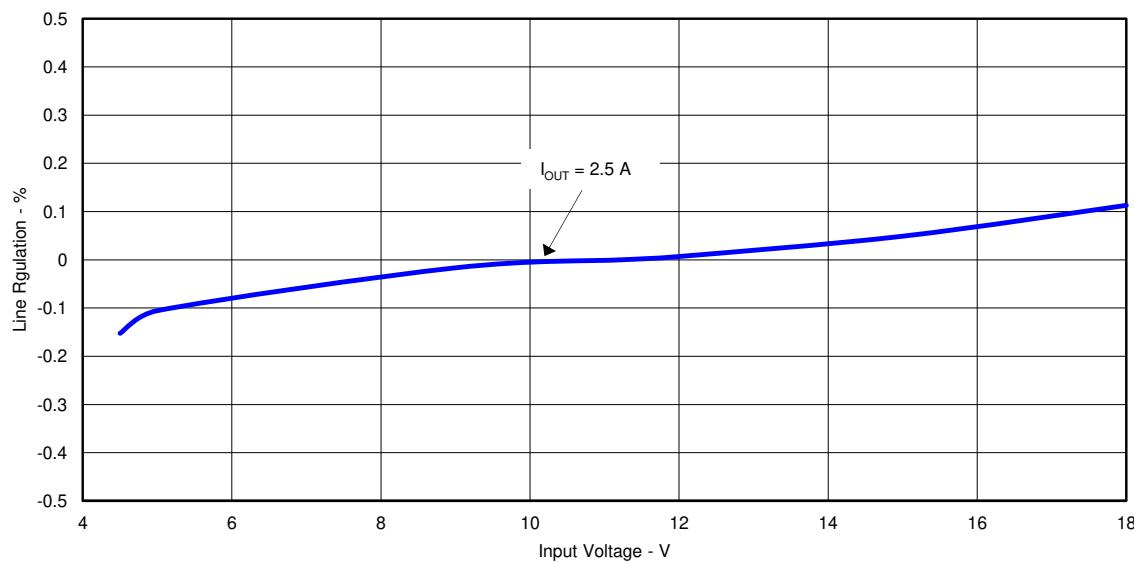


Figure 4-3. TPS56528EVM-534 Load Regulation,  $V_{IN} = 5\text{ V}$  and  $V_{IN} = 12\text{ V}$

## 4.5 Line Regulation

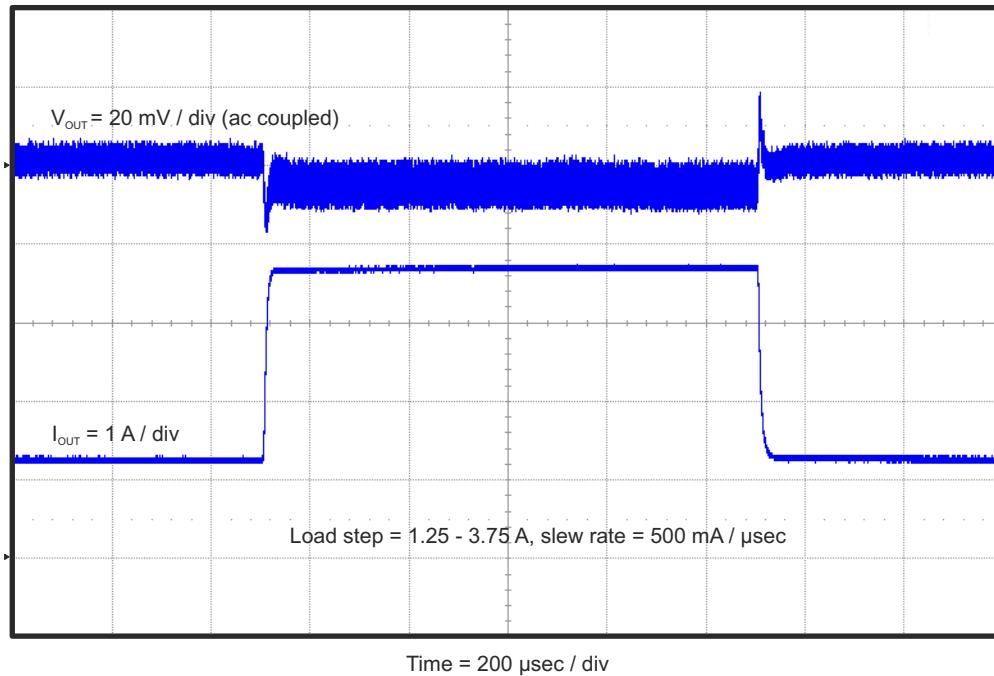
The line regulation for the TPS56528EVM-534 is shown in [Figure 4-4](#).



**Figure 4-4. TPS56528EVM-534 Line Regulation**

## 4.6 Load Transient Response

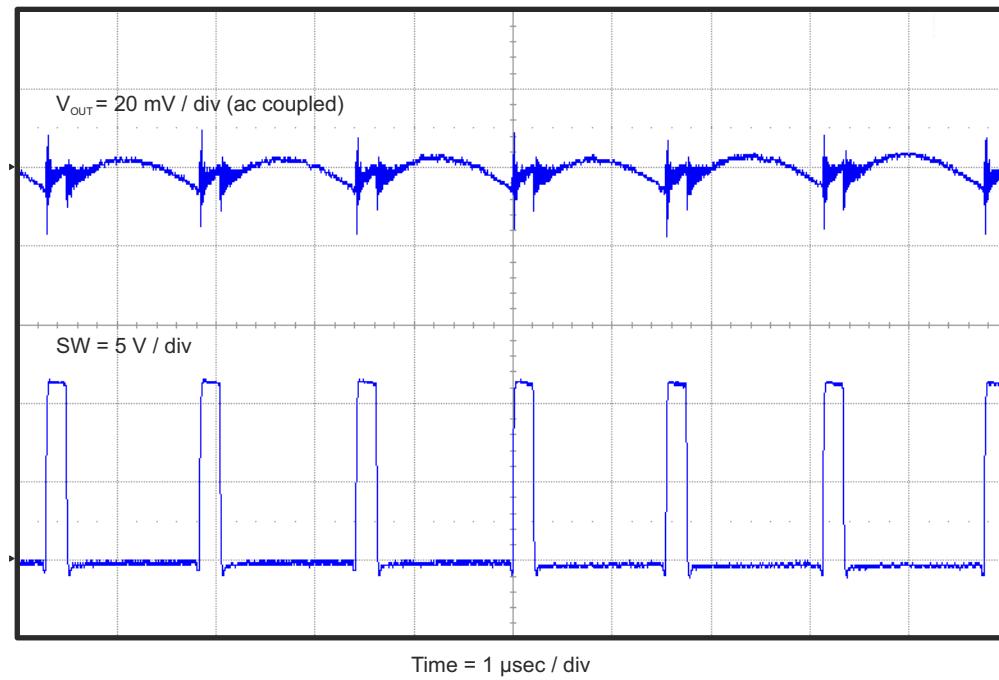
The TPS56528EVM-534 response to load transient is shown in [Figure 4-5](#). The current step is from 1.25 A to 3.75 A. Total peak-to-peak voltage variation is as shown.



**Figure 4-5. TPS56528EVM-534 Load Transient Response**

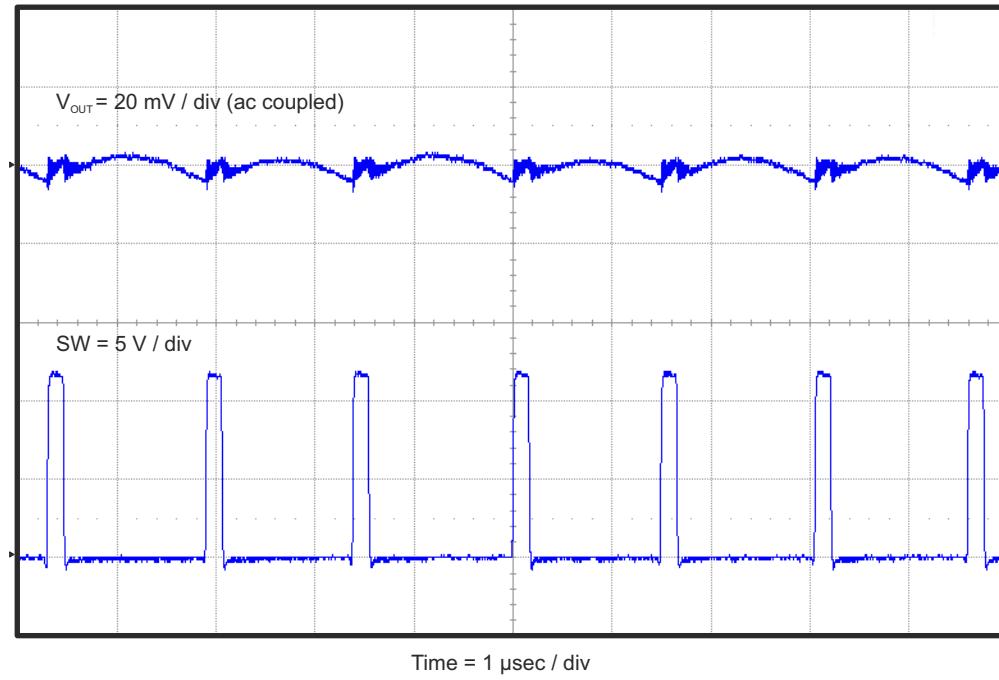
## 4.7 Output Voltage Ripple

The TPS56528EVM-534 output voltage ripple is shown in [Figure 4-6](#). The output current is the rated full load of 5 A.



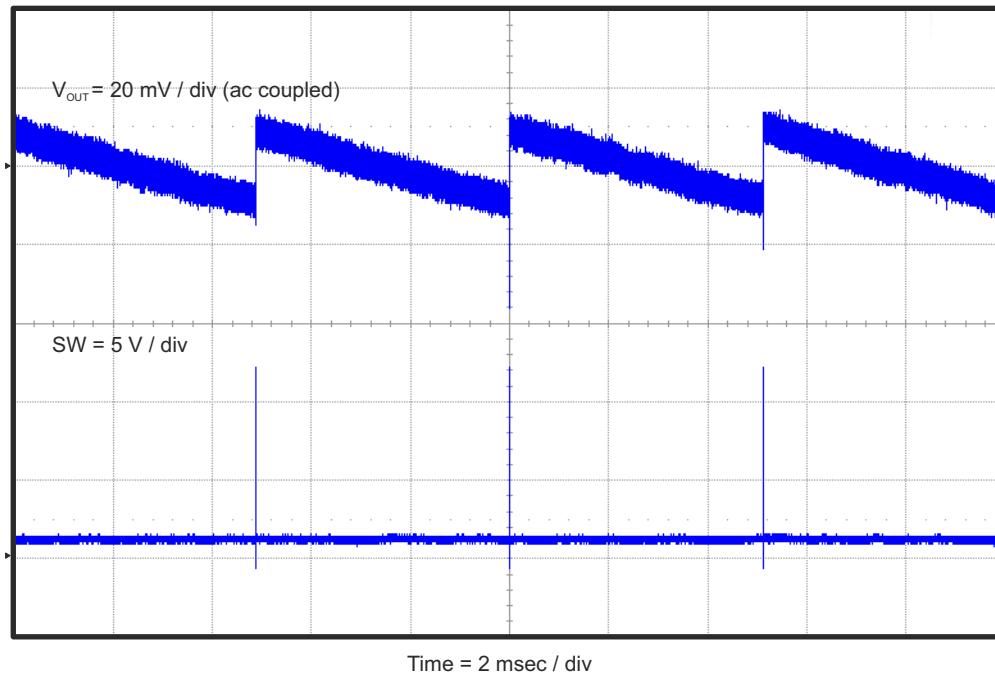
**Figure 4-6. TPS56528EVM-534 Output Voltage Ripple ( $I_{OUT} = 5 \text{ A}$ )**

The TPS56528EVM-534 output voltage ripple is shown in [Figure 4-7](#). The output current is 500 mA.



**Figure 4-7. TPS56528EVM-534 Output Voltage Ripple ( $I_{OUT} = 500 \text{ mA}$ )**

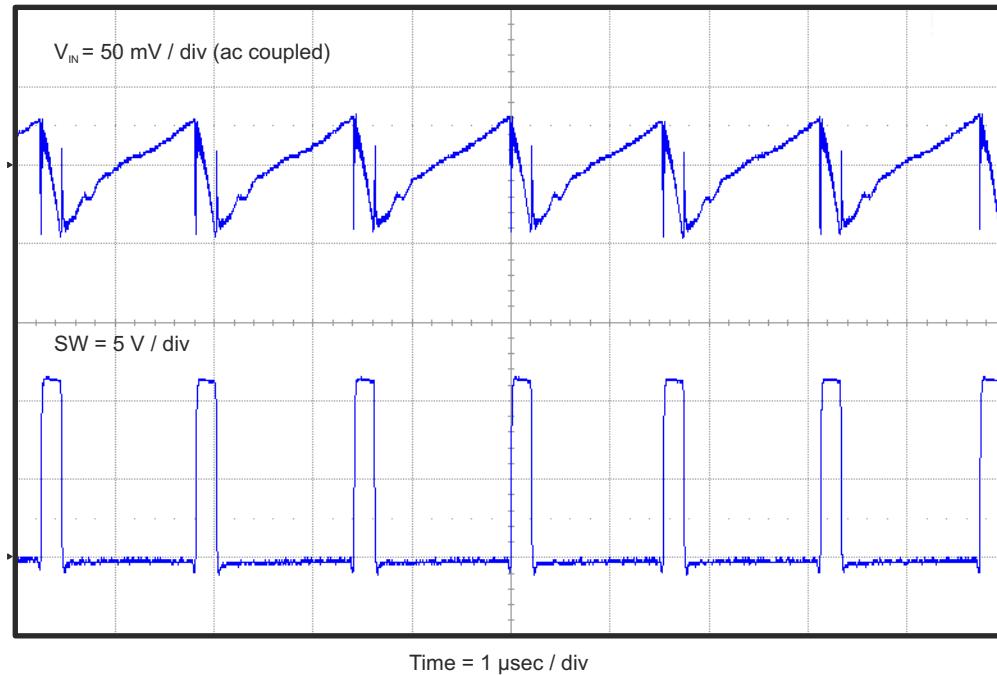
The TPS56528EVM-534 output voltage ripple is shown in [Figure 4-8](#). The output current is 1 mA.



**Figure 4-8. TPS56528EVM-534 Output Voltage Ripple ( $I_{OUT} = 1 \text{ mA}$ )**

#### 4.8 Input Voltage Ripple

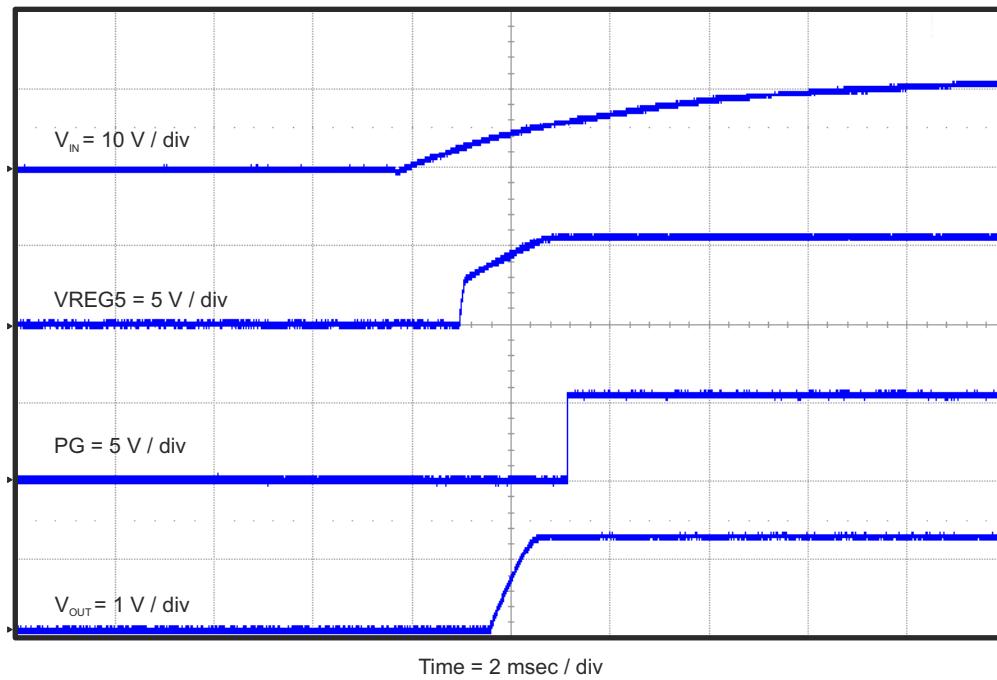
The TPS56528EVM-534 input voltage ripple is shown in [Figure 4-9](#). The output current is the rated full load of 5 A.



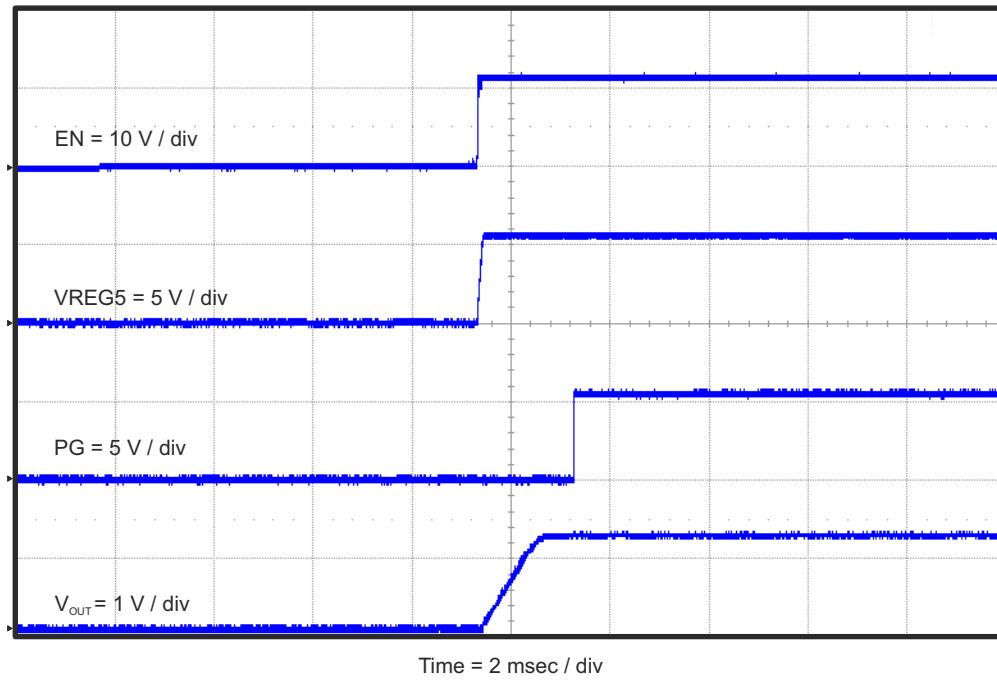
**Figure 4-9. TPS56528EVM-534 Input Voltage Ripple**

#### 4.9 Start-Up

The TPS56528EVM-534 start-up waveforms relative to  $V_{IN}$  and EN are shown in [Figure 4-10](#) and [Figure 4-11](#).  $R_{LOAD} = 1 \Omega$ .



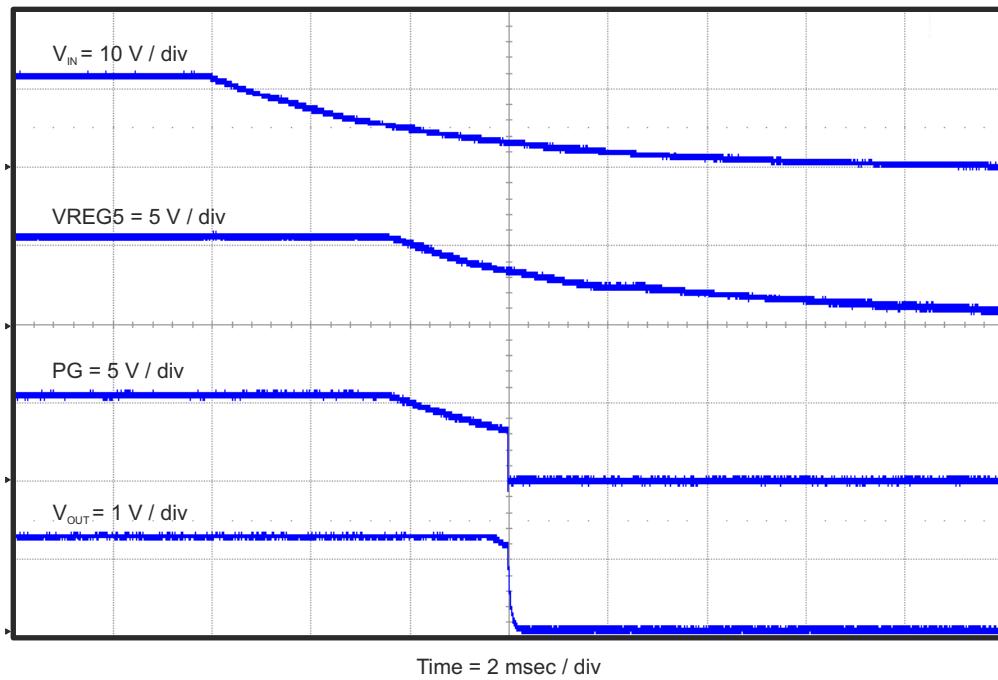
**Figure 4-10. TPS56528EVM-534 Start-Up Relative to  $V_{IN}$  with  $V_{REG5}$ ,  $PG$  and  $V_{OUT}$**



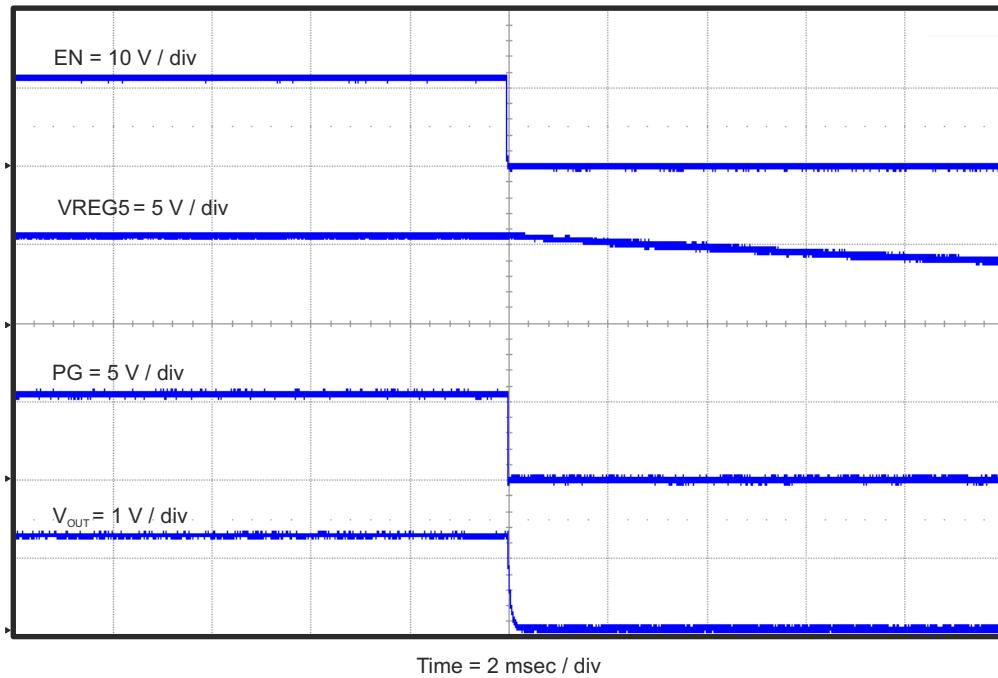
**Figure 4-11. TPS56528EVM-534 Start-Up Relative to EN with  $V_{REG5}$ ,  $PG$  and  $V_{OUT}$**

#### 4.10 Shut-Down

The TPS56528EVM-534 shut-down waveforms relative to  $V_{IN}$  and EN are shown in [Figure 4-12](#) and [Figure 4-13](#).  $R_{LOAD} = 1 \Omega$ .



**Figure 4-12. TPS56528EVM-534 Shut-Down Relative to V<sub>IN</sub> with VREG5, PG and V<sub>OUT</sub>**



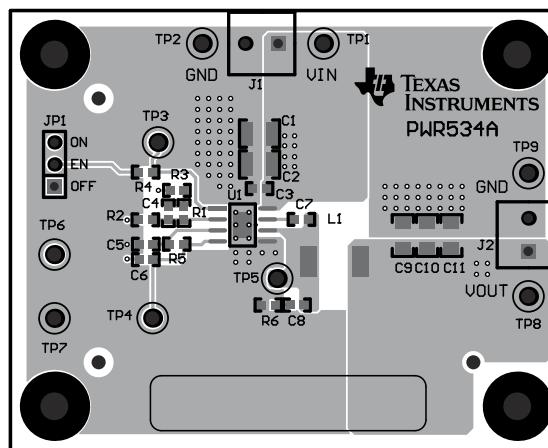
**Figure 4-13. TPS56528EVM-534 Shut-Down Relative to EN with VREG5, PG and V<sub>OUT</sub>**

## 5 Board Layout

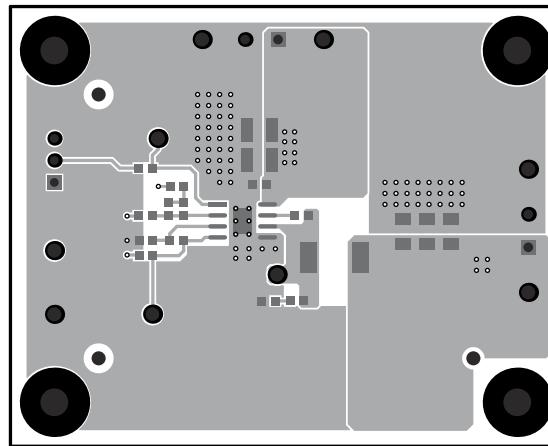
This section provides a description of the TPS56528EVM-534, board layout, and layer illustrations.

### 5.1 Layout

The board layout for the TPS56528EVM-534 is shown in [Figure 5-1](#) through [Figure 5-5](#). The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS56428 and a large area filled with ground. Many of the signal traces also are located on the top side. The input decoupling capacitors are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. Internal layer 1, internal layer 2 and the bottom layer are predominantly power ground planes. An analog ground (AGND) area is provided on internal layer 1. Analog ground (AGND) and power ground (PGND) are connected at a single point on internal layer 1 as shown. Internal layer 2 contains an additional VIN area as well as a connection to the VIN pin of the EN control jumper JP1. The bottom layer contains the output voltage feedback trace.



**Figure 5-1. Top Assembly**



**Figure 5-2. Top Layer**

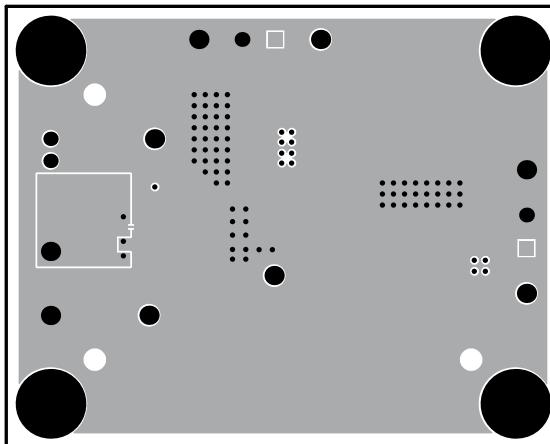


Figure 5-3. Internal Layer 1

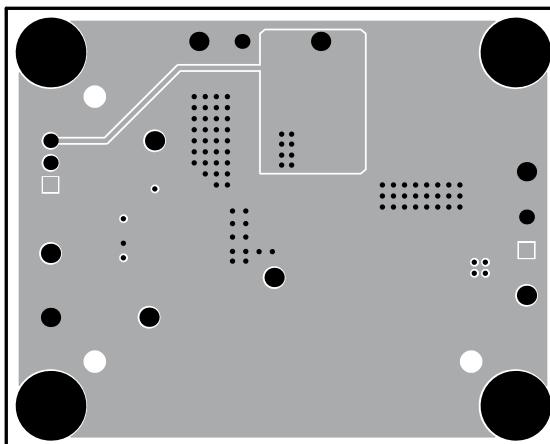


Figure 5-4. Internal Layer 2

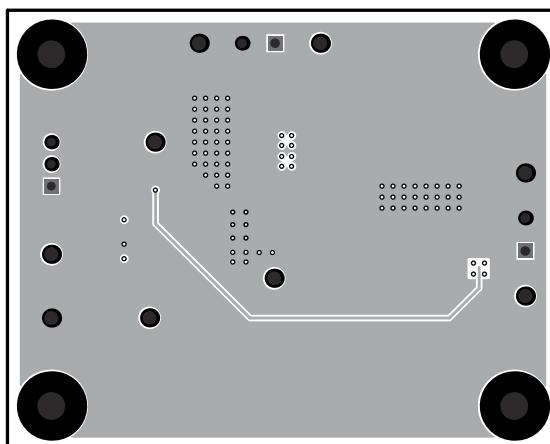


Figure 5-5. Bottom Layer

## 6 Schematic, Bill of Materials, and Reference

### 6.1 Schematic

Figure 6-1 is the schematic for the TPS56528EVM-534.

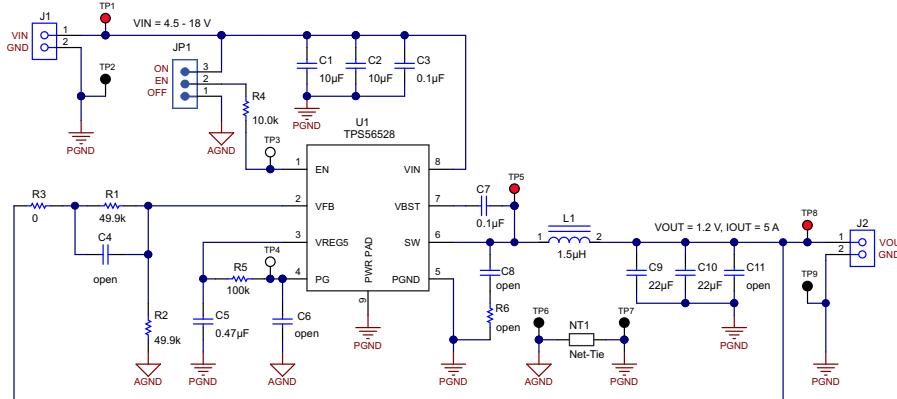


Figure 6-1. TPS56528EVM-534 Schematic Diagram

## 6.2 Bill of Materials

**Table 6-1. Bill of Materials**

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed Circuit Board	2.00" x 2.50"	PWR534A	Any
C1, C2	2	10uF	CAP, CERM, 10uF, 35V, +10%, X7R, 1210	1210	GRM32ER7YA106KA12L	MuRata
C3, C7	2	0.1uF	CAP, CERM, 0.1uF, 50V, +10%, X7R, 0603	0603	GRM188R71H104KA93D	MuRata
C4, C6, C8	0		CAP, CERM, xxxF, xxV, [TempCo], xx%, 0603	0603		
C5	1	0.47uF	CAP, CERM, 0.47uF, 25V, +10%, X5R, 0603	0603	GRM188R61E474KA12D	MuRata
C9, C10	2	22uF	CAP, CERM, 22uF, 10V, +10%, X5R, 1206	1206	GRM31CR61A226KE19L	MuRata
C11	0		CAP, CERM, xxxF, xxV, [TempCo], xx%, 1206	1206		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
J1, J2	2	2x1	Conn Term Block, 2POS, 3.81mm, TH	PhoenixConact_1727010	1727010	Phoenix Contact
JP1	1	1x3	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
L1	1	1.5μH	Inductor, SMT, 11A, 9.7 milliohm	0.256 x 0.280 inch	SPM6530-1R5M100	TDK
LBL1	1		Thermal Transfer Printable Labels, 1.25" W x 0.25" H - 10,000 per roll	PCB Label 1.25" H x 0.25" W	THT-13-457-10	Brady
R1, R2	2	49.9k	RES, 49.9k ohm, 1%, 0.1W, 0603	0603	CRCW060349K9FKEA	Vishay-Dale
R3	1	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	MCR03EZPJ000	Rohm
R4	1	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R5	1	100k	RES, 100k ohm, 1%, 0.1W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R6	0		RES, xxx ohm, x%, xW, 0603	0603		
SH-JP1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1, TP5, TP8	3	Red	Test Point, TH, Multipurpose, Red	Keystone5010	5010	Keystone
TP2, TP6, TP7, TP9	4	Black	Test Point, TH, Multipurpose, Black	Keystone5011	5011	Keystone
TP3, TP4	2	White	Test Point, TH, Multipurpose, White	Keystone5012	5012	Keystone
U1	1		DC-DC Converter, 4.5 - 18 Vin, 5A	SOP8	TPS56528DDA	Texas Instruments

## 6.3 Reference

1. *TPS56528, 4.5-V to 18-V Input, 5-A Synchronous Step-Down SWIFT™ Converter* data sheet ([SLVSBV3](#))

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2013) to Revision A (June 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	<a href="#">2</a>
• Updated user's guide title.....	<a href="#">2</a>

## **IMPORTANT NOTICE AND DISCLAIMER**

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated