

## N-Channel Enhancement Mode Field Effect Transistor

STL45N10F7AG use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in

### Features

Low RDS(on) & FOM

Extremely low switching loss

Excellent stability and uniformity of Invertors

### Applications

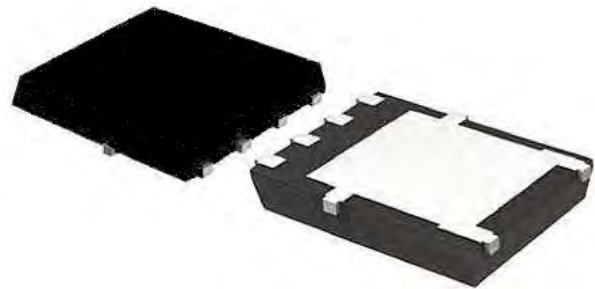
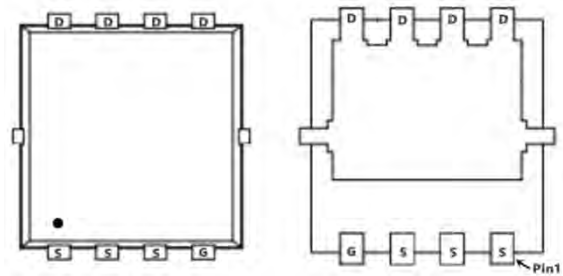
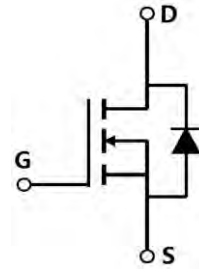
Consumer electronic power supply

Motor control

Synchronous-rectification

Isolated DC

Synchronous-rectification application



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
STL45N10F7AG	DFN5*6-8L	APG40N10NF	5000

### Absolute Maximum Ratings at $T_j=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V <sub>DS</sub>	100	V
Gate source voltage	V <sub>GS</sub>	±20	V
Continuous drain current <sup>1)</sup> , T <sub>C</sub> =25 °C	I <sub>D</sub>	40	A
Pulsed drain current <sup>2)</sup> , T <sub>C</sub> =25 °C	I <sub>D, pulse</sub>	120	A
Power dissipation <sup>3)</sup> , T <sub>C</sub> =25 °C	P <sub>D</sub>	72	W
Single pulsed avalanche energy <sup>5)</sup>	E <sub>AS</sub>	30	mJ
Operation and storage temperature	T <sub>stg</sub> , T <sub>j</sub>	-55 to 150	°C
Thermal resistance, junction-case	R <sub>θJC</sub>	1.74	°C/W

Thermal resistance, junction-ambient <sup>4)</sup>	R $\theta$ JA	62	°C/W
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## Electrical Characteristics at T<sub>J</sub>=25 °C unless otherwise specified

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0 V, I <sub>D</sub> =250 $\mu$ A	100			V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 $\mu$ A	1.0		2.5	V
Drain-source on-state resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10 V, I <sub>D</sub> =8 A		16	20	m $\Omega$
Drain-source on-state resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5 V, I <sub>D</sub> =6 A			26	m $\Omega$
Gate-source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =20 V			100	nA
					-100	
Drain-source leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =100 V, V <sub>GS</sub> =0 V			1	$\mu$ A
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0 V, V <sub>DS</sub> =50 V, f=1 MHz		1190.6		pF
Output capacitance	C <sub>oss</sub>			194.6		pF
Reverse transfer capacitance	C <sub>rss</sub>			4.1		pF
Turn-on delay time	t <sub>d(on)</sub>	V <sub>GS</sub> =10 V, V <sub>DS</sub> =50 V, R <sub>G</sub> =2.2 $\Omega$ , I <sub>D</sub> =10 A		17.8		ns
Rise time	t <sub>r</sub>			3.9		ns
Turn-off delay time	t <sub>d(off)</sub>			33.5		ns
Fall time	t <sub>f</sub>			3.2		ns
Total gate charge	Q <sub>g</sub>	I <sub>D</sub> =8 A, V <sub>DS</sub> =50 V, V <sub>GS</sub> =10 V		19.8		nC
Gate-source charge	Q <sub>gs</sub>			2.4		nC
Gate-drain charge	Q <sub>gd</sub>			5.3		nC
Gate plateau voltage	V <sub>plateau</sub>			3.2		V
Diode forward current	I <sub>S</sub>	V <sub>GS</sub> <V <sub>th</sub>			40	
Pulsed source current	I <sub>SP</sub>				120	A
Diode forward voltage	V <sub>SD</sub>	I <sub>S</sub> =8 A, V <sub>GS</sub> =0 V			1.3	V
Reverse recovery time	t <sub>rr</sub>	I <sub>S</sub> =8 A, di/dt=100 A/ $\mu$ s		50.2		ns
Reverse recovery charge	Q <sub>rr</sub>			95.1		nC
Peak reverse recovery current	I <sub>rrm</sub>			2.5		A

### Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R $\theta$ JA is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>a</sub>=25 °C.
- 5) V<sub>DD</sub>=50 V, R<sub>G</sub>=25  $\Omega$ , L=0.3 mH, starting T<sub>J</sub>=25 °C.

## Electrical Characteristics Diagrams

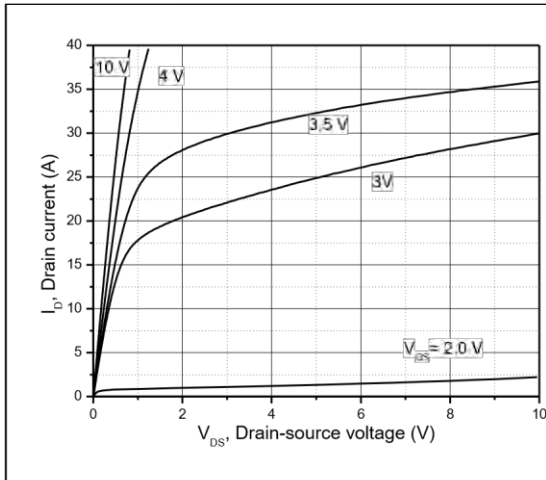


Figure 1, Typ. output characteristics

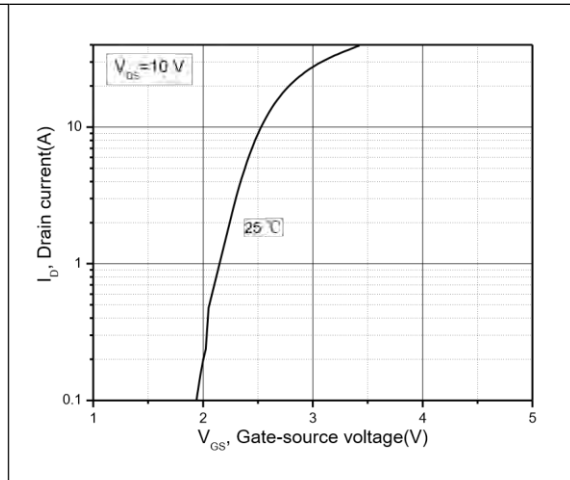


Figure 2, Typ. transfer characteristics

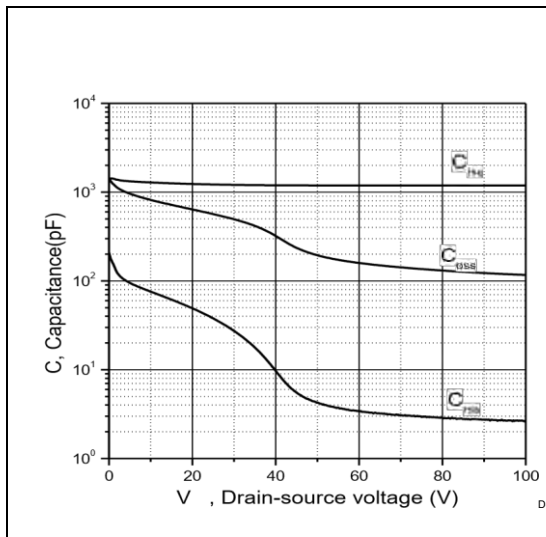


Figure 3, Typ. capacitances

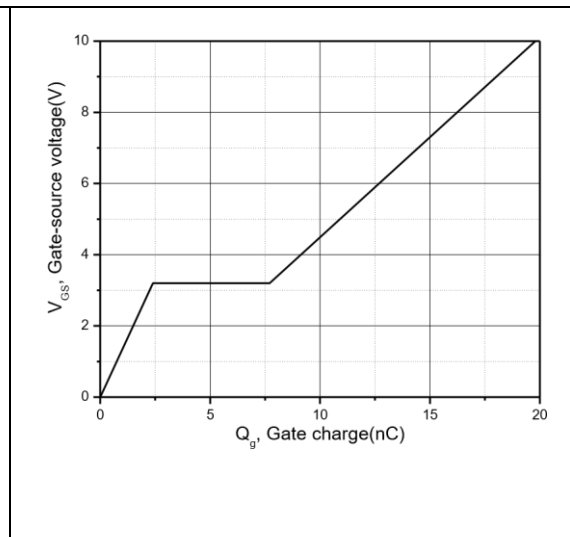


Figure 4, Typ. gate charge

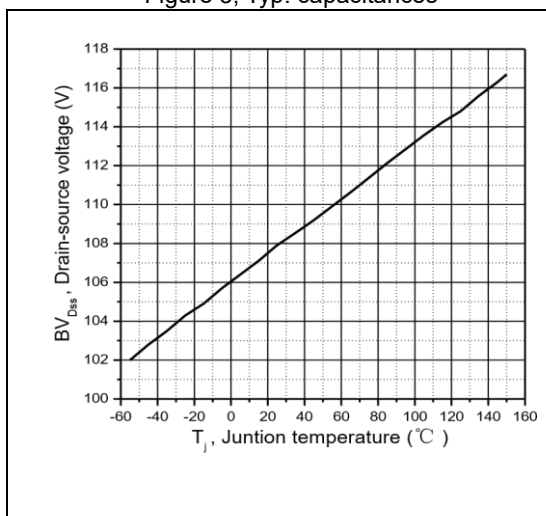


Figure 5, Drain-source breakdown voltage

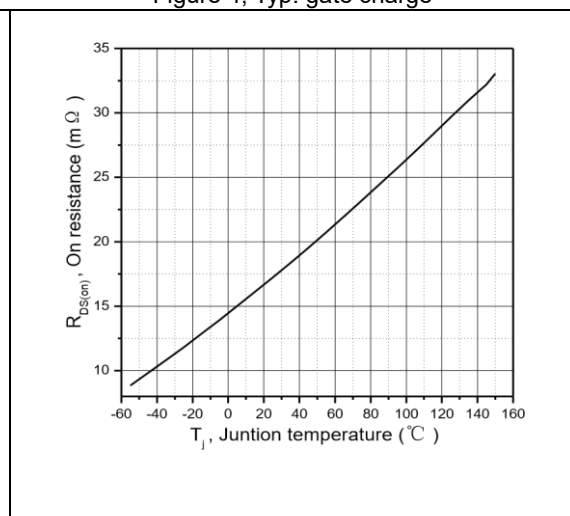


Figure 6, Drain-source on-state resistance

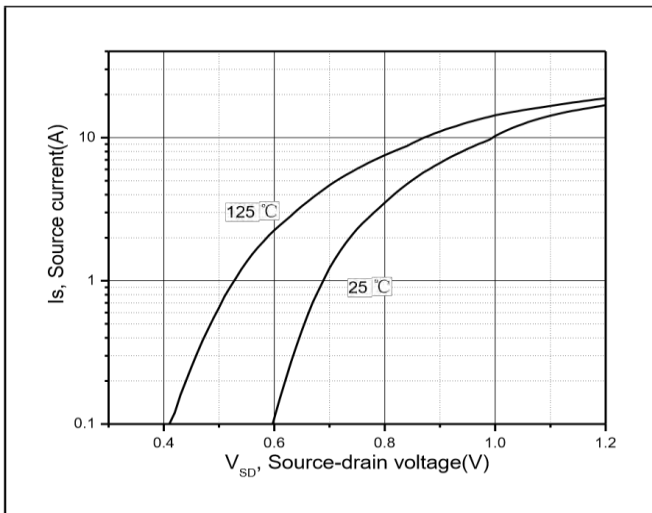


Figure 7, Forward characteristic of body diode

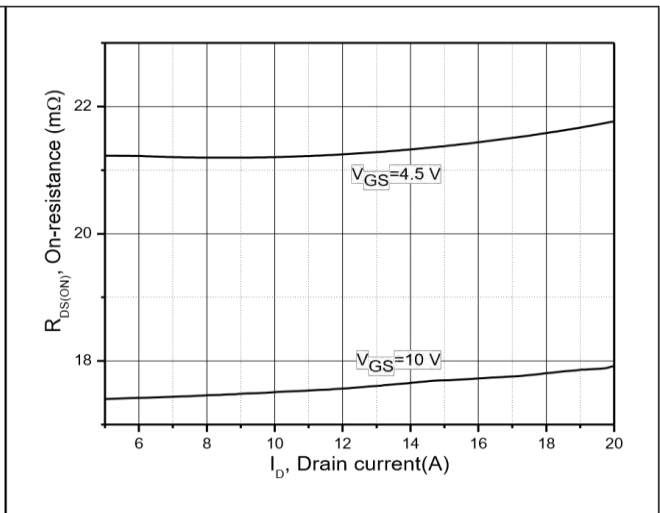


Figure 8, Drain-source on-state resistance

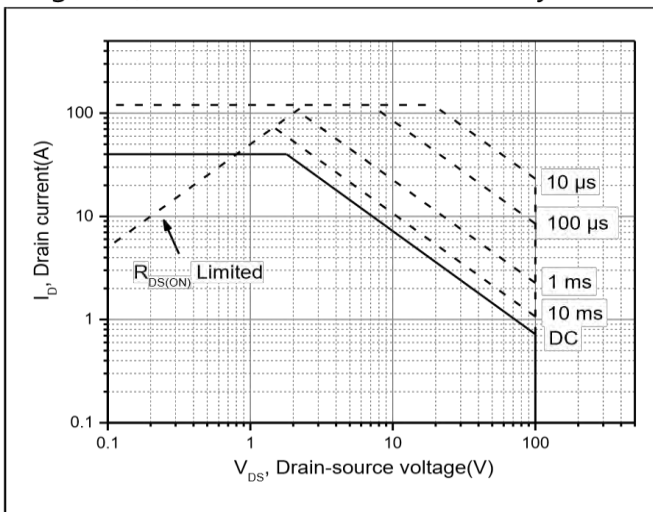


Figure 9, Safe operation area  $T_C=25\text{ }^\circ\text{C}$

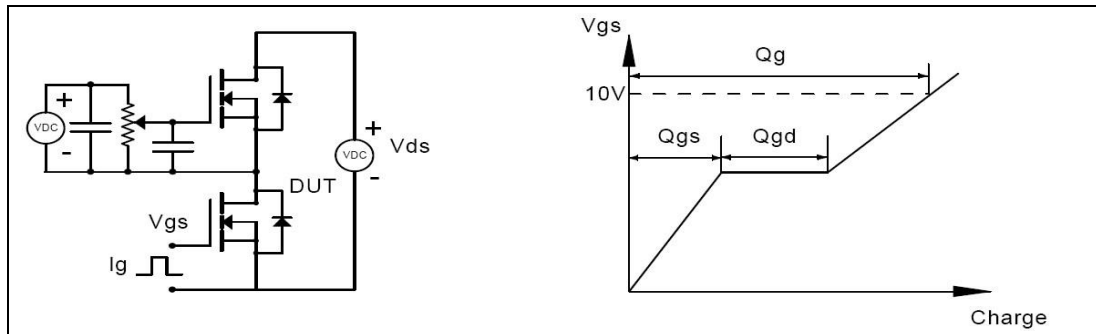


Figure 1, Gate charge test circuit & waveform

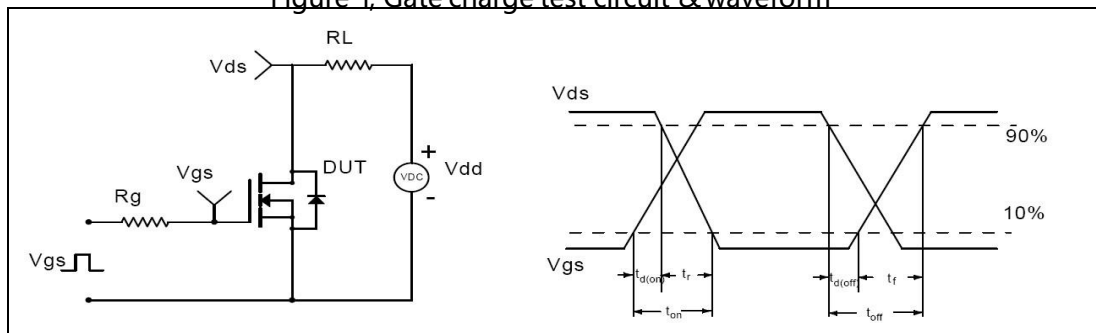


Figure 2, Switching time test circuit & waveforms

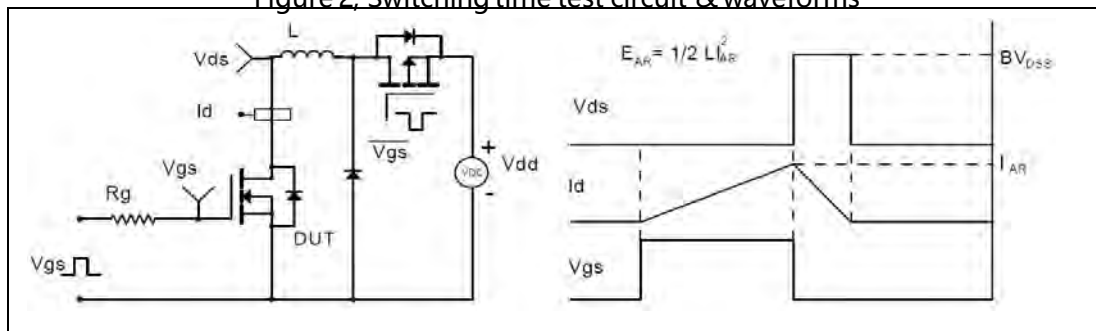


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

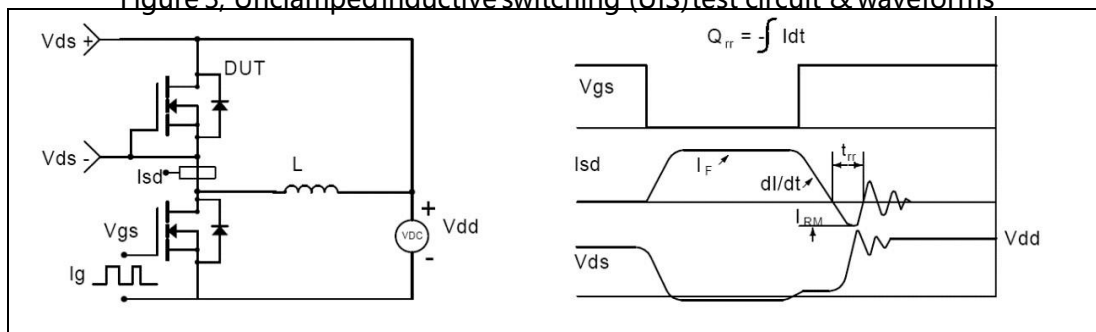
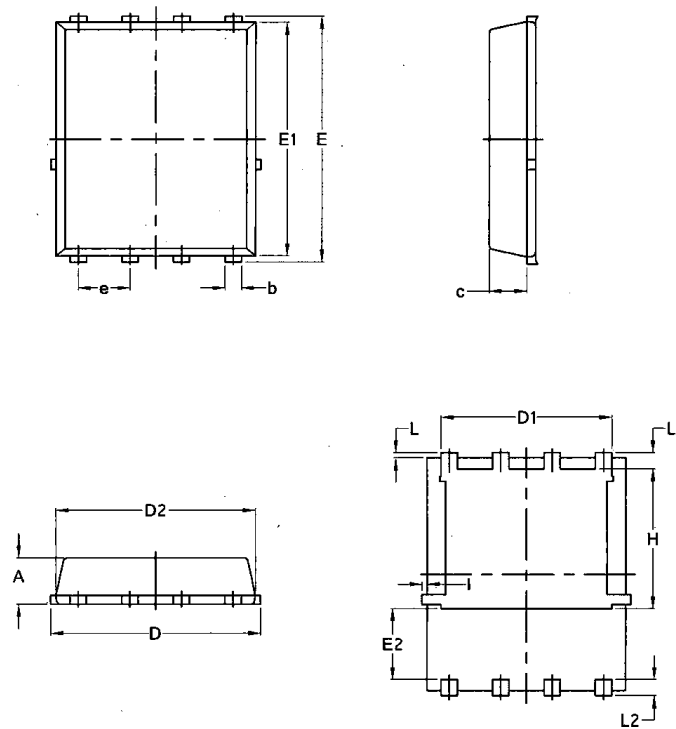


Figure 4, Diode reverse recovery test circuit & waveforms

## Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070