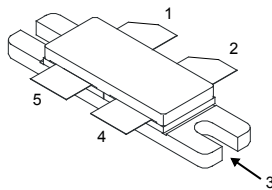


250 W, 28/32 V, HF to 1 GHz, RF Power LDMOS transistor


B4E

Pin connection	
Pin	Connection
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
ST05250	945 MHz	28 V	250 W	13.5 dB	52 %

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the european directive 2002/95/EC

Applications

- 2 – 30 MHz HF or short wave communication
- 30 – 88 MHz ground communication
- 118 – 140 MHz avionics
- 136 – 174 MHz commercial ground communication
- 30 – 512 MHz jammer, ground/air communication
- HF – 1 GHz ISM - instrumentation

Description

The **ST05250** is a 250 W, 28/32 V LDMOS FETs, designed for wideband communication and ISM applications in the frequency range from HF to 1 GHz. It can be used in class AB, B or C for all typical modulation formats.



Product status link
ST05250

Product summary	
Order code	ST05250
Marking	ST05250
Package	B4E
Packing	Tape and reel 13"
Base / Bulk qty	120 / 120

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_{CASE}= 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	90	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	36	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	0.32	°C/W

1. $T_C= 85\text{ °C}$, $T_J=200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified).

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	90			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 28\text{ V}$			1	nA
		$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$				
I_{GSS}	Gate-body leakage current	$V_{GS} = -8/+10\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 28\text{ V}, I_D = 650\text{ }\mu\text{A}$	1		3	V
$V_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 0.7\text{ A}$			0.21	V
C_{iss}	Common source input capacitance	$V_{GS} = 0\text{ V}, V_{DD} = 28\text{ V}, f = 1\text{ MHz}$		123		pF
C_{oss}	Common source output capacitance			2.5		
C_{rss}	Common source feedback capacitance			40		

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$f = 945\text{ MHz}, 3\text{dB compression}$	-	250		W
G_{PS}	Power gain		-	13.5		dB
η_D	Drain efficiency		-	52		%
VSWR	Load mismatch	At $P_{OUT} = 250\text{ W}$ all phases	-		10:1	

Note: $V_{DD} = 28\text{ V}, I_{DQ} = 500\text{ mA}$, pulsed CW, pulse width = 20 μs , duty cycle = 10%.

3 Typical performances

Figure 1. P_{1dB} and drain efficiency versus frequency (2 - 130MHz)

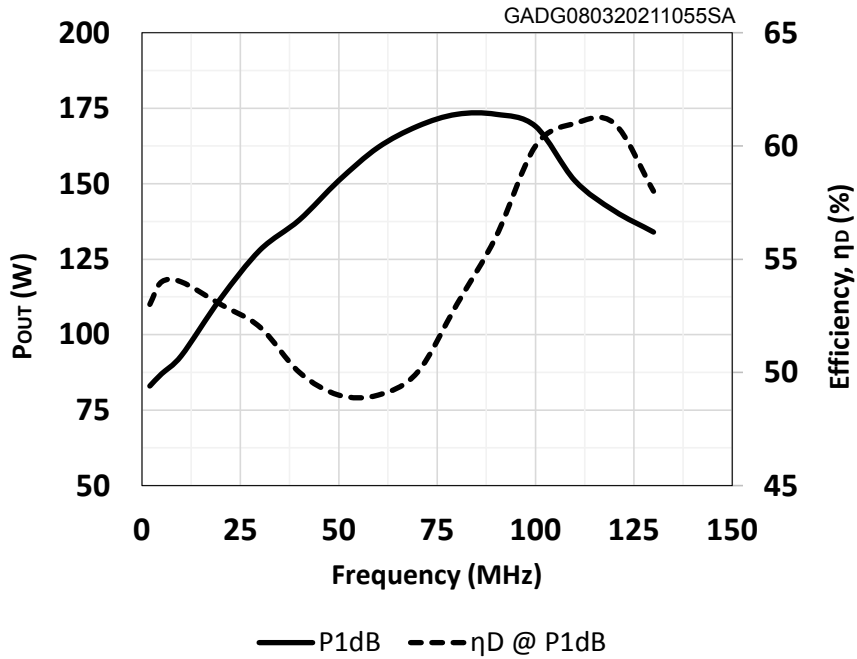


Figure 2. P_{3dB} and drain efficiency versus frequency (2 - 130 MHz)

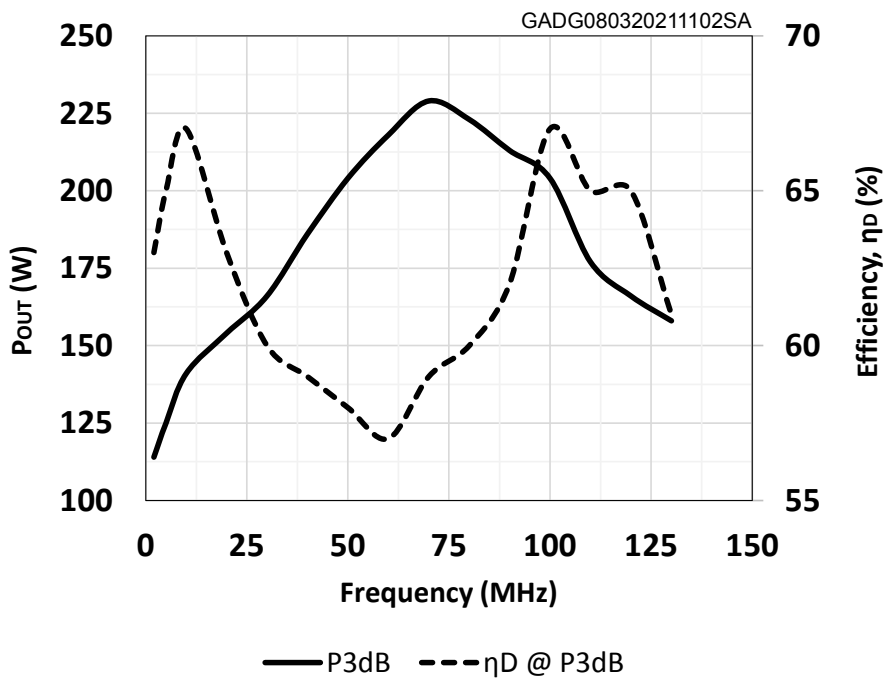


Figure 3. P_{3dB} and drain efficiency versus frequency (30 - 512 MHz)

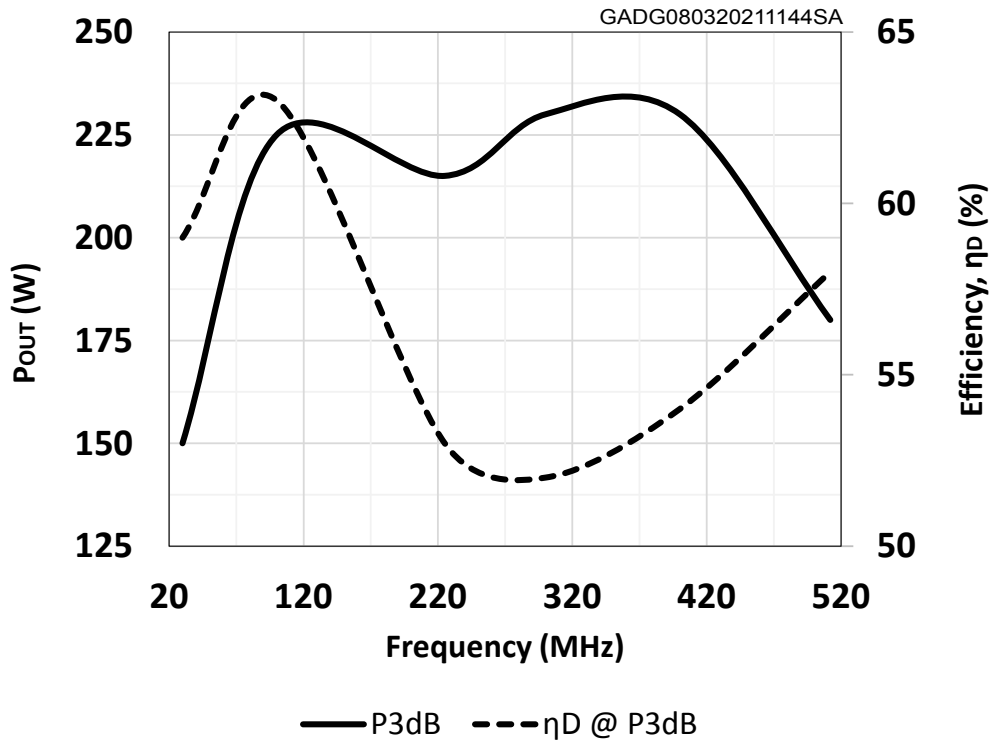
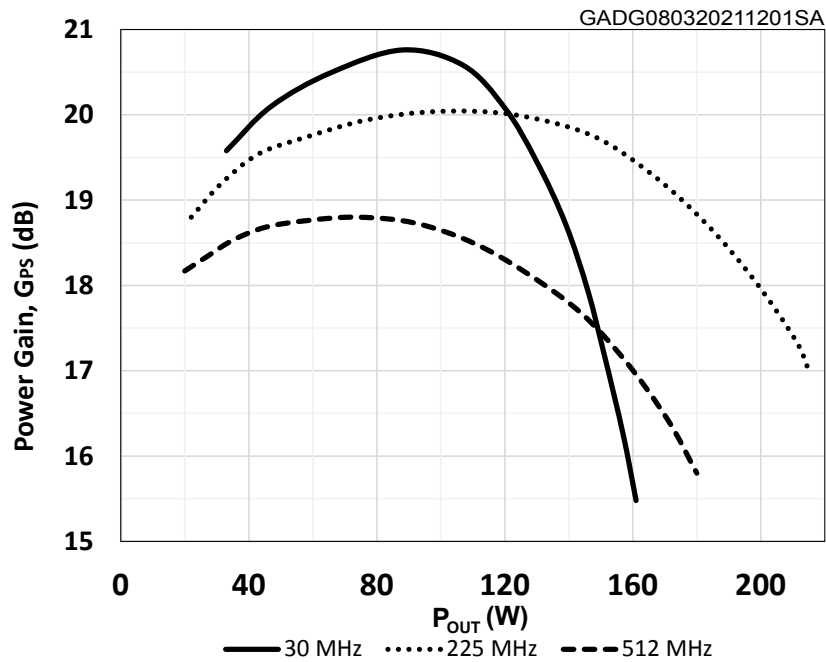


Figure 4. Power gain versus output power (30 - 512 MHz)



Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 200\text{ mA}$, CW signal.

Figure 5. Power gain and drain efficiency versus output power (f=945 MHz)

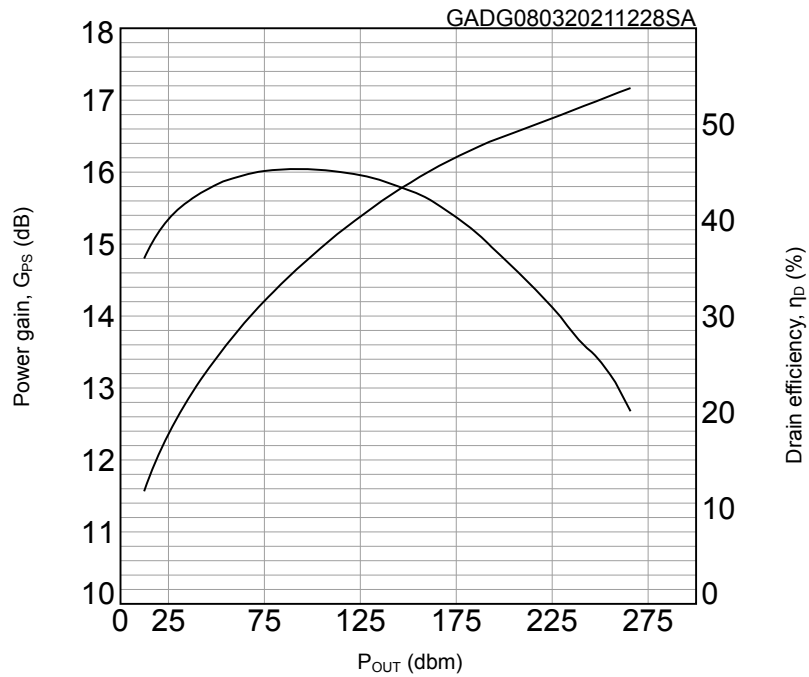
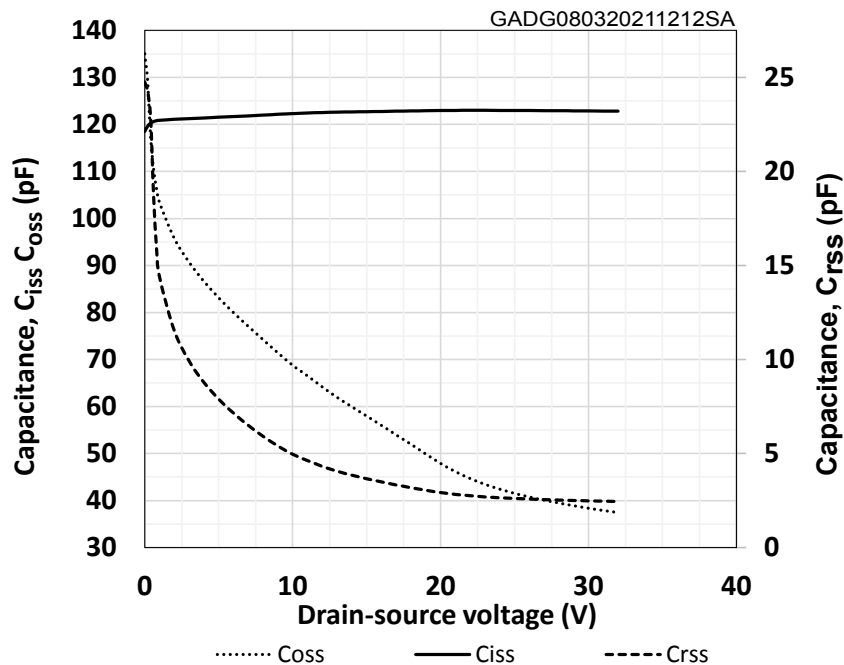
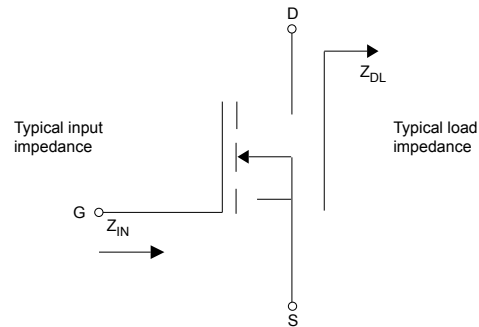


Figure 6. Capacitance vs drain voltage at 1 MHz



4 Impedance

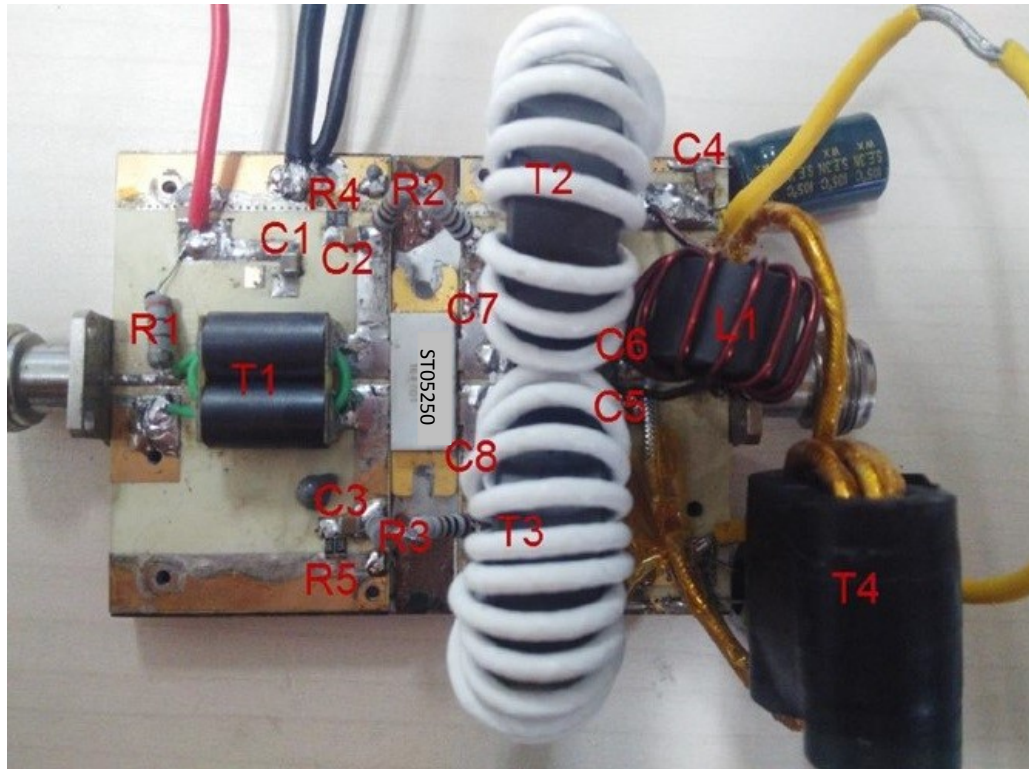
Figure 7. Current conventions

Table 6. Impedance data

Frequency	$Z_{in}(\Omega)$	$Z_{DL}(\Omega)$
2	49.9 -j2.26	5 +j0.002
5	49.35 -j5.6	5+j0.005
10	47.5 -j10.75	5+j0.01
20	41.3 - j18.6	5+j0.02
30	34 -j22.8	5+j0.03
50	22 -j24	4.99+j0.047
70	14.6 -j21.6	4.99+j0.066
90	10.35 -j18.8	4.982+j0.084
100	8.5 -j17.5	4.98+j0.1
200	3.37 -j10.8	4.91+j0.17
300	1.6 -j6.7	4.8+j0.24
400	1.59 -j4.3	4.76+j0.245
500	1.64 -j4.35	4.53 +j0.225
600	1.19-j2.22	4.34+j0.29
700	1.175-j1.55	4.15+j0.24
800	1.16-j0.98	3.96+j0.155
900	1.16-j0.49	3.76+j0.04
1000	1.155-j0.05	3.58-j0.1

Note: Measured gate-to-gate and drain-to-drain, respectively (balanced configuration).

5 Test circuits

Figure 8. Test circuit photo (2 - 130 MHz)

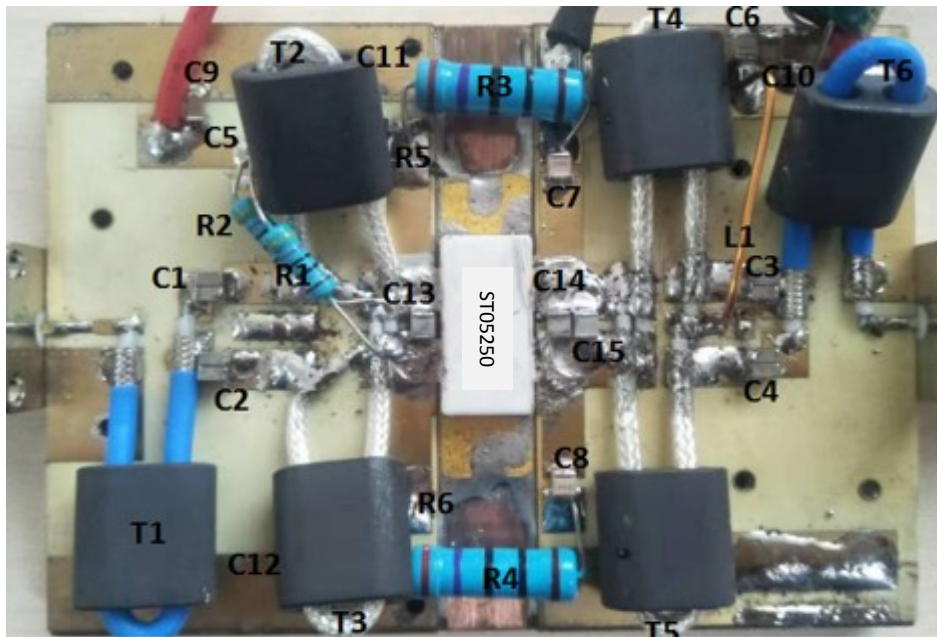


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Table 7. Components list (2 - 130 MHz)

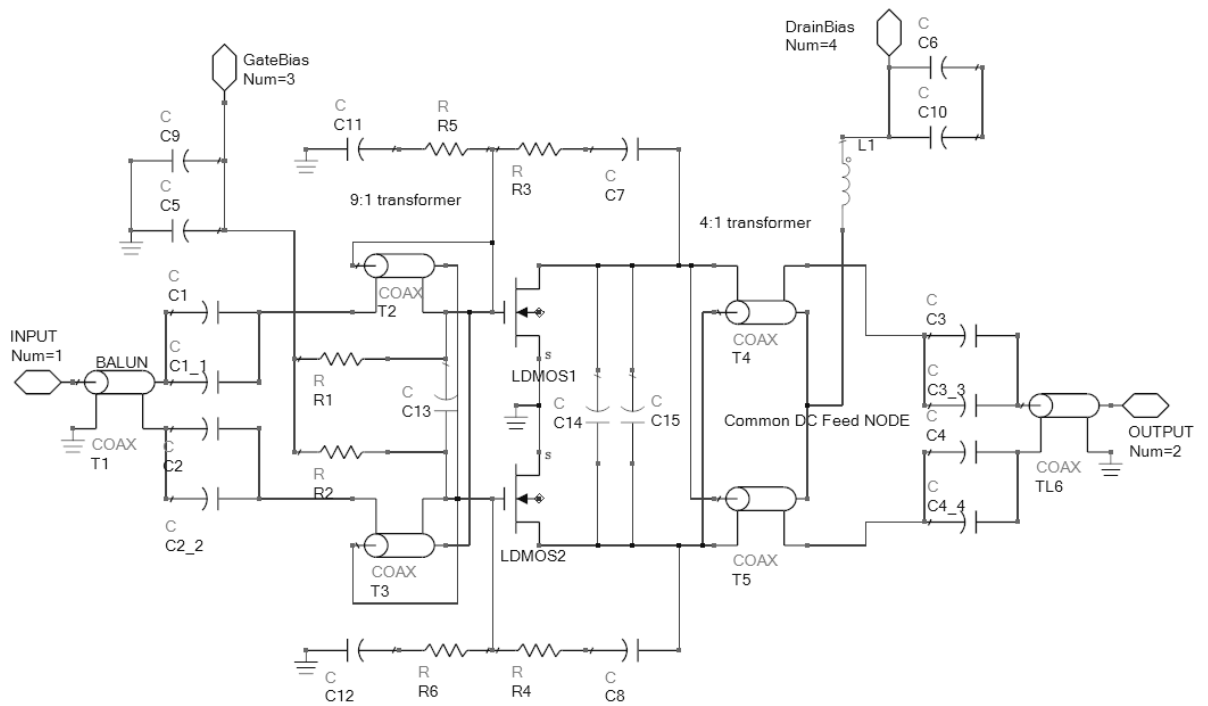
Component	Value	Description/manufacturer
C1, C2, C3, C4, C5, C6, C7, C8	10 μ F	100 V ceramic multilayer capacitor
R1, R2, R3	300 Ω	3 W chip resistor
R4, R5	27 Ω	3 W chip resistor
T1	4:1 transformer	Fair rite 2843000202
T2, T3	TC-22 13 turns	AMI DONCORP FT-140-73 UI = 2500
T4	50 Ω - 4 turns	Fair rite 2643625102 UI = 800
L1	12 turns	Fair rite 2643665802 UI = 800
PCB	0.762 mm [0.030"] thick, $\epsilon_r = 3.48$, Rogers RO4350B	

Figure 9. Test circuit photo (30 - 512 MHz)



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Figure 10. Test circuit schematic (30 - 512 MHz)

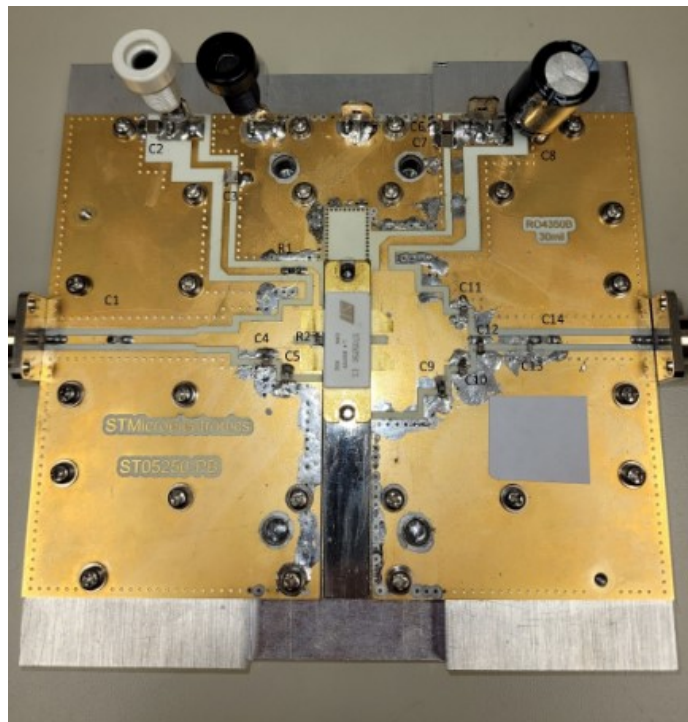


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Table 8. Components list (30 - 512 MHz)

Component	Value	Description/manufacturer
C1, C2, C3, C4	120 pF	ATC800B
C5, C6, C7, C8	1 nF	DCL70B
C9, C10, C11, C12	10 μ F	100V ceramic multilayer capacitor
C13, C14, C15	10 pF	ATC800B
R1, R2	470 Ω	1 W
R3, R4	270 Ω	3 W
R5, R6	2*33 Ω	0805 chip resistor
T1, T6	50 Ω - 70 mm	BN-61-202 SF-086-1.5
T2, T3	17.5 Ω - 70 mm	BN-61-202 SFF-17.5-1.5
T4, T5	12.5 Ω - 70 mm	BN-61-202 SFF-12.5-1.5
L1	40 mm	Diameter = 0.7 mm
PCB	0.762 mm (0.030") thick, $\epsilon_r = 3.48$, Rogers RO4350B	

Figure 11. Test circuit photo (f= 945 MHz)



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Table 9. Components list (f= 945 MHz)

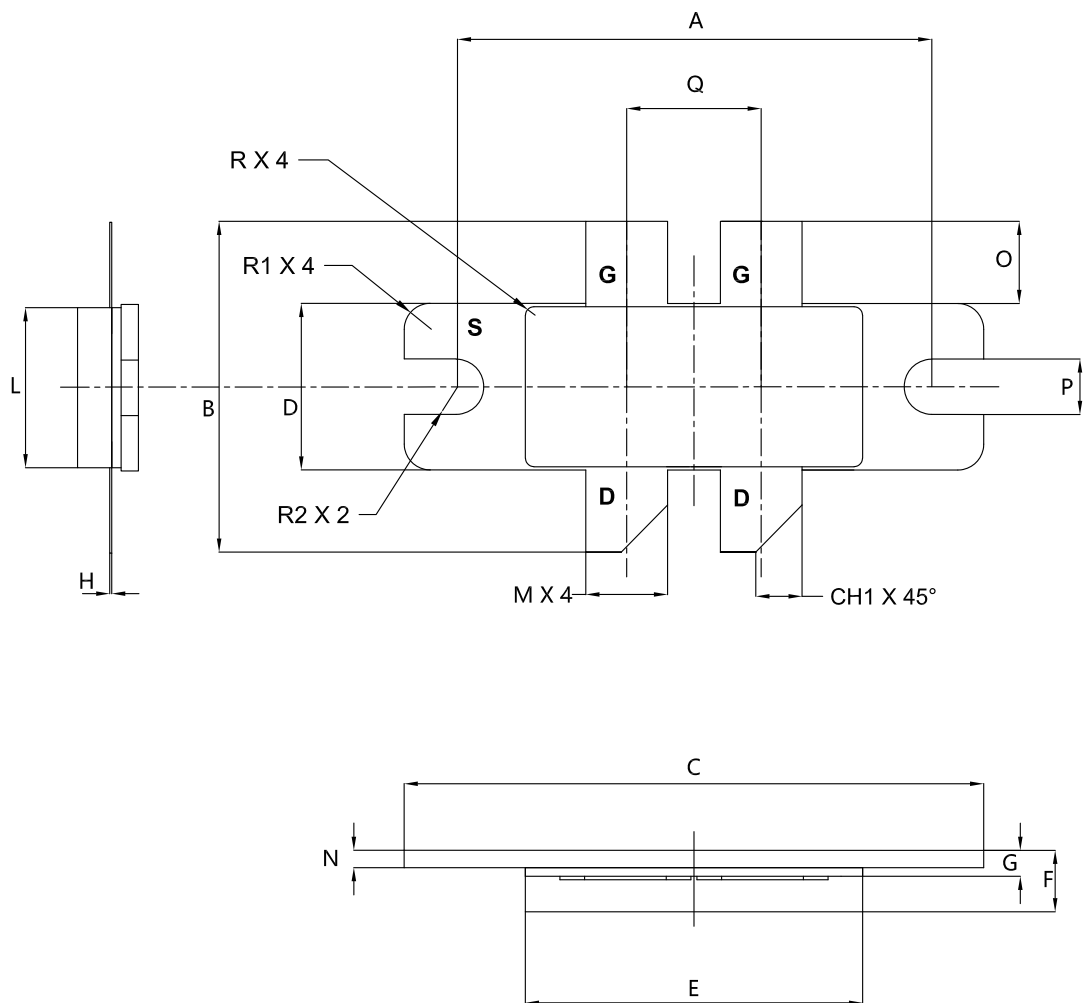
Component	Value	Description/manufacturer
C1, C14	39 pF	ATC 100A
C2, C6	10 μ F	1206 50 V chip capacitor
C3, C7	39 pF	ATC 100B
C4	12 pF	ATC 100A
C5, C9, C10	6.8 pF	ATC 100A
C8	470 μ F	63 V electrolytic
C11, C12	1.2 pF	ATC 100A
C13	0.6 pF	ATC 100A
R1, R2	10 Ω	063 chip resistor
PCB	0.762 mm (0.030") thick, $\epsilon_r = 3.48$, Rogers RO4350B	

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 B4E package information

Figure 12. B4E package outline



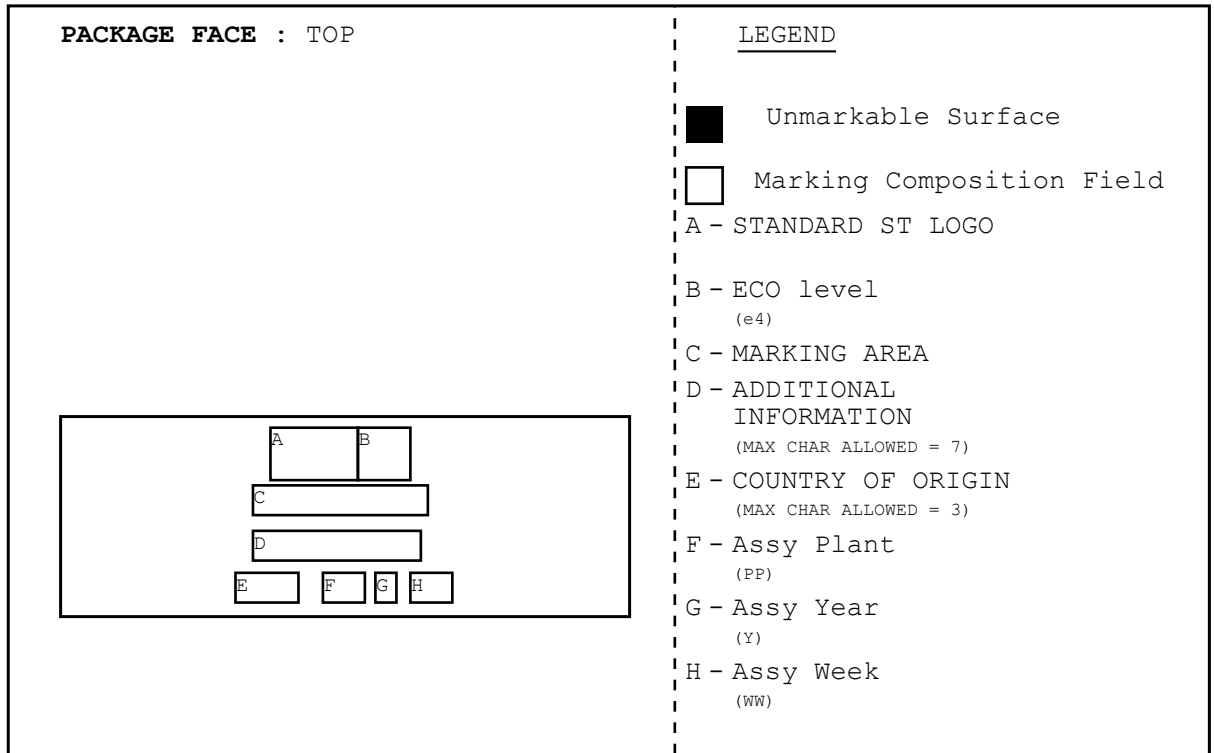
DM00418520_2

Table 10. B4E package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	27.81	27.94	28.07
B	18.93	19.43	19.93
C	33.91	34.04	34.17
D	9.65	9.78	9.91
E	19.56	19.81	20.06
F	3.23	3.61	3.99
G	1.40	1.53	1.66
H	0.07		0.15
L	9.20	9.40	9.60
M	4.67	4.80	4.93
N	0.89	1.02	1.15
O	4.70	4.83	4.96
P	3.13	3.26	3.39
Q	7.77	7.90	8.03
R		0.50	
R1		1.52	
R2		1.63	
CH1		2.72	

7 Marking information

Figure 13. Marking composition



GADG040220211644GT

Revision history

Table 11. Document revision history

Date	Version	Changes
01-Aug-2018	1	Initial release.
09-Sep-2020	2	Updated <i>Section Product status / summary</i> , <i>Table 5. Dynamic</i> and <i>Section 4.1 B4E package information</i> .
23-Nov-2020	3	Updated <i>Figure 1. Output power and efficiency vs frequency</i> . Minor text changes.
15-Mar-2021	4	Modified Gain value in features table on cover page Modified <i>Table 2. Thermal data</i> , <i>Table 3. ESD protection</i> , <i>Table 4. Static (per side)</i> , <i>Table 5. Dynamic</i> . Added <i>Section 3 Typical performance</i> . Modified the entire <i>Section 5 Test circuits</i> .

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
3	Typical performances	4
4	Impedance	7
5	Test circuits	8
6	Package information	12
6.1	B4E package information	12
7	Marking information	14
	Revision history	15

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