

RoHS

COMPLIANT

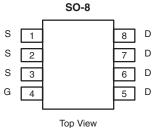
HALOGEN

FREE

F7459U-VB Datasheet

N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)			
20	0.0049 at V_{GS} = 4.5 V	20 ^e	27.5 nC			
	0.0056 at V_{GS} = 2.5 V	20 ^e	27.3110			

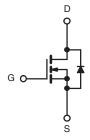


FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Low-Side MOSFET for Synchronous Buck - Game Machine
 - PC



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	20	V	
Gate-Source Voltage		V _{GS}	± 16	v	
	T _C = 25 °C		20 ^e		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C		18.2		
	T _A = 25 °C		15.2 ^{b, c}		
	T _A = 70 °C		12.1 ^{b, c}	Α	
Pulsed Drain Current		I _{DM}	50	A	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	5.1		
	T _A = 25 °C		2.2 ^{b, c}		
Single Pulse Avalanche Current		I _{AS}	30		
Avalanche Energy	L = 0.1 mm	E _{AS}	45	mJ	
	T _C = 25 °C	– – P _D	5.7		
Maximum Power Discinction	T _C = 70 °C		3.6	w	
Maximum Power Dissipation	T _A = 25 °C		2.5 ^{b, c}	vv	
	T _A = 70 °C	1	1.6 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	39	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	18	22	0/11		

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 85 °C/W.

e. Package limited.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	20			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			19		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 5.3		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.0		2.1	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 16 V$			± 100	nA
		$V_{DS} = 20 V, V_{GS} = 0 V$			1	μΑ
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 20 V, V_{GS} = 0 V, T_{J} = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5$ V, $V_{GS} = 10$ V	30			Α
	_	V _{GS} = 4.5 V, I _D = 10 A		0.0049		Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 7 A		0.0056		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 10 A		55		S
Dynamic ^b						1
Input Capacitance	C _{iss}			3700		pF
Output Capacitance	C _{oss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		745		
Reverse Transfer Capacitance	C _{rss}			315		
		$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		62	95	
Total Gate Charge	Qg			27.5	42	nC
Gate-Source Charge	Q _{gs}	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 10 A		8.0		
Gate-Drain Charge	Q _{gd}			6.0		
Gate Resistance	Rg	f = 1 MHz	0.15	0.7	1.4	Ω
Turn-On Delay Time	t _{d(on)}			30	55	-
Rise Time	t _r	V_{DD} = 10 V, R_L = 2 Ω		13	25	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong \text{5}$ A, V_GEN = 4.5 V, R_g = 1 Ω		60	100	
Fall Time	t _f			30	55	-
Turn-On Delay Time	t _{d(on)}			13	25	ns
Rise Time	t _r	V_{DD} = 10 V, R_L = 2 Ω		9	18	-
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong \text{5}$ A, V_GEN = 10 V, R_g = 1 Ω		38	65	
Fall Time	t _f			8	16	
Drain-Source Body Diode Characterist	ics					
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			5.1	A
Pulse Diode Forward Current ^a	I _{SM}				50	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.71	1.1	V
Body Diode Reverse Recovery Time	t _{rr}			26	50	ns
Body Diode Reverse Recovery Charge	Q _{rr}	t_a $I_F = 10 \text{ A}, \text{ dl/dt} = 100 \text{ A/}\mu\text{s}, \text{ I}_J = 25 \text{ °C}$		16	30	nC
Reverse Recovery Fall Time	t _a			13		
Reverse Recovery Rise Time	t _b			13		ns

Notes:

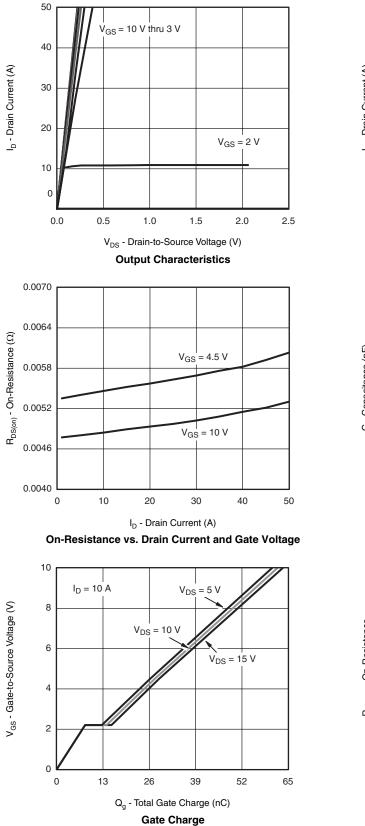
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

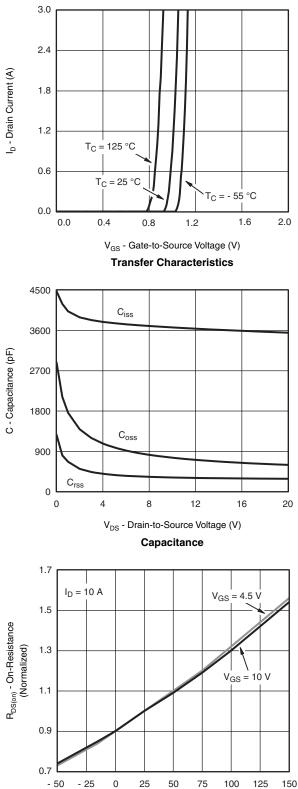
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





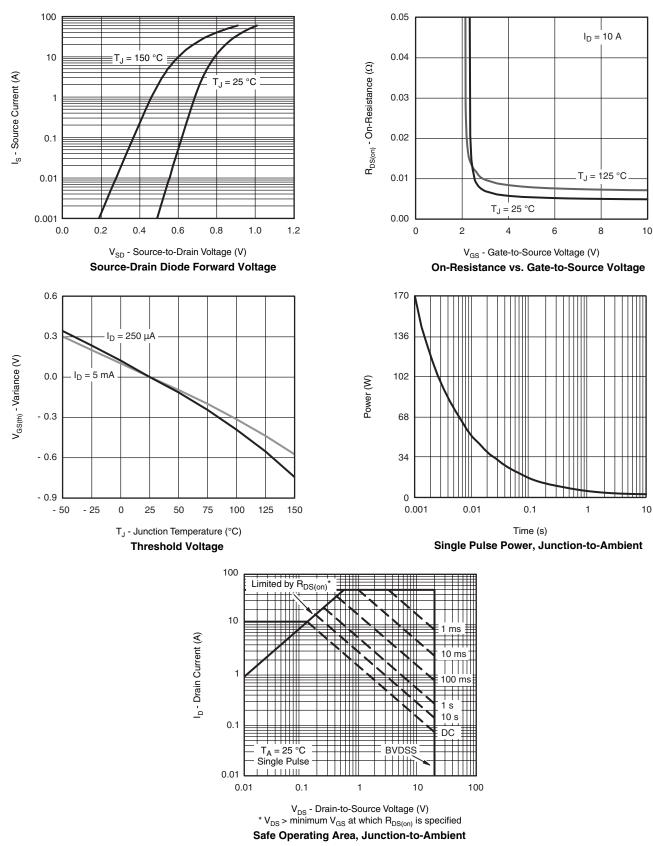




 $\rm T_J$ - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

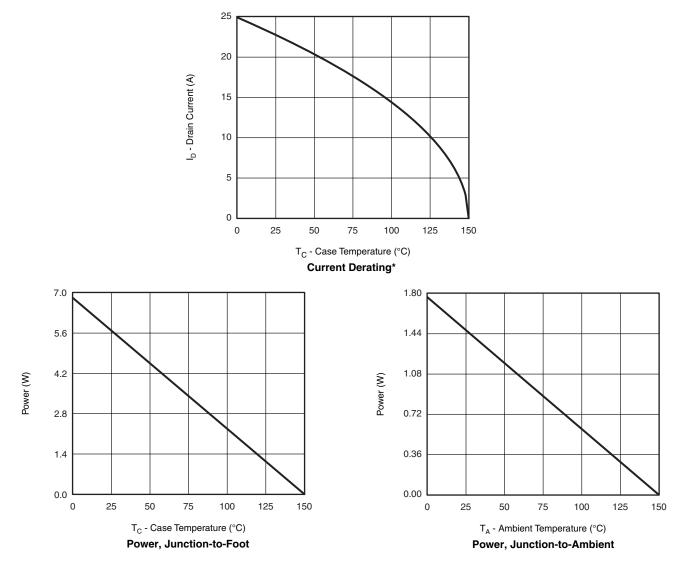




TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



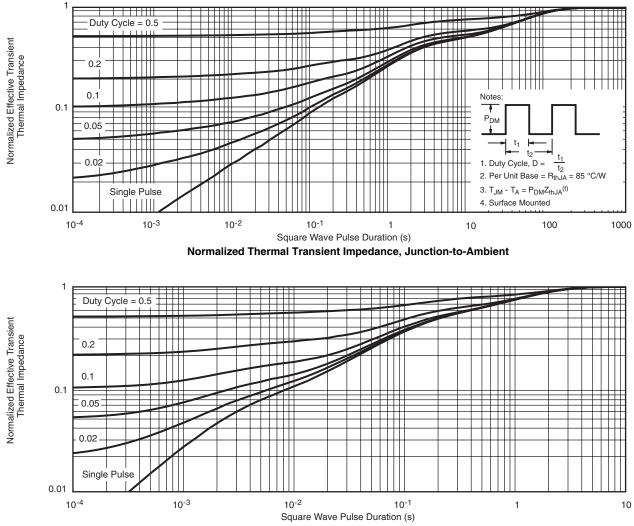
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



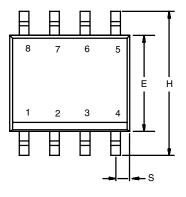


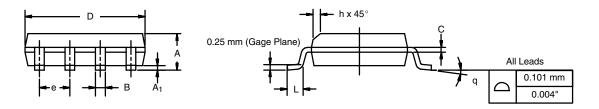






SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012

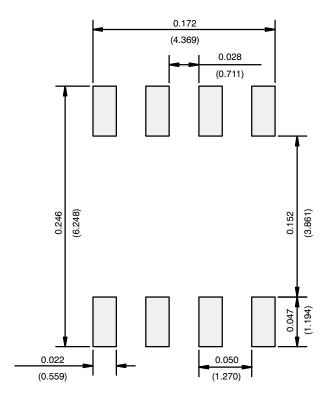




	MILLIM	IETERS	INC	HES	
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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